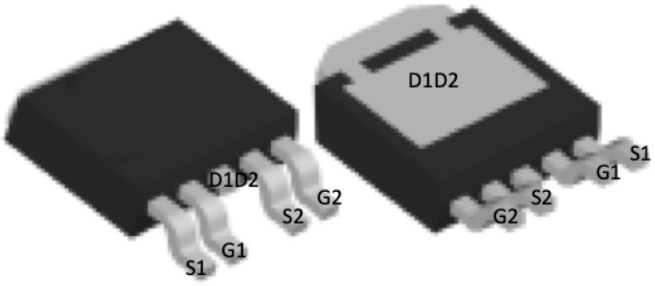
SL607B

N-Channel and P-Channel Complementary Power MOSFET



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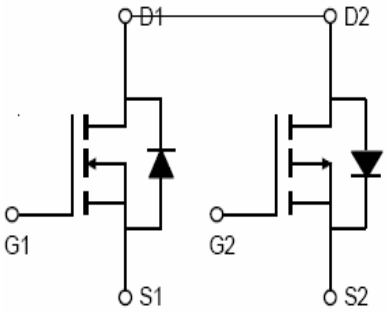

Product Summary

NMOS

- V_{DS} 30V
- I_D 12A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜30mohm
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜45mohm

PMOS

- V_{DS} -30V
- I_D -8A
- $R_{DS(ON)}$(at V_{GS}=-10V) ＜55mohm
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜80mohm

- 100% ∇V_{DS} Tested

General Description

- Trench Power LV MOSFET technology
- High density cell design for low $R_{DS(ON)}$
- High Speed switching

Applications

- Wireless charger
- Load switch
- Power management

■ **Absolute Maximum Ratings** (T_A=25℃unless otherwise noted)

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-source Voltage	V_{DS}	30	-30	V
Gate-source Voltage	V_{GS}	±20	±20	V
Drain Current	I_D	12	-8	A
Pulsed Drain Current [A]	I_{DM}	30	-20	A
Total Power Dissipation	P_D	15	15	W
Thermal Resistance Junction-to-Ambient [B]	$R_{\theta JA}$	62.5	62.5	℃/ W
Junction and Storage Temperature Range	T_J ,T_{STG}	-55～+150	-55～+150	℃

■ N-MOS Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.0	1.5	2.2	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=5.6A		20	30	mΩ
		V_{GS}=4.5V, I_D=5.0A		30	45	
Diode Forward Voltage	V_{SD}	I_S=5.6A,V_{GS}=0V			1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=15V,V_{GS}=0V,f=1MHZ		490		pF
Output Capacitance	C_{oss}			92		
Reverse Transfer Capacitance	C_{rss}			69		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=15V,I_D=5.6A		5.2		nC
Gate-Source Charge	Q_{gs}			0.9		
Gate-Drain Charge	Q_{gd}			1.2		
Reverse Recovery Chrage	Q_{rr}	I_F=5.6A, di/dt=100A/us		1.28		
Reverse Recovery Time	t_{rr}			16.5		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=4.5V, V_{DS}=15V, I_D=1A R_{GEN}=3Ω		4.5		
Turn-on Rise Time	t_r			2.5		
Turn-off Delay Time	$t_{D(off)}$			12.8		
Turn-off fall Time	t_f			3.5		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ P-MOS Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=-250μA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V,V_{GS}=0V			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-1.0	-1.5	-2.4	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-5.0A		43	55	mΩ
		V_{GS}=-4.5V, I_D=-4.0A		55	80	
Diode Forward Voltage	V_{SD}	I_S=-4A,V_{GS}=0V			-1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-15V,V_{GS}=0V,f=1MHZ		719		pF
Output Capacitance	C_{oss}			441		
Reverse Transfer Capacitance	C_{rss}			118		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-10V,V_{DS}=-15V,I_D=-5.1A		27		nC
Gate-Source Charge	Q_{gs}			2.6		
Gate-Drain Charge	Q_{gd}			6.6		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V, V_{DS}=-15V, I_D=-1A R_{GEN}=6Ω		8		ns
Turn-on Rise Time	t_r			15		
Turn-off Delay Time	$t_{D(off)}$			77		
Turn-off fall Time	t_f			42		

C. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

D. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ N-MOS Typical Performance Characteristics

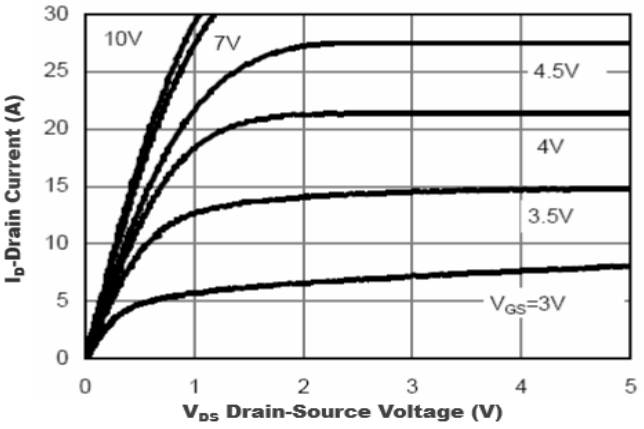

Figure1. Output Characteristics

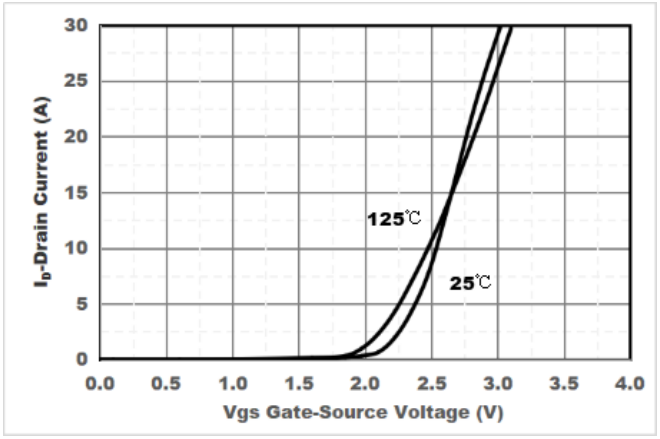

Figure2. Transfer Characteristics

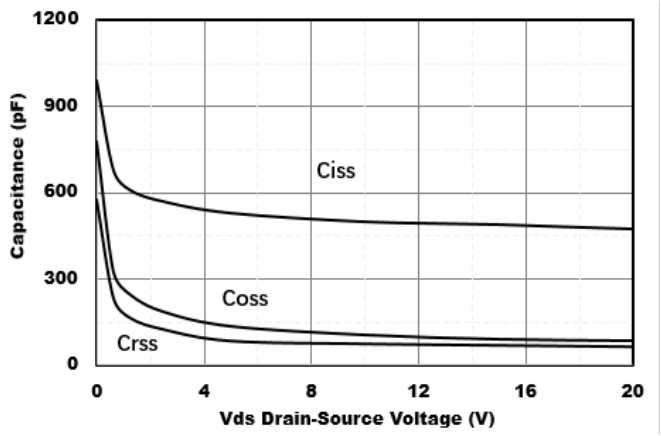

Figure3. Capacitance Characteristics

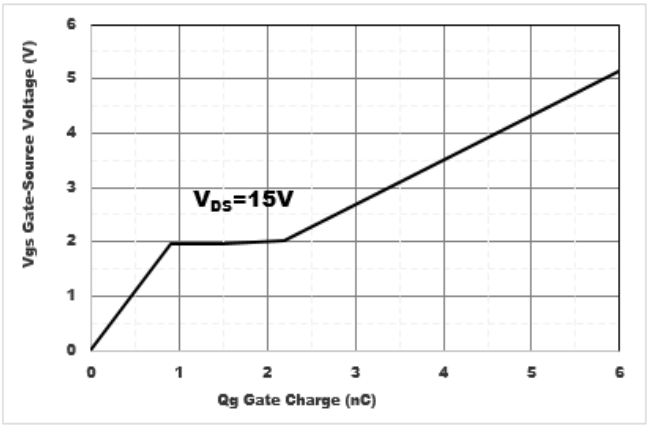

Figure4. Gate Charge

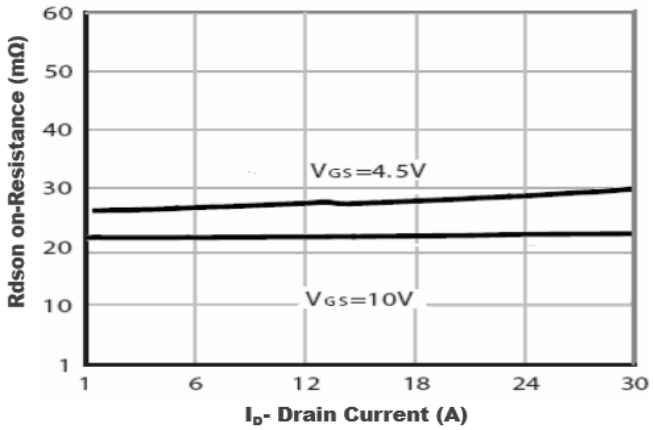

Figure5. Drain-Source on Resistance

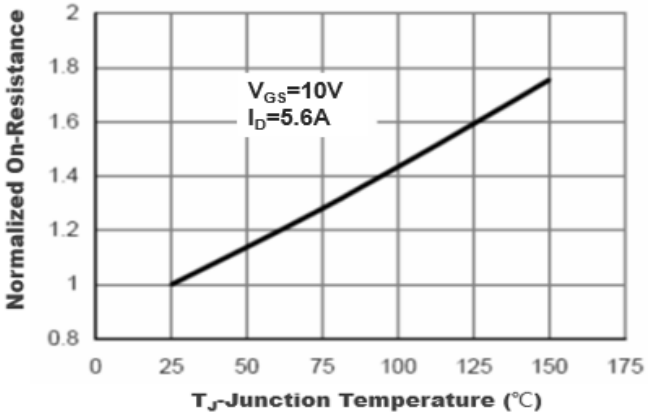

Figure6. Drain-Source on Resistance

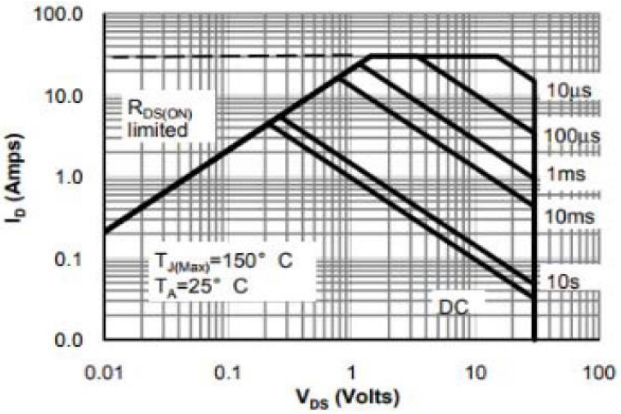

Figure7. Safe Operation Area

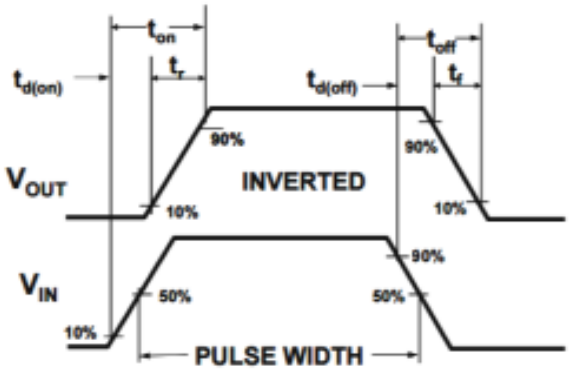

Figure8. Switching wave

■ P-MOS Typical Performance Characteristics

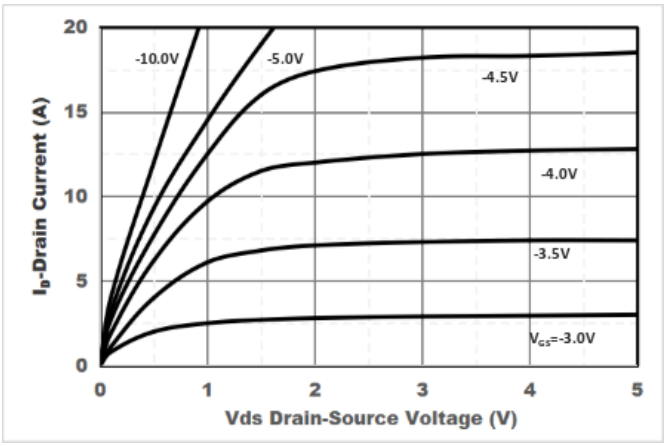

Figure1. Output Characteristics

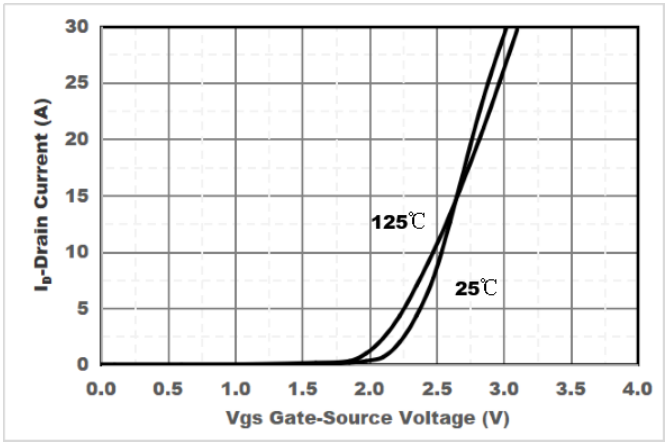

Figure2. Transfer Characteristics

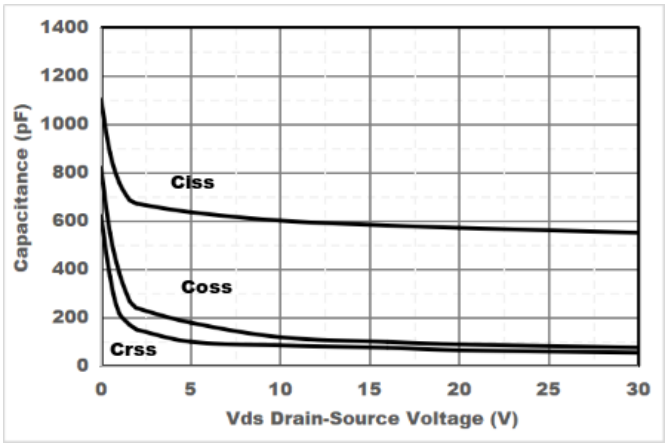

Figure3. Capacitance Characteristics

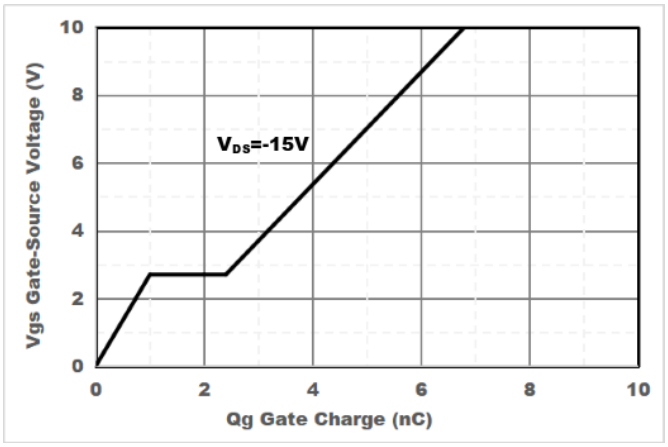

Figure4. Gate Charge

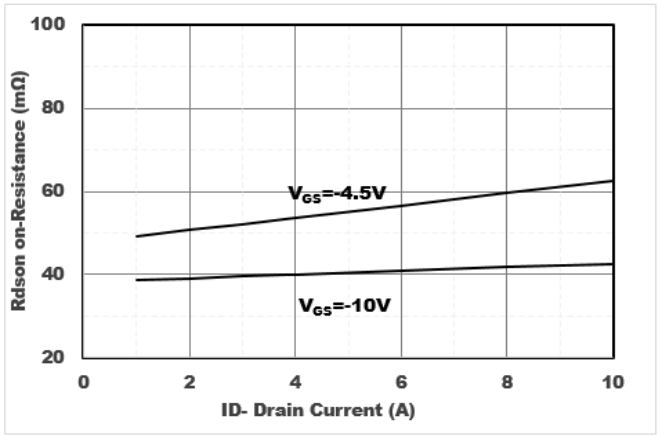

Figure5. Drain-Source on Resistance

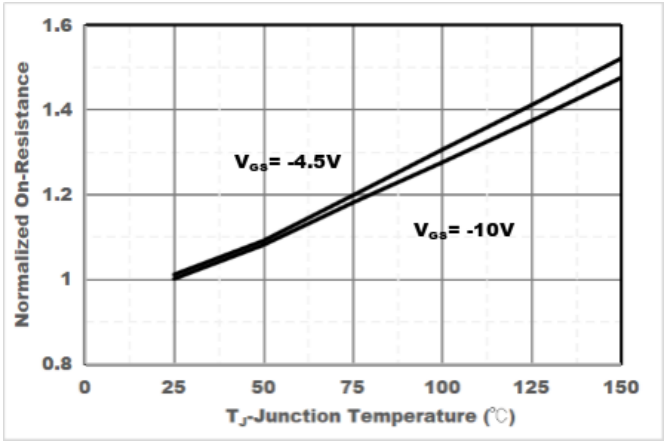

Figure6. Drain-Source on Resistance

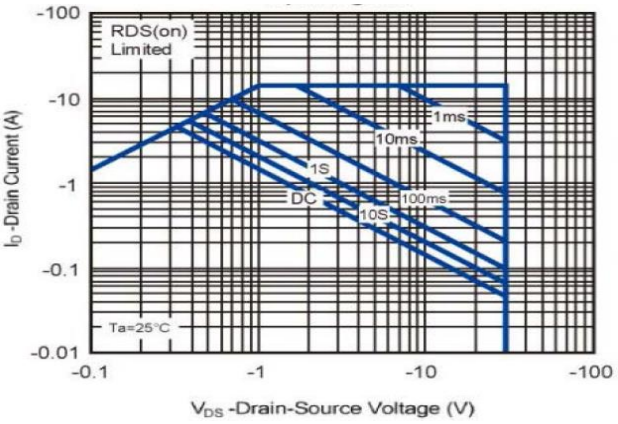

Figure7. Safe Operation Area

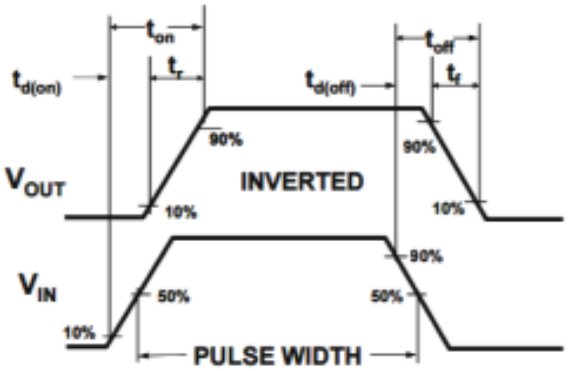

Figure8. Switching wave

■ TO-252-4L Package information