

**LOW-JITTER SAW OSCILLATOR (SPSO)**

OUTPUT : LV-PECL, LVDS, HCSSL



Product Number  
 EG-2121CA: Q3805CAx0xxxx00  
 : X1M000101xxxx00  
 EG-2102CA: Q3806CA00xxxx00  
 : X1M000091xxxx00

**EG-2121CA**  
**EG-2102CA**



- Frequency range : 53.125 MHz to 700 MHz
- Supply voltage : 2.5 V ... EG-2121CA  
3.3 V ... EG-2102CA
- Output : LV-PECL or LVDS or HCSSL
- Function : Output enable (OE)
- External dimensions : 7.0 × 5.0 × 1.2 mm

•Very low jitter and low phase noise by SAW unit.

**Specifications (characteristics)**

► Differential LV-PECL Output

| Item                        | Symbol  | EG-2121CA  |  | EG-2102CA                                     |  | Conditions / Remarks   |                                    |
|-----------------------------|---|--|--|---|--|--|------------------------------------|
|                             |   | LV-PECL  |  |   |  |  |                                    |
| Output frequency range      | f <sub>o</sub>                                      | 53.125 MHz to 500 MHz                                      |  | 100 MHz to 700 MHz                            |  | Please contact us about available frequencies.               |                                    |
| Supply voltage              | V <sub>CC</sub>                                     | 2.5 V ± 0.125 V  |  | 3.3 V ± 0.3 V                                 |  |  |                                    |
| Storage temperature         | T <sub>stg</sub>                                    | -40 °C to +100 °C  |  |   |  | Storage as single product.                                   |                                    |
| Operating temperature       | T <sub>use</sub>                                    | P: 0 °C to +70 °C, R: -5 °C to +85 °C, S: -20 °C to +70 °C |  |   |  |  |                                    |
| Frequency tolerance         | f <sub>tol</sub>                                    | G: ± 50 × 10 <sup>-6</sup> , H: ± 100 × 10 <sup>-6</sup>   |  |   |  |  |                                    |
| Current consumption         | I <sub>CC</sub>                                     | 80 mA Max.   |  | 100 mA Max.                                   |  | OE=V <sub>CC</sub> , L ECL=50 Ω                              |                                    |
| Disable current             | I <sub>dis</sub>                                    | 20 mA Max.   |  | 32 mA Max.                                    |  | OE=GND   |                                    |
| Symmetry                    | SYM   | P: 40 % to 60 %<br>(f <sub>o</sub> > 350 MHz)              |  | P: 45 % to 55 %                               |  | at outputs crossing point                                    |                                    |
|                             |   | P: 45 % to 55 %<br>(f <sub>o</sub> ≤ 350 MHz)              |  |   |  |  |                                    |
|                             |   | D: 48 % to 52 %<br>(f <sub>o</sub> ≤ 175 MHz)              |  | D: 48 % to 52 %<br>(f <sub>o</sub> ≤ 350 MHz) |  |  |                                    |
| Output voltage              | V <sub>OH</sub>                                     | 1.55 V Typ.  |  | 2.35 V Typ.                                   |  | DC characteristics   |                                    |
|                             | V <sub>CC</sub> -1.025 V to V <sub>CC</sub> -0.88 V |  |  |   |  |  |                                    |
|                             | V <sub>OL</sub>                                     | 0.8 V Typ.   |  | 1.6 V Typ.                                    |  |  |                                    |
| Output load condition (ECL) | L <sub>ECL</sub>                                    | V <sub>CC</sub> -1.81 V to V <sub>CC</sub> -1.62 V         |  |   |  | Terminated to V <sub>CC</sub> -2.0 V                         |                                    |
| Input voltage               | V <sub>IH</sub>                                     | 70 % V <sub>CC</sub> Min.                                  |  |   |  | OE terminal  |                                    |
|                             | V <sub>IL</sub>                                     | 30 % V <sub>CC</sub> Max.                                  |  |   |  |  |                                    |
| Rise time / Fall time       | t <sub>r</sub> / t <sub>f</sub>                     | 400 ps Max.  |  |   |  | Between 20 % and 80 % of (V <sub>OH</sub> -V <sub>OL</sub> ) |                                    |
| Start-up time               | t <sub>str</sub>                                    | 10 ms Max.   |  |   |  | Time at minimum supply voltage to be 0 s                     |                                    |
| Phase Jitter                | t <sub>pj</sub>                                     | 0.8 ps Max.  |  |   |  | f <sub>o</sub> < 100 MHz                                     | Offset frequency: 12 kHz to 20 MHz |
|                             |   | 0.5 ps Max.  |  |   |  | 100 MHz ≤ f <sub>o</sub> < 200 MHz                           |                                    |
|                             |   | 0.3 ps Max.  |  |   |  | 200 MHz ≤ f <sub>o</sub>                                     |                                    |
| Frequency aging             | f <sub>aging</sub>                                  | ± 10 × 10 <sup>-6</sup> / year Max.                        |  |   |  | +25 °C, First year, V <sub>CC</sub> =2.5 V, 3.3 V            |                                    |

► LVDS Output

| Item                         | Symbol                          | EG-2121CA  |  | EG-2102CA                                     |  | Conditions / Remarks  |                                    |
|------------------------------|---------------------------------|--|--|---|--|---|------------------------------------|
|                              |                                 | LVDS   |  |   |  |   |                                    |
| Output frequency range       | f <sub>o</sub>                  | 53.125 MHz to 700 MHz                                      |  |   |  | Please contact us about available frequencies.                    |                                    |
| Supply voltage               | V <sub>CC</sub>                 | 2.5 V ± 0.125 V  |  | 3.3 V ± 0.3 V                                 |  |   |                                    |
| Storage temperature          | T <sub>stg</sub>                | -40 °C to +100 °C  |  |   |  | Storage as single product.  |                                    |
| Operating temperature        | T <sub>use</sub>                | P: 0 °C to +70 °C, R: -5 °C to +85 °C, S: -20 °C to +70 °C |  |   |  |   |                                    |
| Frequency tolerance          | f <sub>tol</sub>                | G: ± 50 × 10 <sup>-6</sup> , H: ± 100 × 10 <sup>-6</sup>   |  |   |  |   |                                    |
| Current consumption          | I <sub>CC</sub>                 | 30 mA Max.   |  | 45 mA Max.                                    |  | OE=V <sub>CC</sub> , L LVDS= 100 Ω                                |                                    |
| Disable current              | I <sub>dis</sub>                | 20 mA Max.   |  | 30 mA Max.                                    |  | OE=GND  |                                    |
| Symmetry                     | SYM                             | L: 40 % to 60 %<br>(f <sub>o</sub> > 350 MHz)              |  | L: 40 % to 60 %<br>(f <sub>o</sub> > 350 MHz) |  | at outputs crossing point   |                                    |
|                              |                                 | L: 45 % to 55 %<br>(f <sub>o</sub> ≤ 350 MHz)              |  | L: 45 % to 55 %<br>(f <sub>o</sub> ≤ 350 MHz) |  |   |                                    |
|                              |                                 | V: 48 % to 52 %<br>(f <sub>o</sub> ≤ 175 MHz)              |  | V: 48 % to 52 %<br>(f <sub>o</sub> ≤ 175 MHz) |  |   |                                    |
| Output voltage               | V <sub>OD</sub>                 | 350 mV Typ. 247 mV to 454 mV                               |  |   |  | DC characteristics  |                                    |
|                              | dV <sub>OD</sub>                | 50 mV Max.   |  |   |  |   |                                    |
|                              | V <sub>OS</sub>                 | 1.25 V Typ. 1.125 V to 1.375 V                             |  |   |  |   |                                    |
|                              | dV <sub>OS</sub>                | 150 mV Max.  |  |   |  |   |                                    |
| Output load condition (LVDS) | L <sub>LVDS</sub>               | 100 Ω  |  |   |  | Connected between OUT to $\overline{\text{OUT}}$                  |                                    |
| Input voltage                | V <sub>IH</sub>                 | 70 % V <sub>CC</sub> Min.                                  |  |   |  | OE terminal   |                                    |
|                              | V <sub>IL</sub>                 | 30 % V <sub>CC</sub> Max.                                  |  |   |  |   |                                    |
| Rise time / Fall time        | t <sub>r</sub> / t <sub>f</sub> | 400 ps Max.  |  |   |  | Between 20 % and 80 % of Differential Output Peak to Peak voltage |                                    |
| Start-up time                | t <sub>str</sub>                | 10 ms Max.   |  |   |  | Time at minimum supply voltage to be 0 s                          |                                    |
| Phase Jitter                 | t <sub>pj</sub>                 | 0.8 ps Max.  |  |   |  | f <sub>o</sub> < 100 MHz  | Offset frequency: 12 kHz to 20 MHz |
|                              |                                 | 0.5 ps Max.  |  |   |  | 100 MHz ≤ f <sub>o</sub> < 200 MHz                                |                                    |
|                              |                                 | 0.3 ps Max.  |  |   |  | 200 MHz ≤ f <sub>o</sub>  |                                    |
| Frequency aging              | f <sub>aging</sub>              | ± 10 × 10 <sup>-6</sup> / year Max.                        |  |   |  | +25 °C, First year, V <sub>CC</sub> =2.5 V, 3.3 V                 |                                    |

► HCSL Output

| Item                         | Symbol                          | EG-2121CA  |  | EG-2102CA     |  | Conditions / Remarks                              |
|------------------------------|---------------------------------|--|--|---------------|--|---|
|                              |                                 | HCSL   |  |               |  |   |
| Output frequency range       | fo                              | 100 MHz to 350 MHz   |  |               |  | Please contact us about available frequencies.    |
| Supply voltage               | V <sub>CC</sub>                 | 2.5 V ± 0.125 V  |  | 3.3 V ± 0.3 V |  |   |
| Storage temperature          | T <sub>stg</sub>                | -40 °C to +125 °C  |  |               |  | Storage as single product.                        |
| Operating temperature        | T <sub>use</sub>                | P: 0 °C to +70 °C, R: -5 °C to +85 °C, S: -20 °C to +70 °C |  |               |  |   |
| Frequency tolerance          | f <sub>tol</sub>                | G: ±50 × 10 <sup>-6</sup> , H: ±100 × 10 <sup>-6</sup>     |  |               |  |   |
| Current consumption          | I <sub>CC</sub>                 | 80 mA Max.   |  | 85 mA Max.    |  | OE=V <sub>CC</sub> , L HCSL=50 Ω                  |
| Disable current              | I <sub>dis</sub>                | 20 mA Max.   |  | 35 mA Max.    |  | OE=GND  |
| Symmetry                     | SYM                             | 45 % to 55 %   |  |               |  | at outputs crossing point                         |
| Output Voltage               | V <sub>OH</sub>                 | 0.75 V Typ.  |  |               |  | DC characteristics                                |
|                              | V <sub>OL</sub>                 | -0.3 V Typ.  |  |               |  |   |
| Output load condition (HCSL) | L HCSL                          | 50 Ω   |  |               |  | Terminated to GND                                 |
| Input voltage                | V <sub>IH</sub>                 | 70 % V <sub>CC</sub> Min.                                  |  |               |  | OE terminal                                       |
|                              | V <sub>IL</sub>                 | 30 % V <sub>CC</sub> Max.                                  |  |               |  |   |
| Rise time / Fall time        | t <sub>r</sub> / t <sub>f</sub> | 500 ps Max.  |  |               |  | Between 0.175 V and 0.525 V of output             |
| Start-up time                | t <sub>str</sub>                | 10 ms Max.   |  |               |  | Time at minimum supply voltage to be 0 s          |
| Phase Jitter                 | t <sub>pj</sub>                 | 0.8 ps Max.  |  |               |  | fo < 100 MHz                                      |
|                              |                                 | 0.5 ps Max.  |  |               |  | 100 MHz ≤ fo < 200 MHz                            |
|                              |                                 | 0.3 ps Max.  |  |               |  | 200 MHz ≤ fo                                      |
| Frequency aging *2           | f <sub>aging</sub>              | ± 10 × 10 <sup>-6</sup> / year Max.                        |  |               |  | +25 °C, First year, V <sub>CC</sub> =2.5 V, 3.3 V |

Product Name EG-2121 CA 250.00000MHz P G P A

(Standard form)

- ① Model    ② Package type    ③ Frequency  
 ④ Output/Symmetry    ⑤ Frequency tolerance    ⑥ Operating temperature  
 ⑦ Frequency aging (A\*1: Frequency tolerance include aging, N\*2: Frequency tolerance exclude aging)

\*1 This includes initial frequency tolerance, temperature variation, supply voltage change, reflow drift, and aging(+25 °C, 10 years).

\*2 This includes initial frequency tolerance, temperature variation, supply voltage change, and reflow drift(except aging).

(⑤⑥⑦): GRA, GSA are not available)

(⑤⑥): As for LV-PECL and LVDS output, for 53.125 MHz ≤ fo < 100 MHz only HP is available)

| ④<br>Symbol | Output  | Symmetry   |                             |
|-------------|---------|--|-----------------------------|
|             |         | EG-2121CA  | EG-2102CA                   |
| P           | LV-PECL | 40 % to 60 % (fo > 350 MHz)<br>45 % to 55 % (fo ≤ 350 MHz) | 45 % to 55 %                |
| D           | LV-PECL | 48 % to 52 % (fo ≤ 175 MHz)                                | 48 % to 52 % (fo ≤ 350 MHz) |
| L           | LVDS    | 40 % to 60 % (fo > 350 MHz)<br>45 % to 55 % (fo ≤ 350 MHz) |                             |
| V           | LVDS    | 48 % to 52 % (fo ≤ 175 MHz)                                |                             |
| H           | HCSL    | 45 % to 55 %   |                             |

| ⑤ Frequency tolerance |                         |
|-----------------------|-------------------------|
| G                     | ±50 × 10 <sup>-6</sup>  |
| H                     | ±100 × 10 <sup>-6</sup> |

| ⑥ Operating temperature |                  |
|-------------------------|------------------|
| P                       | 0 °C to +70 °C   |
| R                       | -5 °C to +85 °C  |
| S                       | -20 °C to +70 °C |

Table 2 Jitter

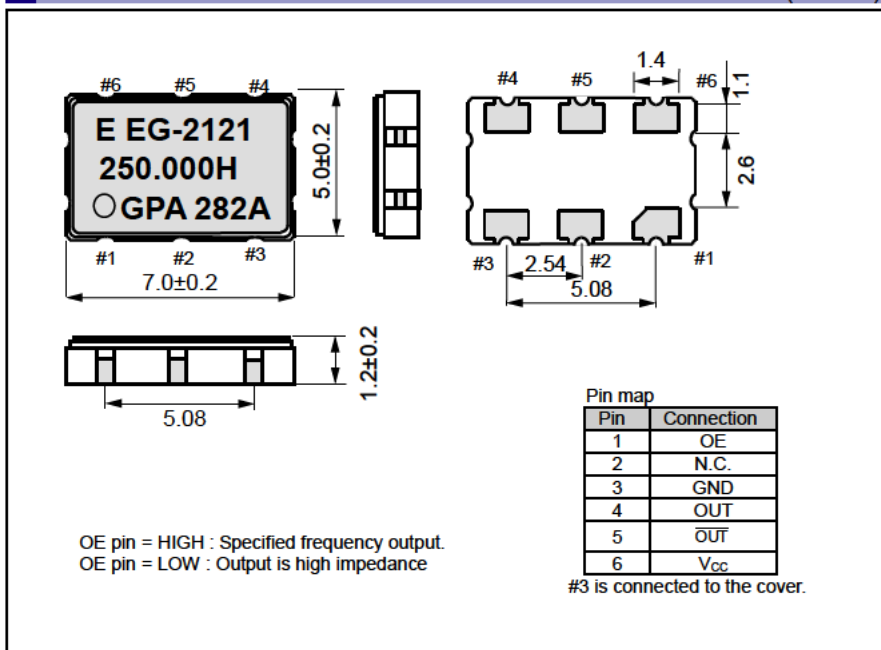
| Item     | Symbol           | Specifications | Remarks                                    |
|----------|------------------|----------------|--|
| Jitter * | t <sub>DJ</sub>  | 0.2 ps Typ.    | Deterministic Jitter                       |
|          | t <sub>RJ</sub>  | 3 ps Typ.      | Random Jitter                              |
|          | t <sub>RMS</sub> | 3 ps Typ.      | σ (RMS of total distribution)              |
|          | t <sub>p-p</sub> | 25 ps Typ.     | Peak to Peak                               |
|          | t <sub>acc</sub> | 4 ps Typ.      | Accumulated Jitter(σ) n=2 to 50 000 cycles |

\* Tested using a DTS-2075 Digital timing system made by WAVECREST with jitter analysis software VISI6.    : Differential LV-PECL, LVDS output

\* Based on SIA-3100C signal integrity analyzer made from WAVECREST.    : HCSL output

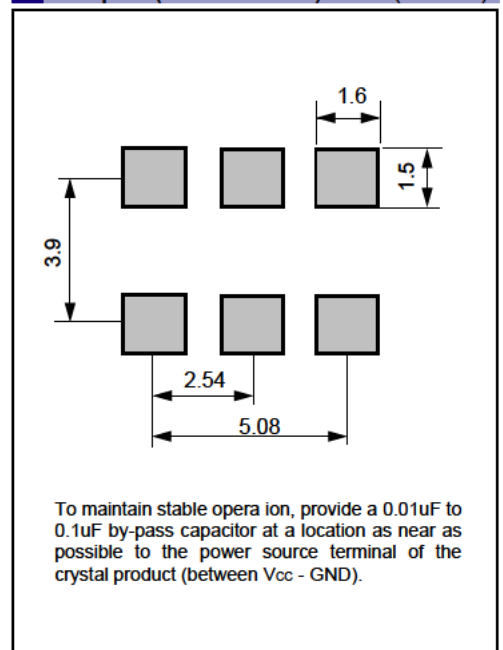
External dimensions

(Unit:mm)



Footprint (Recommended)

(Unit:mm)



## PROMOTION OF ENVIRONMENTAL MANAGEMENT SYSTEM CONFORMING TO INTERNATIONAL STANDARDS

At Seiko Epson, all environmental initiatives operate under the Plan-Do-Check-Action (PDCA) cycle designed to achieve continuous improvements. The environmental management system (EMS) operates under the ISO 14001 environmental management standard.

All of our major manufacturing and non-manufacturing sites, in Japan and overseas, completed the acquisition of ISO 14001 certification.

ISO 14000 is an international standard for environmental management that was established by the International Standards Organization in 1996 against the background of growing concern regarding global warming, destruction of the ozone layer, and global deforestation.

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In order provide high quality and reliable products and services than meet customer needs, Seiko Epson made early efforts towards obtaining ISO9000 series certification and has acquired ISO9001 for all business establishments in Japan and abroad. We have also acquired IATF 16949 certification that is requested strongly by major automotive manufacturers as standard.

IATF 16949 is the international standard that added the sector-specific supplemental requirements for automotive industry based on ISO9001.

### ► Explanation of the mark that are using it for the catalog

|   |   |
|---|---|
|  | ► Pb free.  |
|  | ► Complies with EU RoHS directive.<br>*About the products without the Pb-free mark.<br>Contains Pb in products exempted by EU RoHS directive.<br>(Contains Pb in sealing glass, high melting temperature type solder or other.) |
|  | ► Designed for automotive applications such as Car Multimedia, Body Electronics, Remote Keyless Entry etc.  |
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