IEEE 1394a-2000 CONSUMER ELECTRONICS SOLUTION
Data Sheet Extract, Rev 1.2

FEATURES

- IEEE 1394 Features
  - Integrated 400/200/100-Mbps 2-Port/3-Port PHY
  - Compliant to IEEE Std 1394-1995 and IEEE Std 1394a-2000
  - Supports Bus Manager Functions and Automatic 1394 Self-ID Verification
  - Separate Asynchronous ACK Buffers Decrease ACK-Tracking Burden on External CPU
- DTCP and AES Encryption Support for MPEG-DVB and DSS(TSB43EA42/43 and TSB43EC42/43 Only)
  - DTCP Encryption Support on IEEE Std 1394 Bus
  - AES128 Encryption Support on HSDI Path (TSB43EC42/43 Only)
  - Support for up to Two Encrypted/Decrypted Streams at One Time
  - Full or Restricted AKE Performed With Hardware Assist
  - Secure Loading of DTCP and AES128 Information Using External CPU Interface
  - Localization Support Compliant With DTCP Draft Revision 1.51
- Video Interfaces
  - Two Configurable High-Speed Data Ports for Video Data
    - One Port Configurable As Parallel Or Serial
    - One Port Serial Only
  - Pass-Through Modes for HSDI0 and HSDI1
  - Packet Insertion – Two Insertion Buffers per HSDI for PAT, PMT, SIT, and DIT Packets
  - PID Filtering (32 PID Filters per HSDI Port)
- External CPU Interfaces
  - Motorola 68K-Style 16-Bit Asynchronous Interface
  - SRAM-Like 16-Bit Asynchronous Interface
  - PCI Interface (33 MHz) Compliant to PCI Specification Version 3.0 (Supports PCI Slave and Master Function)
- DMA
  - Higher Asynchronous Throughput With DMA Hardware Enhancements (Available in PCI Mode Only)
  - Internal DMA Controller – Asynchronous, Asynchronous Stream TX/RX
    - General DMA
    - Auto Response DMA for SBP2 Transactions
- Data Buffers
  - 2 x 4K-Byte Isochronous Buffers for Video Data
  - 2 x 2K-Byte Asynchronous/Asynchronous Stream Transmit Buffers
  - 2 x 2K-Byte Asynchronous/Asynchronous Stream Receive Buffers
  - 1 x 1K-Byte Self-ID Buffer
  - Insertion Buffers for MPEG-DVB/DSS Packet Insertion
  - Programmable Data/Space Available Indicators for Buffer Flow Control

- **Hardware Packet Formatting Standards**
  - **IEC61883-1 (General)**
  - **IEC61883-2 (SD-DVCR)**
  - **IEC61883-4 (MPEG2-TS)**
  - **IEC61883-7 (ITU-R BO.1294 System B) – DSS**
  - **Generic 61883 Mode**
  - **Asynchronous Packets**
  - **Asynchronous Streams**
  - **PHY Packets (Including Self-IDs)**
  - **MPEG4 Supported Under IEC61883-4 (No New Requirement for MPEG4 Over IEEE Std 1394)**
- **Additional Features**
  - **JTAG Interface to Support Post-Assembly Scan of Device I/O – Boundary Scan**
  - **Unique "Binding" Method Protects Sensitive Data on the Circuit Board Traces at the External CPU Interface**
  - **Unique "EMI-AES Binding" Method Prevents Protected Data From Being Transmitted in the Clear**

DESCRIPTION

The TSB43Ex42/43 is high-performance consumer electronics IEEE 1394 link layer and integrated physical layer devices designed for digitally interfacing advanced video consumer electronics applications. It supports formatting and transmission of IEC61883 data, including IEC61883-1 (general), IEC61883-2 (SD-DVCR), IEC61883-4 (MPEG2-TS), and IEC61883-7 (ITU-R BO.1294 SystemB-DSS). The TSB43Ex42/43 also supports standard IEEE 1394 data types, such as asynchronous, asynchronous streams, and PHY packets.

The TSB43EAxx/ECxx version incorporates DTCP (M6) baseline per the DTLA (5C) specification to support transmit and receive of up to two MPEG2 transport streams with encryption and decryption. The TSB43EAxx/ECxx version also includes hardware acceleration for content key generation.

The TSB43EBxx series are identical to the TSB43EAxx/ECxx series without implementation of the encryption/decryption features. The TSB43EB42/43 devices allow customers that do not require the encryption/decryption features to incorporate the TSB43Ex42/43 function without becoming DTLA licensees.

The TSB43Ex42/43 features an integrated 2-port/3-port PHY. The PHY operates at 100 Mbps, 200 Mbps, or 400 Mbps. They follow all requirements as stated in the IEEE 1394-1995 and IEEE 1394a-2000 standards.

NOTE

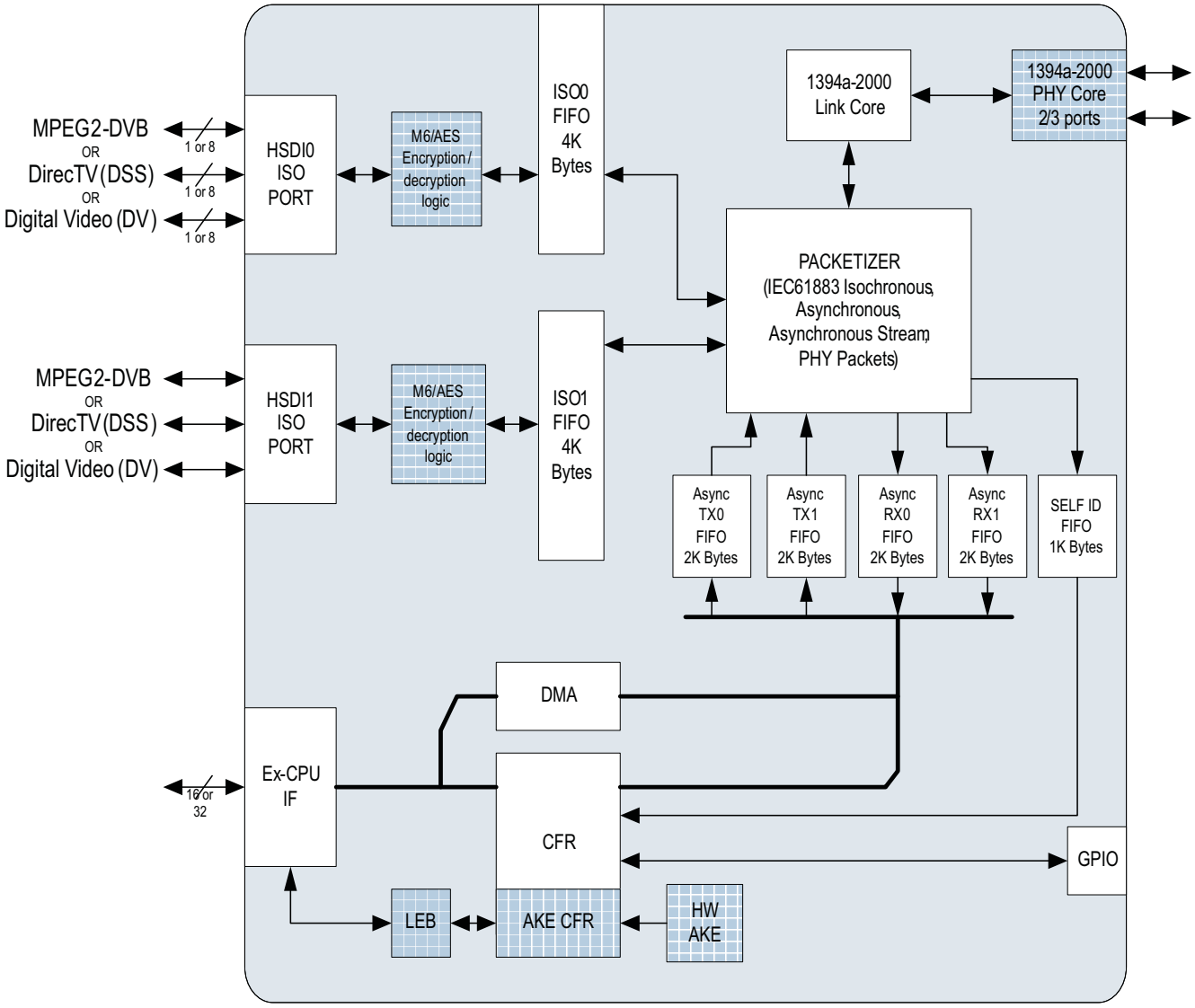
Designing with this device may require extensive support. Before incorporating this device into a design, customers should contact TI or an Authorized TI Distributor.

ORDERING INFORMATION(1)(2)

ORDERING NUMBER	AVAILABILITY	NUMBER OF PHY PORTS	5C/Non-5C	VOLTAGE	PACKAGE	PACKAGE TYPE(3)
TSB43EA42	Available	2	5C only	3.3 V/1.5 V	BGA 144	ZGU
TSB43EB42	Available	2	Non-5C	3.3 V/1.5 V	BGA 144	ZGU
TSB43EC42	Available	2	5C + AES	3.3 V/1.5 V	BGA 144	ZGU
TSB43EB43	To be released	3	Non-5C	3.3 V/1.5 V	BGA 144	ZGU
TSB43EA43	To be released	3	5C only	3.3 V/1.5 V	BGA 144	ZGU
TSB43EC43	To be released	3	5C + AES	3.3 V/1.5 V	BGA 144	ZGU

(1) The devices in the shaded rows are available for order. Other devices are scheduled to be released.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(3) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

BLOCK DIAGRAM



NOTE: Blocks with checked/shaded pattern are available only in selected versions of the device.

DISCLAIMER

Any operations not described by this data manual are undefined. TI is not responsible for the results if the user operates TSB43Ex42/43 in a manner not described by this document.

Operating Voltage(1)

		MIN	MAX	UNIT
Operating voltage	Nominal voltage = 1.5 V	1.35	1.65	V
	Nominal voltage = 3.3 V	3	3.6	V

(1) I/Os are not 5-V tolerant (including PCI interface)

Operating Temperature

		MIN	MAX	UNIT
Operating ambient temperature	Commercial	0	70	°C
	Industrial (To be released)	-40	85	°C
Storage temperature		-65	150	°C

APPLICATION INFORMATION

In an HDTV application (see Figure 1), the TSB43EC42/43 receives the MPEG2 transport stream, decrypts it using the M6 cipher, and outputs it to the application over the HSDI port AES encrypted. The MPEG2 demux and decode device separates the audio and video streams, decodes them, and outputs the 2-channel audio to an audio DAC for listening and the video to an NTSC/PAL encoder for display.

The HDTV receives on-screen display (OSD) information from the video source, such as a set-top box, using the EIA775 standard. The system processor receives the OSD data through the TSB43EC42/43 asynchronous receive buffer. The system graphics controller controls the OSD and mixes it with the video data for display.

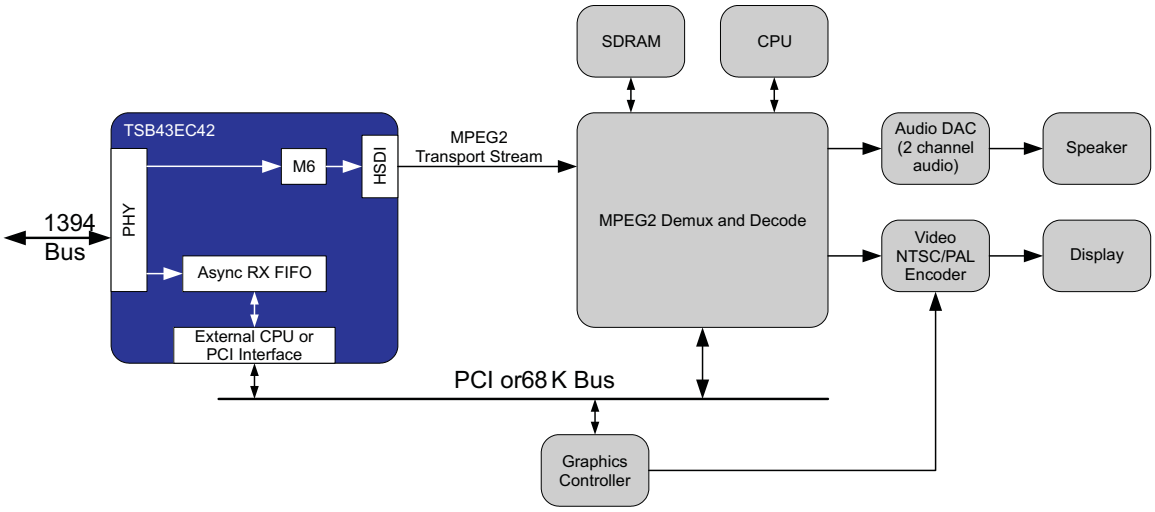


Figure 1. TSB43EC42/43 in HDTV Application

In a set-top box application (see Figure 2), the set-top box receives the MPEG2 transport stream from either satellite or cable sources. The MPEG2 transport stream is input to the TSB43EC42/43 HSDI port in AES encrypted format. The TSB43EC42/43 decrypts the packets received over the HSDI port, performs any PID filtering or packet insertion, encrypts the stream using M6 cipher, and transmits the stream over IEEE 1394.

The set-top box also creates on screen display (OSD) graphics to transmit to the sink device. The system inputs the OSD data to the TSB43EC42/43 asynchronous transmit buffer. The TSB43EC42/43 transmits the OSD using asynchronous packets to the sink device.

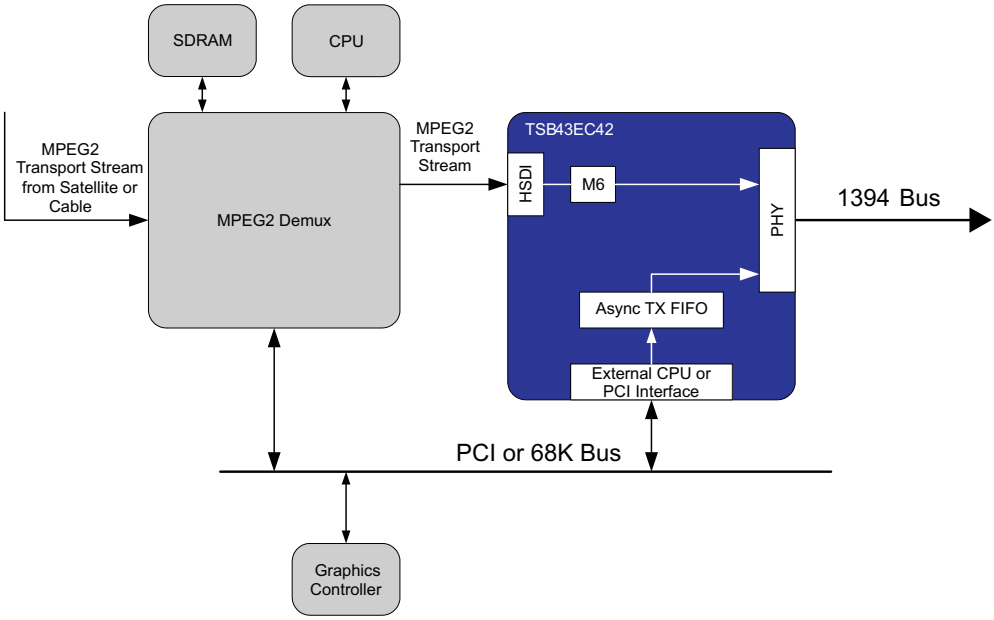


Figure 2. TSB43EC42/43 in STB Application

REVISION HISTORY

Version	Date	Notes
1.0 - Released	Apr-08	Initial release
1.1	Oct-08	Corrections in device name references. Updated availability status of TSB43EC42 in section 4.2 Packet size/ordering information. Updated 4.4 operating temperature section
1.2	Jan-10	Updated availability status of TSB43EA42 in Ordering Information.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSB43EA42ZGU	LIFEBUY	BGA MICROSTAR	ZGU	144	160	RoHS & Green	SNAGCU	Level-3-260C-168 HR	0 to 70	TSB43EA42	
TSB43EB42ZGU	LIFEBUY	BGA MICROSTAR	ZGU	144	126	RoHS & Green	SNAGCU	Level-3-260C-168 HR	0 to 70	TSB43EB42	
TSB43EC42ZGU	LIFEBUY	BGA MICROSTAR	ZGU	144	160	RoHS & Green	SNAGCU	Level-3-260C-168 HR	0 to 70	TSB43EC42	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

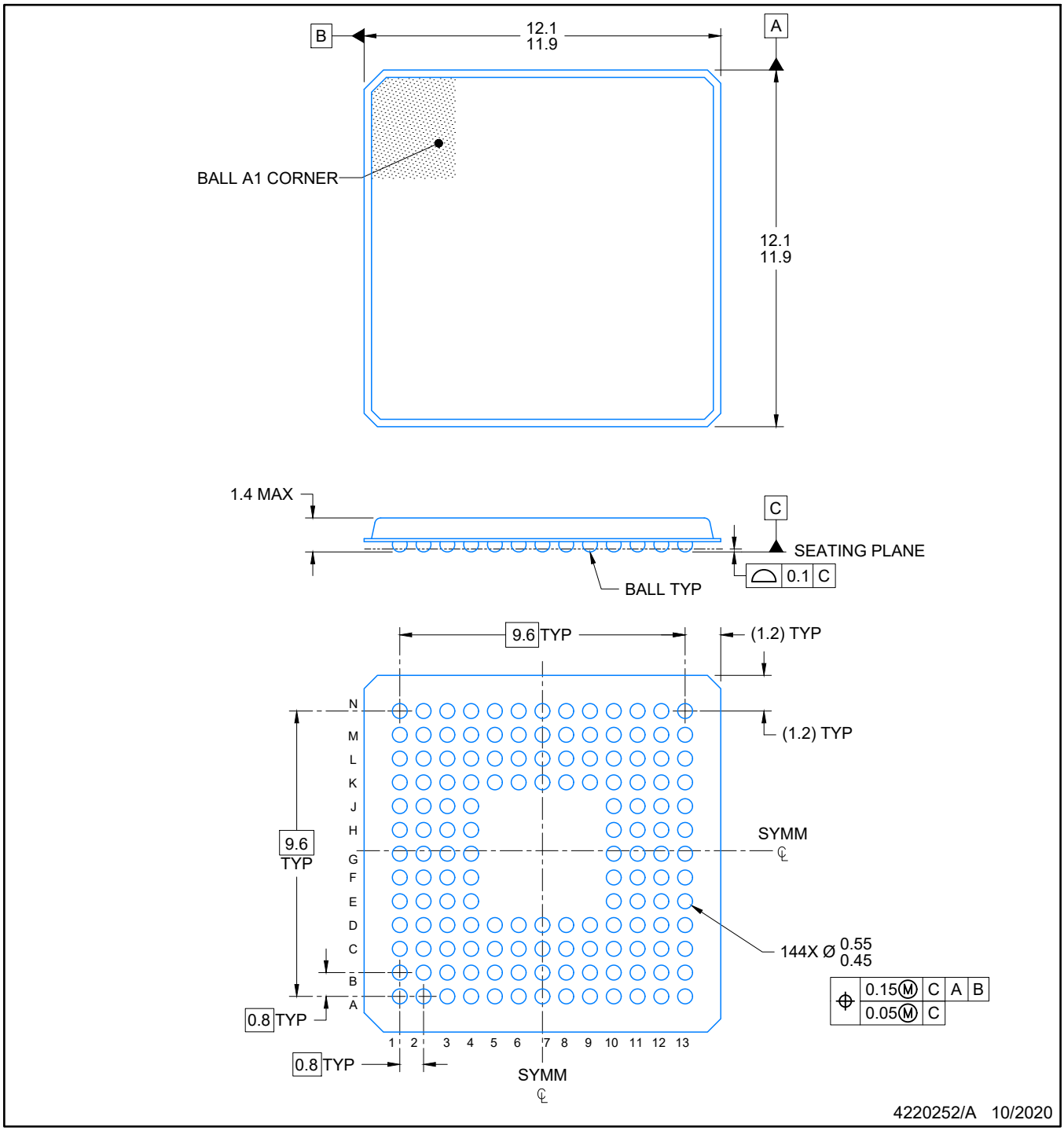
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

ZGU0144A

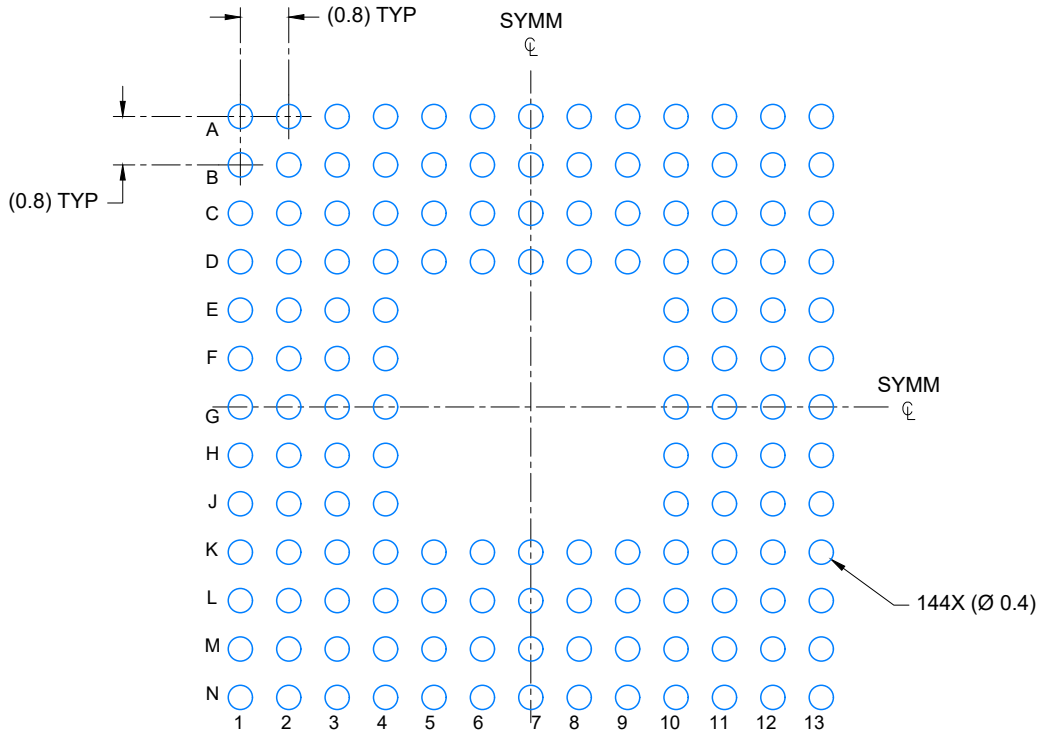
UBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY

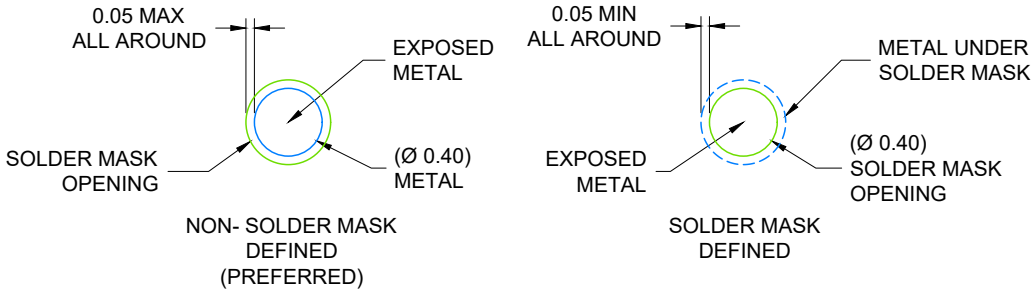


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This is a Pb-Free ball design.



LAND PATTERN EXAMPLE
SCALE: 8X



SOLDER MASK DETAILS
NOT TO SCALE

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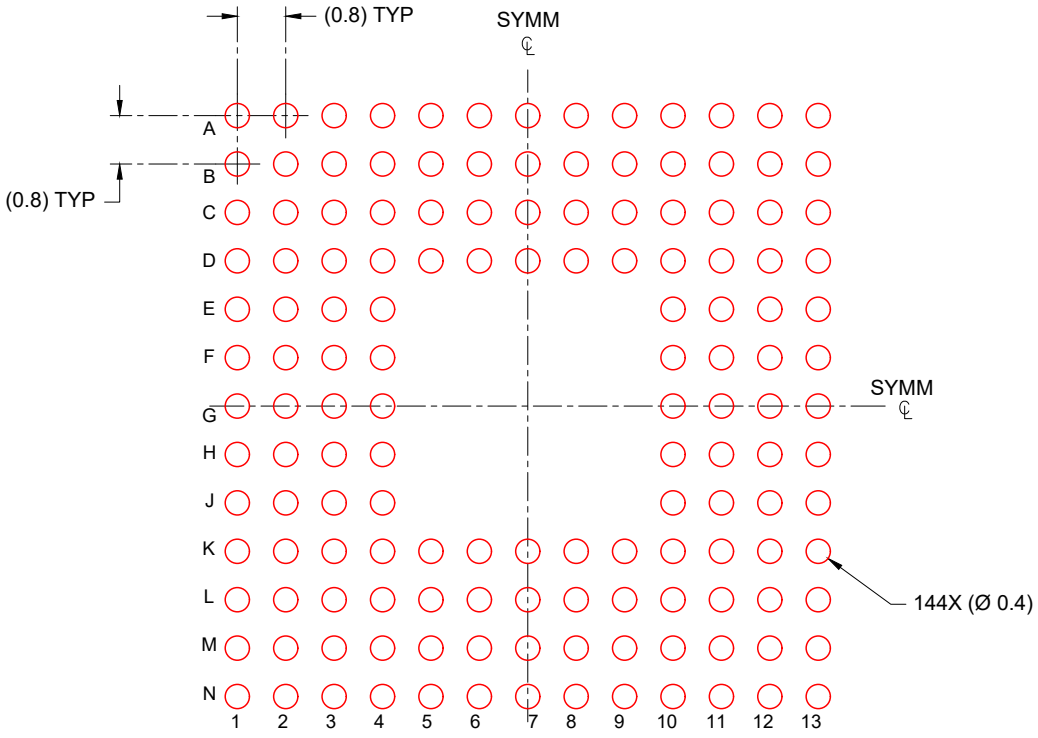
NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.

EXAMPLE STENCIL DESIGN

UBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.150 mm THICK STENCIL
SCALE: 8X

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NOTES: (continued)

5. For alternate stencil design recommendations see IPC-7525 or board assembly site preference.

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