

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

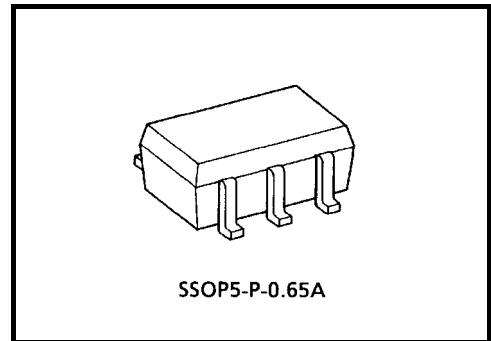
TC7SBL66CFU, TC7SBL384CFU

Low Voltage / Low Capacitance Single Bus Switch

The TC7SBL66C and TC7SBL384C are a Low Voltage / Low Capacitance CMOS single Bus Switch. The low On-resistance of the switch allows connections to be made with minimal propagation delay time.

The TC7SBL66C requires the output enable (OE) input to be set low to place the output into the high impedance state, whereas the TC7SBL384C requires the output enable (\overline{OE}) input to be set high to place the output into the high impedance.

All inputs are equipped with protection circuits against static discharge.



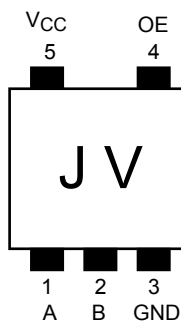
Weight: 0.006 g (typ.)

Features

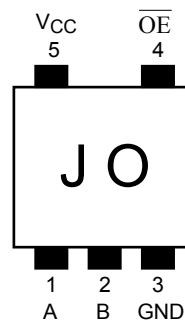
- Operating voltage : $V_{CC} = 1.65$ to 3.6 V
- On-capacitance : $C_{I/O} = 7$ pF Switch On (typ.)@ $V_{CC} = 3$ V
- On-resistance : $R_{ON} = 5.5 \Omega$ (typ.) @ $V_{CC} = 3$ V, $V_{I/O} = 0$ V
- ESD performance : Machine model $\geq \pm 200$ V
Human body model $\geq \pm 2000$ V
- Power-down protection for inputs (OE and \overline{OE} , I/O)
- Package : USV

Pin Assignment (top view)

TC7SBL66CFU



TC7SBL384CFU



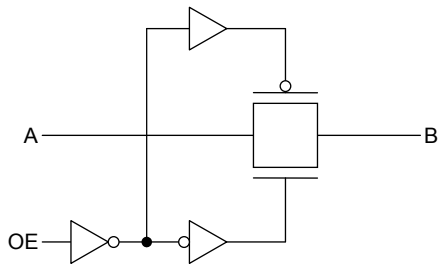
Start of commercial production
2008-06

Truth Table

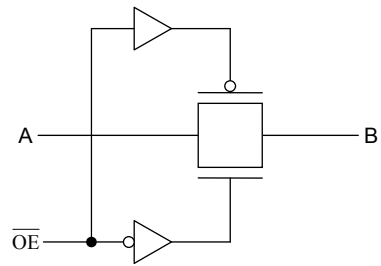
Inputs (66)	Inputs (384)	Function
OE	$\overline{\text{OE}}$	
H	L	A port = B port
L	H	Disconnect

System Diagram

TC7SBL66CFU



TC7SBL384CFU



Absolute Maximum Ratings (Note)

Characteristic	Symbol	Rating	Unit	
Power supply range	V_{CC}	-0.5 to 4.6	V	
Control pin input voltage (\overline{OE} , OE)	V_{IN}	-0.5 to 4.6	V	
Switch terminal I/O voltage	$V_{CC} = 0\text{ V}$ or Switch = Off	V_S	-0.5 to 4.6	V
	Switch = On	V_S	-0.5 to $V_{CC}+0.5$	
Clump diode current	I_{IK}	-50	mA	
Switch I/O current	I_S	50	mA	
Power dissipation	P_D	200	mW	
DC V_{CC} /GND current	I_{CC}/I_{GND}	± 100	mA	
Storage temperature	T_{stg}	-65 to 150	$^{\circ}\text{C}$	

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristic	Symbol	Rating	Unit	
Power supply voltage	V_{CC}	1.65 to 3.6	V	
Control pin input voltage (\overline{OE} , OE)	V_{IN}	0 to 3.6	V	
Switch terminal I/O voltage	$V_{CC} = 0\text{ V}$ or Switch = Off	V_S	0 to 3.6	V
	Switch = On	V_S	0 to V_{CC}	
Operating temperature	T_{opr}	-40 to 85	$^{\circ}\text{C}$	
Input rise and fall time	dt/dv	0 to 10	ns/V	

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics (Ta = -40 to 85°C)

Parameter	Symbol	Test Condition	V _{CC} (V)	Min	Typ. (Note1)	Max	Unit	
Input voltage (OE, \overline{OE})	"H" level	V _{IH}	—	1.65 to 3.6	0.7 × V _{CC}	—	—	V
	"L" level	V _{IL}	—	1.65 to 3.6	—	—	0.3 × V _{CC}	
Input leakage current (OE, \overline{OE})	I _{IN}	V _{IN} = 0 to 3.6 V		1.65 to 3.6	—	—	±1.0	μA
Power-off leakage current	I _{OFF}	OE, \overline{OE} , A, B = 0 to 3.6 V		0	—	—	10	μA
Off-state leakage current (switch off)	I _{SZ}	A, B = 0 to V _{CC} , OE = GND (66), \overline{OE} = V _{CC} (384)		1.65 to 3.6	—	—	±1.0	μA
On resistance (Note2)	R _{ON}	V _{IS} = 0 V, I _{IS} = 30 mA (Note 1)	3.0	—	5.5	10	Ω	
		V _{IS} = 3.0 V, I _{IS} = 30 mA (Note 1)	3.0	—	10	16		
		V _{IS} = 2.4V, I _{IS} = 15 mA (Note 1)	3.0	—	12	18		
		V _{IS} = 0 V, I _{IS} = 24 mA (Note 1)	2.3	—	6	10		
		V _{IS} = 2.3 V, I _{IS} = 24 mA (Note 1)	2.3	—	13	20		
		V _{IS} = 2.0V, I _{IS} = 15 mA (Note 1)	2.3	—	15	21		
		V _{IS} = 0 V, I _{IS} = 4 mA (Note 1)	1.65	—	7	13		
V _{IS} = 1.65 V, I _{IS} = 4 mA (Note 1)	1.65	—	18	27				
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND, I _{OUT} = 0		3.6	—	—	10	μA

Note 1: All typical values are at Ta = 25°C.

Note 2: Measured by the voltage drop between A and B pins at the indicated current through the switch.

On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Characteristics (Ta = -40 to 85°C)

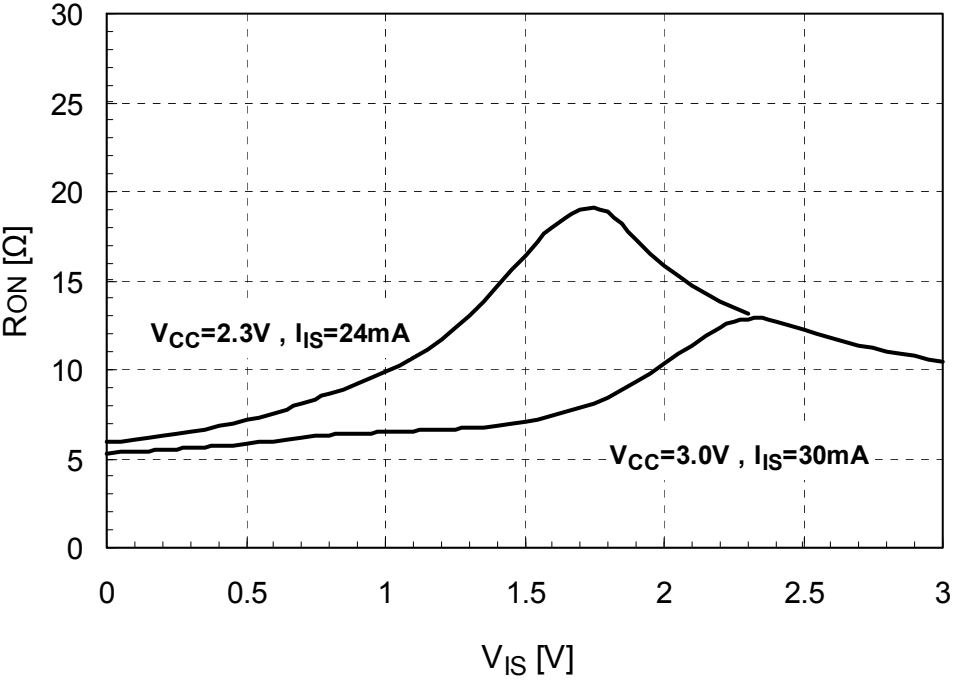
Characteristics	Symbol	Test Condition	V _{CC} (V)	Min	Max	Unit
Output enable time	t _{pZL} t _{pZH}	Figure 1, Figure 2	3.3 ± 0.3	—	6	ns
			2.5 ± 0.2	—	7	
			1.8 ± 0.15	—	11	
Output disable time	t _{pLZ} t _{pHZ}	Figure 1, Figure 2	3.3 ± 0.3	—	6	ns
			2.5 ± 0.2	—	7	
			1.8 ± 0.15	—	11	

Capacitive Characteristics (Ta = 25°C)

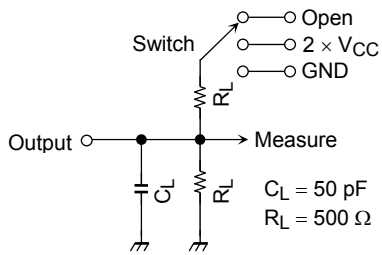
Characteristics	Symbol	Test Condition	V _{CC} (V)	Typ.	Unit
Control pin input capacitance	C _{IN}	V _{IN} = 0 V (Note)	3.0	4	pF
Switch terminal capacitance (Switch Off)	C _{I/O}	OE = GND (66), \overline{OE} = V _{CC} (384), V _{IS} = 0 V (Note)	3.0	3.5	pF
Switch terminal capacitance (Switch On)	C _{I/O}	OE = V _{CC} (66), \overline{OE} = GND (384), V _{IS} = 0 V (Note)	3.0	7	pF

Note: This parameter is guaranteed by design.

R_{ON} - V_{IS} Characteristic (typ.) Ta=25°C



AC Test Circuit



Parameter	Switch
t_{pLZ}, t_{pZL}	$2 \times V_{CC}$
t_{pHZ}, t_{pZH}	GND

Figure 1

AC Waveform

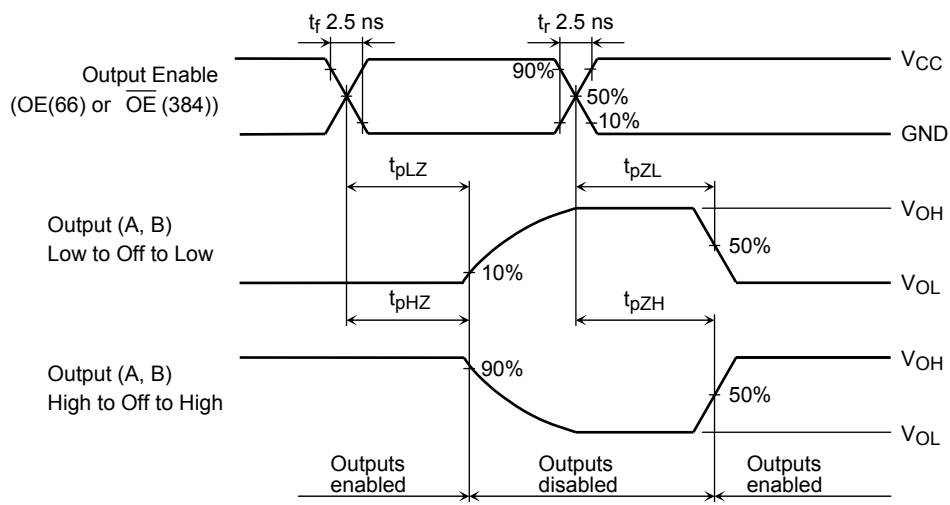


Figure 2 $t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}$

Rise and Fall Times (tr / tf) of the TC7SBL66C, 384C I/O Signals

The tr(out) and tf(out) values of the output signals are affected by the CR time constant of the input, which consists of the switch terminal capacitance (C_{I/O}) and the on-resistance (R_{ON}) of the input.

In practice, the tr(out) and tf(out) values are also affected by the circuit's capacitance and resistance components other than those of the TC7SBL66CFU, 384CFU.

The tr(out) / tf(out) values can be approximated as follows. (Figure 3 shows the test circuit.)

$$tr(out) / tf(out) \text{ (approx)} = -(C_{I/O} + C_L) \cdot (R_{DRIVE} + R_{ON}) \cdot \ln ((V_{OH} - V_{OL}) - V_M) / (V_{OH} - V_{OL})$$

where, R_{DRIVE} is the output impedance of the previous-stage circuit.

Calculation example:

$$tr(out) \text{ (approx)} = -(7 + 15)E-12 \cdot (120 + 5.5) \cdot \ln ((3.0 - 0) - 1.5) / (3.0 - 0) \approx 1.9 \text{ ns}$$

Calculation conditions:

V_{CC} = 3.0 V, C_L = 15 pF, R_{DRIVE} = 120 Ω (output impedance of the previous IC), V_M = 1.5 V (V_{CC} / 2)
 Output voltage of the previous IC = digital (i.e., high-level voltage = V_{CC}; low-level voltage = GND)

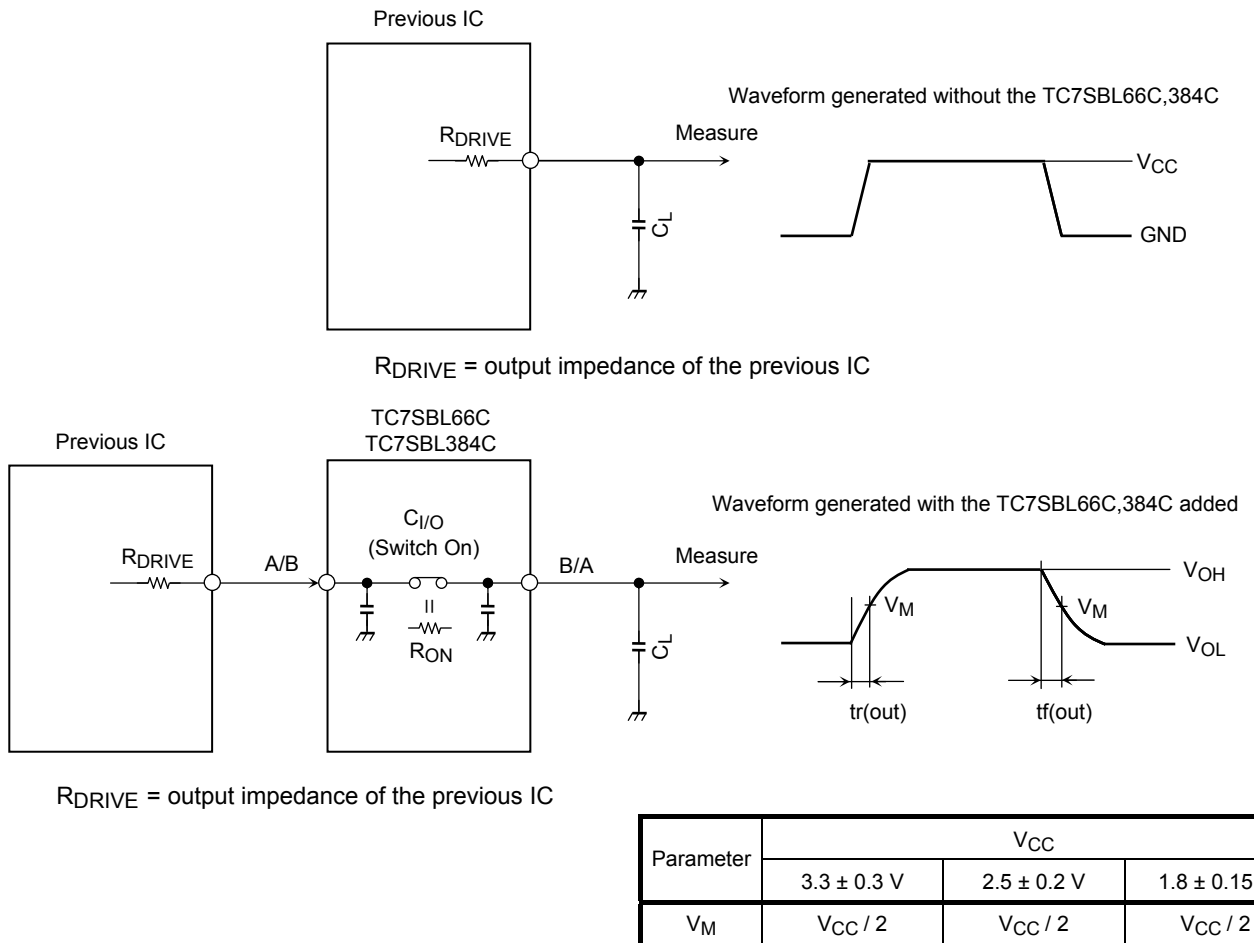
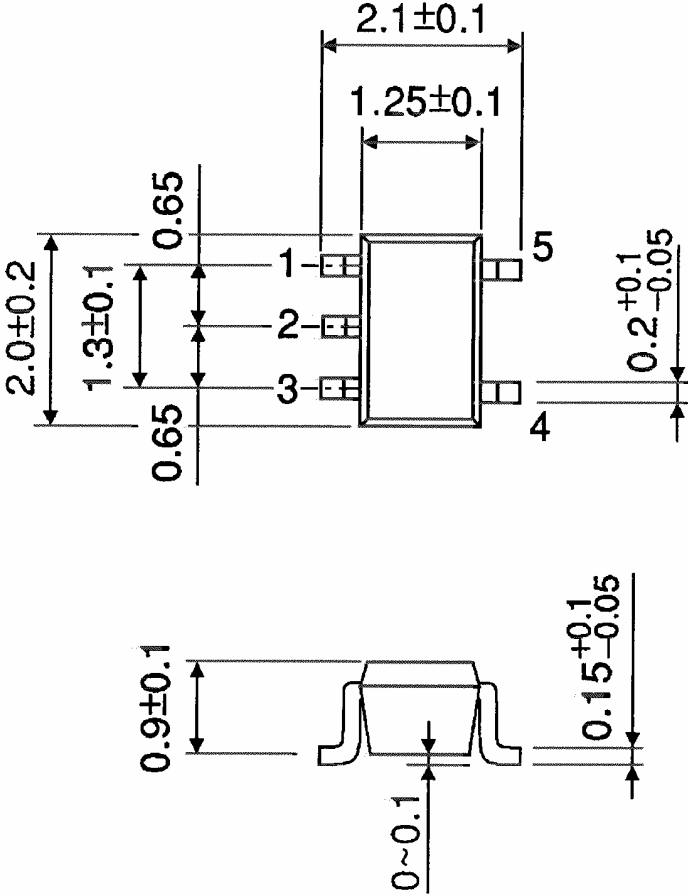


Figure 3 Test Circuit

Package Dimensions

SSOP5-P-0.65A

Unit : mm



Weight: 0.006 g (typ.)

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