HI-5042, HI-5043, HI-5047, HI-5049, HI-5051

CMOS Analog Switches

FN3127
Rev 7.00
June 16, 2016

This family of CMOS analog switches offers low resistance switching performance for analog voltages up to the supply rails and for signal currents up to 80mA. “ON” resistance is low and stays reasonably constant over the full range of operating signal voltage and current. r_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0^oC and 75^oC. r_{ON} is nominally 25Ω for HI-5049 and HI-5051 and 50Ω for HI-5042 through HI-5047.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at 25^oC). This family of switches also features very low power operation (1.5mW at 25^oC).

There are 7 devices in this switch series which are differentiated by type of switch action and value of r_{ON} (see Functional Description Table). The HI-504X and HI-505X series switches can directly replace IH-5040 series devices, and are functionally compatible with the DG180 and DG190 family

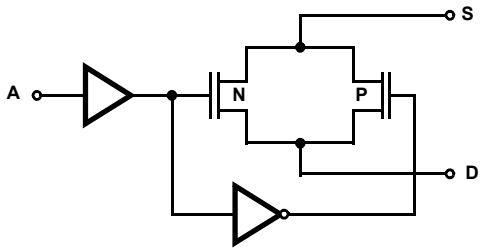
Features

- Wide Analog Signal Range . . . . . ±15V
- Low “ON” Resistance 25Ω
- High Current Capability 80mA
- Break-Before-Make Switching
  - Turn-On Time 370ns
  - Turn-Off Time 280ns
- No Latch-Up
- Input MOS Gates are Protected from Electrostatic Discharge
- DTL, TTL, CMOS, PMOS Compatible
- Pb-Free Available (RoHS Compliant)

Applications

- High Frequency Switching
- Sample and Hold
- Digital Filters
- Operational Amplifier Gain Switching

Functional Diagram



Functional Description

PART NUMBER	TYPE	r_{ON}
HI-5042	SPDT	50Ω
HI-5043	Dual SPDT	50Ω
HI-5047	4PST	50Ω
HI-5049	Dual DPST	25Ω
HI-5051	Dual SPDT	25Ω

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. DWG. #
HI1-5042-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-5043-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-5043-5	0 to 75	16 Ld CERDIP	F16.3
HI3-5043-5	0 to 75	16 Ld PDIP	E16.3
HI3-5043-5Z (See Note)	0 to 75	16 Ld PDIP* (Pb-free)	F16.3
HI9P5043-5	0 to 75	16 Ld SOIC	M16.15
HI9P5043-5Z (See Note)	0 to 75	16 Ld SOIC (Pb-free)	M16.15
HI1-5047-5	0 to 75	16 Ld CERDIP	F16.3
HI1-5049-5	0 to 75	16 Ld CERDIP	F16.3
HI1-5051-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-5051-5	0 to 75	16 Ld CERDIP	F16.3
HI3-5051-5	0 to 75	16 Ld PDIP	E16.3
HI3-5051-5Z **(No longer available, recommended replacement: HI9P5051-9Z** (See Note)	0 to 75	16 Ld PDIP * (Pb-free)	E16.3
HI9P5051-9	-40 to 85	16 Ld SOIC	M16.15
HI9P5051-9Z (See Note)	-40 to 85	16 Ld SOIC (Pb-free)	M16.15

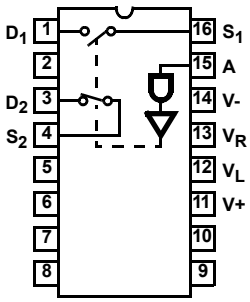
*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

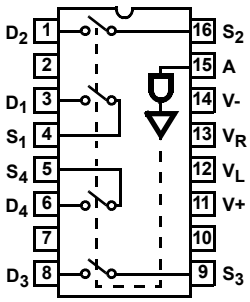
Pinouts (SWITCHES SHOWN FOR LOGIC "0" INPUT)

Single Control

SPDT
HI-5042 (50Ω)



4PST
HI-5047 (50Ω)

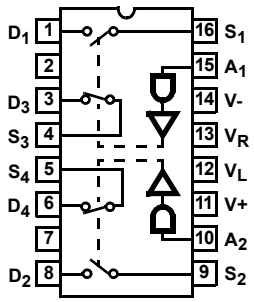


NOTE: Unused pins may be internally connected. Ground all unused pins.

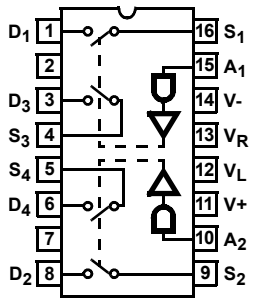
Pinouts (SWITCHES SHOWN FOR LOGIC "0" INPUT)

Dual Control

DUAL SPDT
HI-5043 (50Ω), HI-5051 (25Ω)



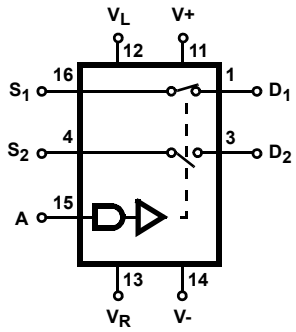
DUAL DPST
HI-5049 (25Ω)



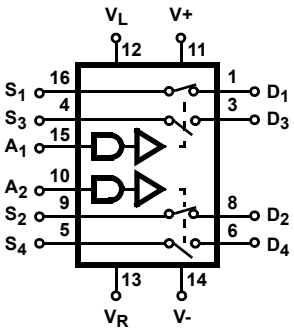
NOTE: Unused pins may be internally connected. Ground all unused pins.

Switch Functions (SWITCHES SHOWN FOR LOGIC “1” INPUT)

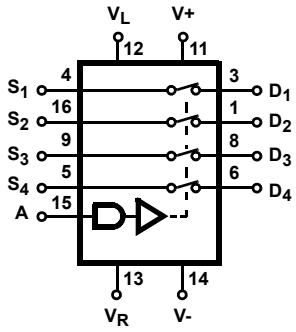
SPDT
HI-5042 (50Ω)



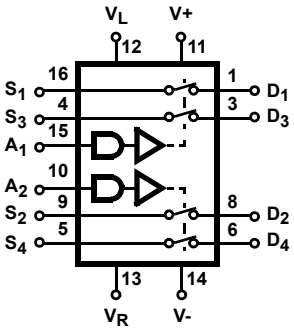
DUAL SPDT
HI-5043 (50Ω)



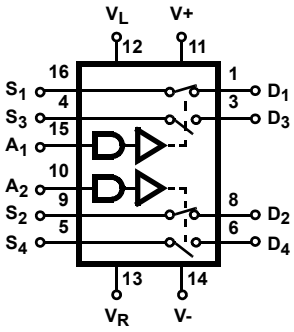
4PST
HI-5047 (50Ω)



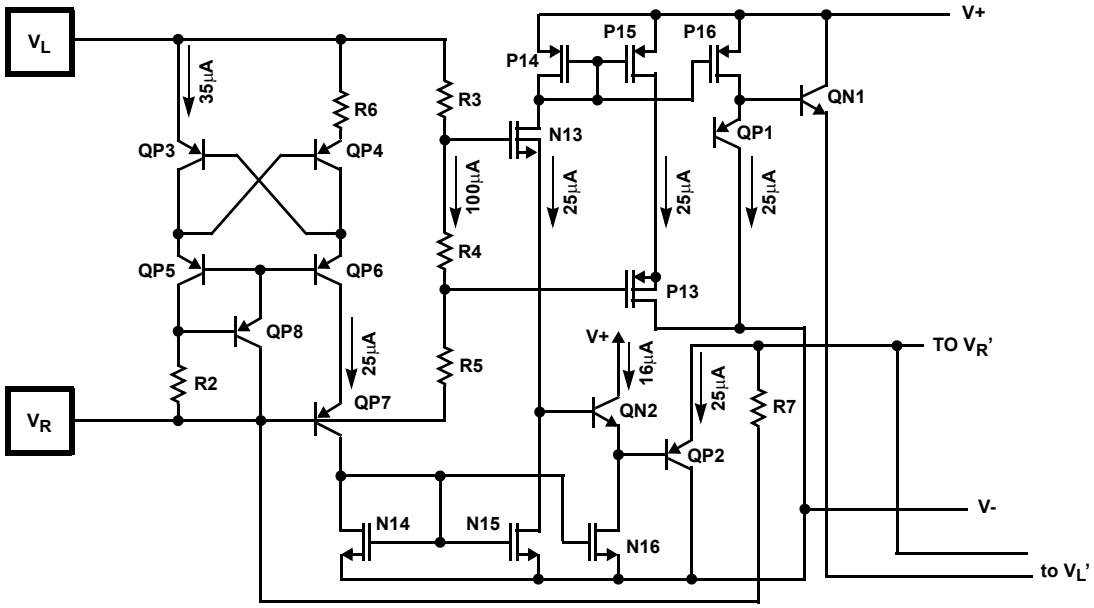
DUAL DPST
HI-5049 (25Ω)



DUAL SPDT
HI-5051 (25Ω)

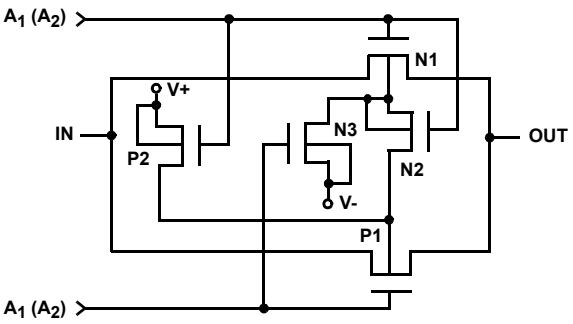


Schematic Diagrams

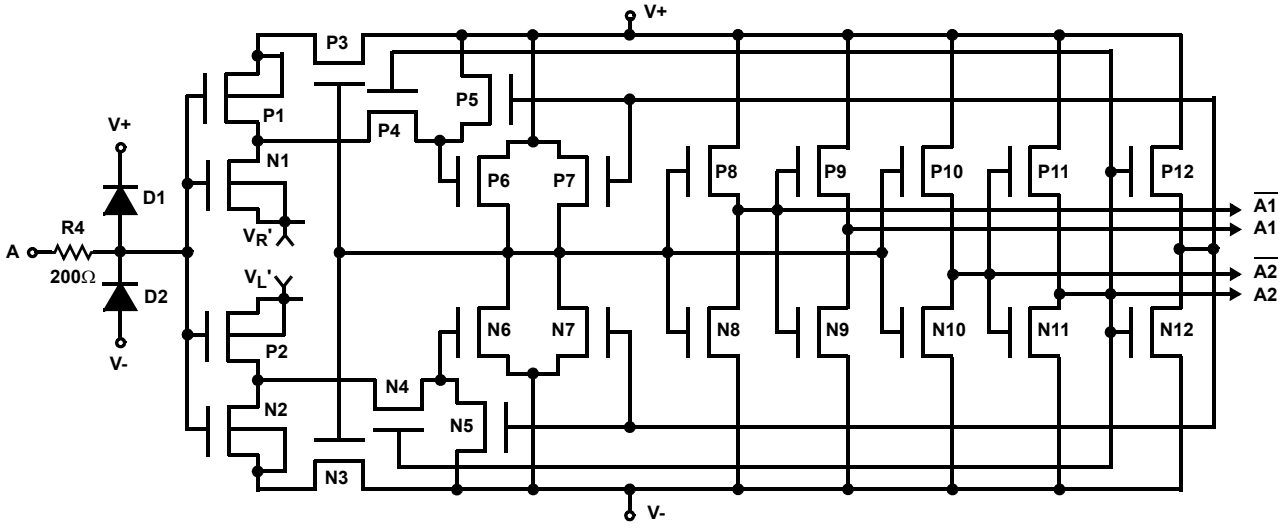


NOTE: Connect V+ to V_L for minimizing power consumption when driving from CMOS circuits.

TTL/CMOS REFERENCE CIRCUIT (NOTE)



SWITCH CELL



NOTE: All N-Channel bodies to V-, all P-Channel bodies to V+ except as shown.

DIGITAL INPUT BUFFER AND LEVEL SHIFTER

Absolute Maximum Ratings

Supply Voltage (V+ to V-). 36V
V_R to Ground . . . . . V+, V-
Digital and Analog Input Voltage . . . . . (V+) +4V to (V-) -4V
Analog Current (S to D) Continuous 30mA
Analog Current (S to D) Peak 80mA

Operating Conditions

Temperature Range
HI-50XX-2. . . . . -55°C to 125°C
HI-50XX-5. . . . . 0°C to 75°C
HI-50XX-9. . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	75	22
SOIC Package	110	N/A
PDIP Package*	90	N/A

Maximum Junction Temperature
Plastic Packages . . . . . 150°C
Ceramic Packages . . . . . 175°C
Maximum Storage Temperature. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = +15V, -15V; V_R = 0V; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = 0.8V, V_L = 5V, Unless Otherwise Specified. For Test Conditions, Consult Performance Characteristics, Unused Pins are Grounded

PARAMETER	TEST CONDITIONS	TEMP (°C)	-2			-5, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC CHARACTERISTICS									
Switch ON Time, t_{ON}	(Note 5)	25	-	370	500	-	370	500	ns
Switch OFF Time, t_{OFF}	(Note 5)	25	-	280	500	-	280	500	ns
Charge Injection, Q	(Note 3)	25	-	5	20	-	5	-	mV
OFF Isolation	(Note 4)	25	75	80	-	-	80	-	dB
Crosstalk	(Note 4)	25	-80	-88	-	-	-88	-	dB
Input Switch Capacitance, $C_{S(OFF)}$		25	-	11	-	-	11	-	pF
Output Switch Capacitance, $C_{D(OFF)}$		25	-	11	-	-	11	-	pF
Output Switch Capacitance, $C_{D(ON)}$		25	-	22	-	-	22	-	pF
Digital Input Capacitance, C_A		25	-	5	-	-	5	-	pF
Drain To Source Capacitance, $C_{DS(OFF)}$		25	-	0.5	-	-	0.5	-	pF
DIGITAL INPUT CHARACTERISTICS									
Input Low Threshold, V_{AL}		Full	-	-	0.8	-	-	0.8	V
Input High Threshold, V_{AH}		Full	2.4	-	-	2.4	-	-	V
Input Leakage Current (High or Low), I_A		Full	-	0.01	1.0	-	0.01	1.0	µA
ANALOG SWITCH CHARACTERISTICS									
Analog Signal Range		Full	-15	-	+15	-15	-	+15	V
ON Resistance, r_{ON}									
HI-5042 to HI-5047	(Note 2)	25	-	50	75	-	50	75	Ω
		Full	-	-	150	-	-	150	Ω
HI-5049, HI-5051	(Note 2)	25	-	25	45	-	25	45	Ω
		Full	-	-	50	-	-	50	Ω
Channel-to-Channel Match, Δr_{ON}									
HI-5042 to HI-5047		25	-	2	10	-	2	10	Ω
HI-5049, HI-5051		25	-	1	5	-	1	5	Ω

Electrical Specifications Supplies = +15V, -15V; V_R = 0V; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = 0.8V, V_L = 5V, Unless Otherwise Specified. For Test Conditions, Consult Performance Characteristics, Unused Pins are Grounded **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (^oC)	-2			-5, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
OFF Input or Output Leakage Current, $I_{S(OFF)} = I_{D(OFF)}$		25	-	0.8	2	-	0.8	2	nA
		Full	-	100	200	-	100	200	nA
ON Leakage Current, $I_{D(ON)}$		25	-	0.01	2	-	0.01	2	nA
		Full	-	2	200	-	2	200	nA
POWER REQUIREMENTS									
Quiescent Power Dissipation, P_D		25	-	1.5	-	-	1.5	-	mW
I+, I-, I_L, I_R		25	-	-	0.2	-	-	0.3	mA
I+, +15V Quiescent Current	(Note 5)	Full	-	-	0.3	-	-	0.5	mA
I-, -15V Quiescent Current	(Note 5)	Full	-	-	0.3	-	-	0.5	mA
I_L, +5V Quiescent Current	(Note 5)	Full	-	-	0.3	-	-	0.5	mA
I_R, Ground Quiescent Current	(Note 5)	Full	-	-	0.3	-	-	0.5	mA

NOTES:

2. $V_{OUT} = \pm 10V$, $I_{OUT} = \mp 1mA$.
3. V_{IN} = 0V, C_L = 10nF.
4. $R_L = 100\Omega$, f = 100kHz, $V_{IN} = 2.0V_{P-P}$, C_L = 5pF.
5. V_{AL} = 0V, V_{AH} = 5V.

Test Circuits and Waveforms

$T_A = 25^oC$, V+ = +15V, V- = -15V, V_L = +5V, V_R = 0V, V_{AH} = 3V and V_{AL} = 0.8V Unless Otherwise Specified

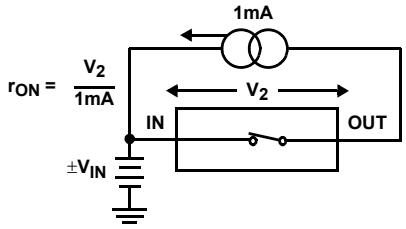


FIGURE 1A. TEST CIRCUIT

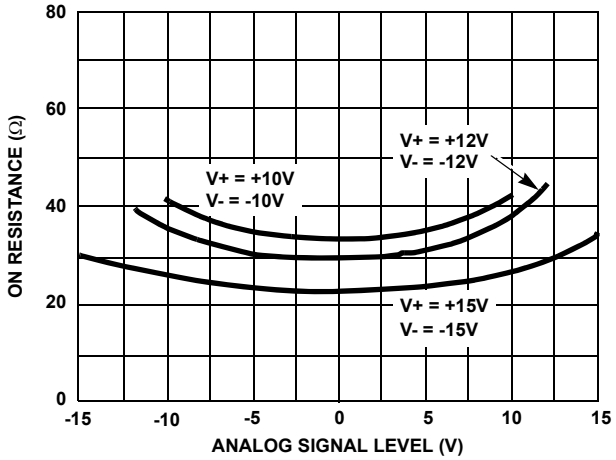


FIGURE 1B. ON RESISTANCE vs ANALOG SIGNAL LEVEL

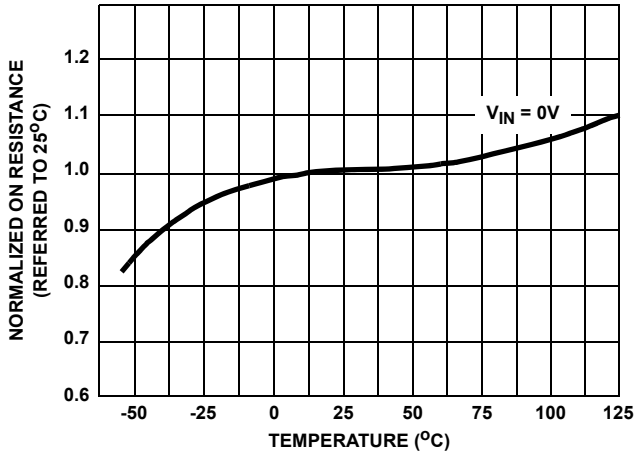


FIGURE 1C. NORMALIZED ON RESISTANCE vs TEMPERATURE

FIGURE 1. ON RESISTANCE

Test Circuits and Waveforms

$T_A = 25^oC$, V+ = +15V, V- = -15V, V_L = +5V, V_R = 0V, V_{AH} = 3V and V_{AL} = 0.8V Unless Otherwise Specified **(Continued)**

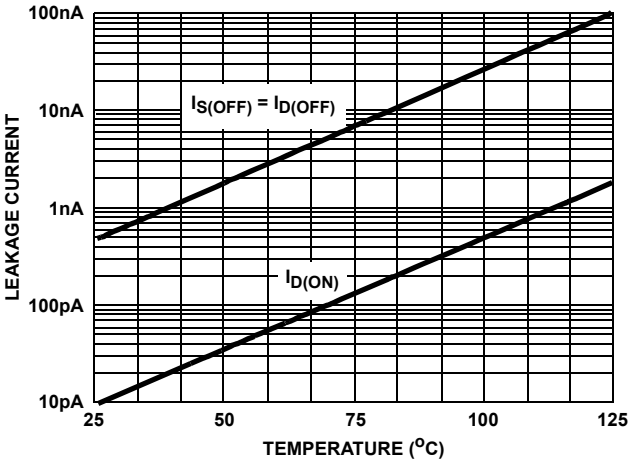


FIGURE 2A. LEAKAGE CURRENTS vs TEMPERATURE

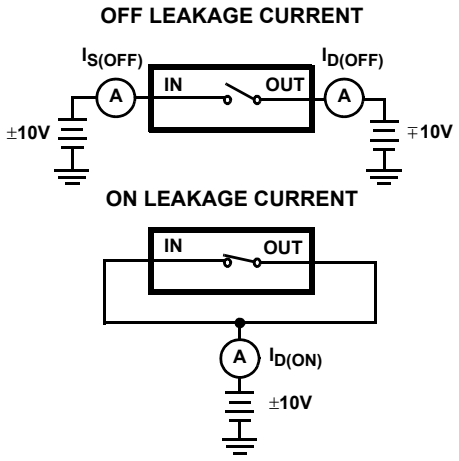


FIGURE 2B. TEST CIRCUITS

FIGURE 2. LEAKAGE CURRENTS

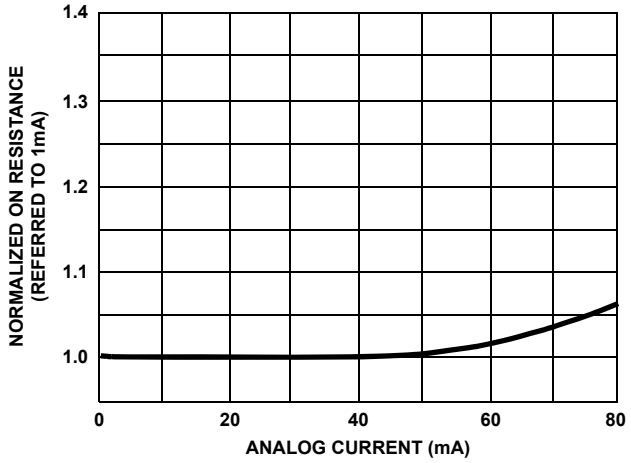


FIGURE 3A. NORMALIZED ON RESISTANCE vs ANALOG CURRENT

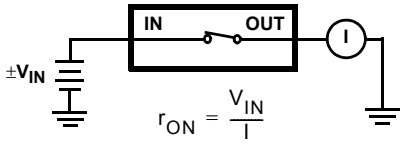


FIGURE 3B. TEST CIRCUIT

FIGURE 3. NORMALIZED ON RESISTANCE

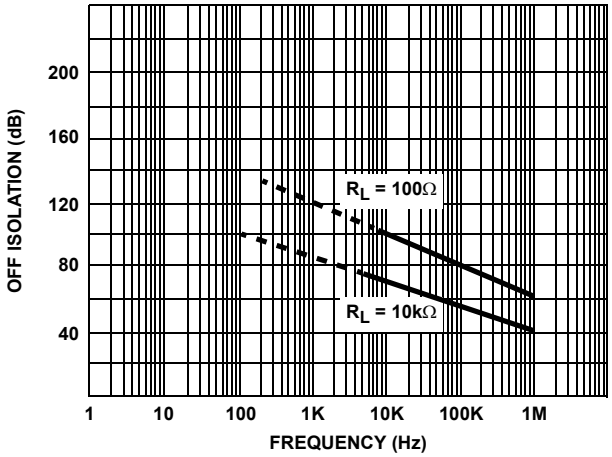


FIGURE 4A. OFF ISOLATION vs FREQUENCY

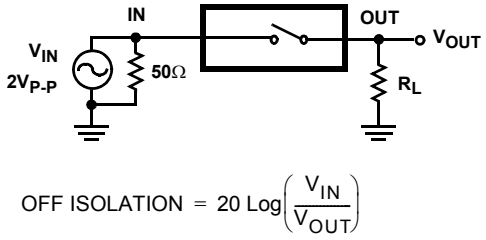


FIGURE 4B. TEST CIRCUIT

FIGURE 4C. OFF ISOLATION

Test Circuits and Waveforms

$T_A = 25^oC$, V+ = +15V, V- = -15V, V_L = +5V, V_R = 0V, V_{AH} = 3V and V_{AL} = 0.8V Unless Otherwise Specified **(Continued)**

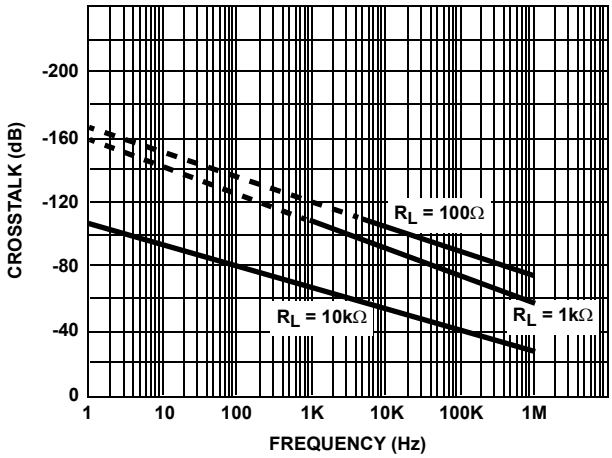
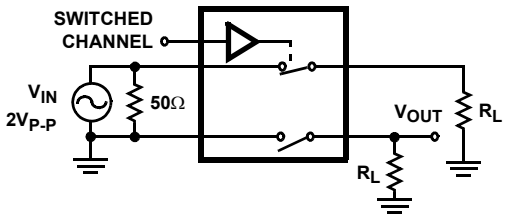


FIGURE 5A. CROSSTALK vs FREQUENCY



$$\text{CROSSTALK} = 20\ \text{Log}\left(\frac{V_{OUT}}{V_{IN}}\right)$$

FIGURE 5B. TEST CIRCUIT

FIGURE 5. CROSSTALK

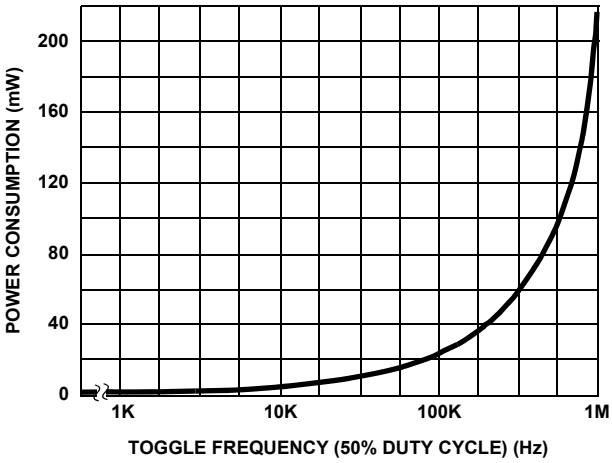


FIGURE 6A. POWER CONSUMPTION vs FREQUENCY

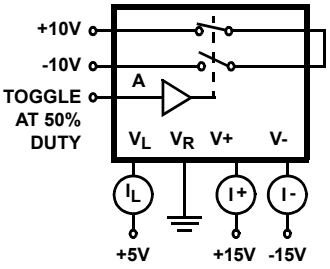


FIGURE 6B. TEST CIRCUIT

FIGURE 6. POWER CONSUMPTION

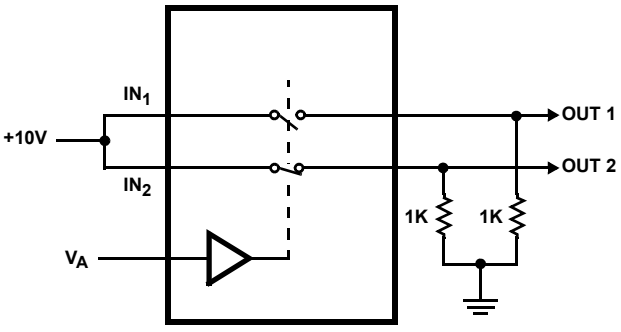


FIGURE 7A. TEST CIRCUIT

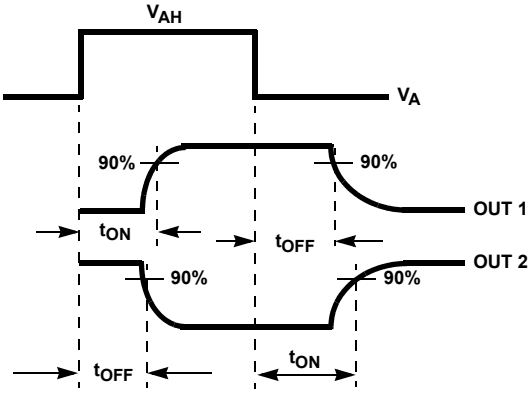
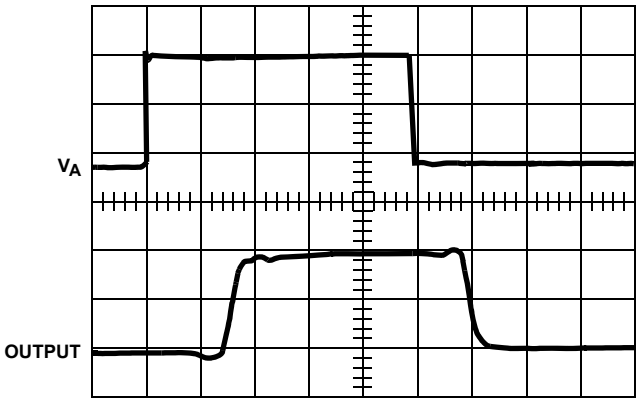


FIGURE 7B. MEASUREMENT POINTS

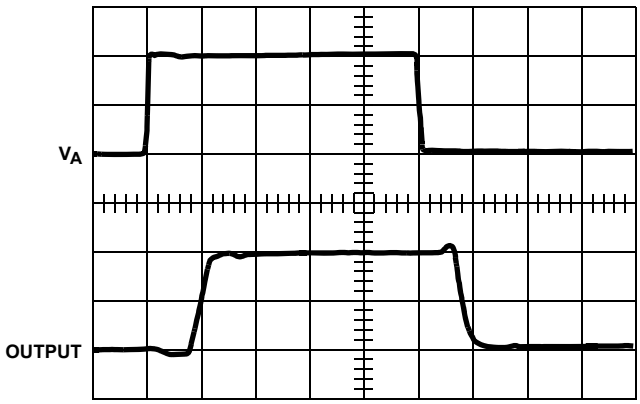
Test Circuits and Waveforms

$T_A = 25^oC$, V+ = +15V, V- = -15V, V_L = +5V, V_R = 0V, V_{AH} = 3V and V_{AL} = 0.8V Unless Otherwise Specified **(Continued)**



V_A = 0V to 5V
Vertical: 2V/Div.
Horizontal: 200ns/Div.

FIGURE 7C. WAVEFORMS WITH TTL COMPATIBLE LOGIC INPUT



V_A = 0V to 10V
Vertical: 5V/Div.
Horizontal: 200ns/Div.

FIGURE 7D. WAVEFORMS WITH CMOS COMPATIBLE LOGIC INPUT

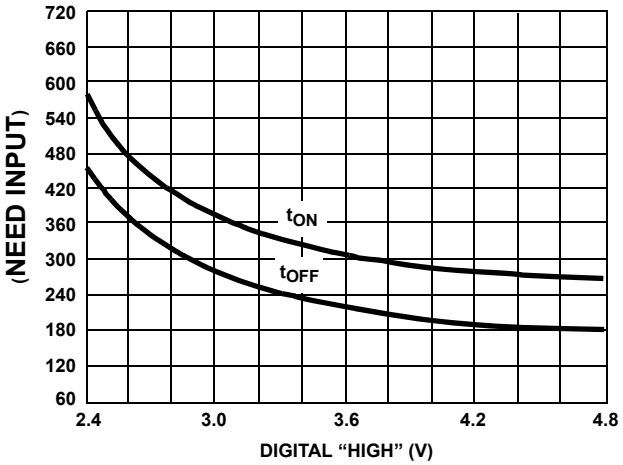


FIGURE 7E. SWITCHING TIMES vs POSITIVE DIGITAL VOLTAGE

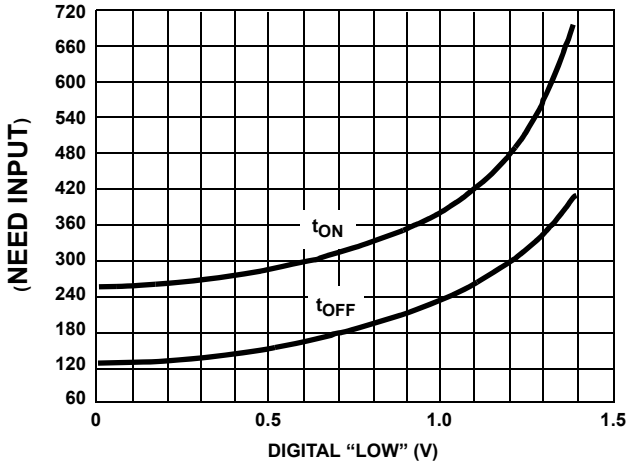


FIGURE 7F. SWITCHING TIMES vs NEGATIVE DIGITAL VOLTAGE

FIGURE 7. SWITCH t_{ON} AND t_{OFF}

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
June 16, 2016	FN3127.7	Updated Ordering Information table on page 2. Added Revision History and About Intersil sections. Updated POD M16.15 to the latest revision changes are as follows: Remove "u" symbol from drawing (overlaps the "a" on Side View). Multiple changes were made to table.

About Intersil

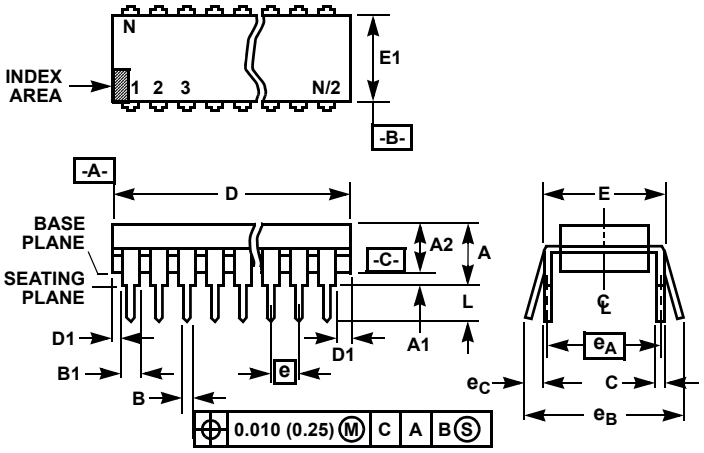
Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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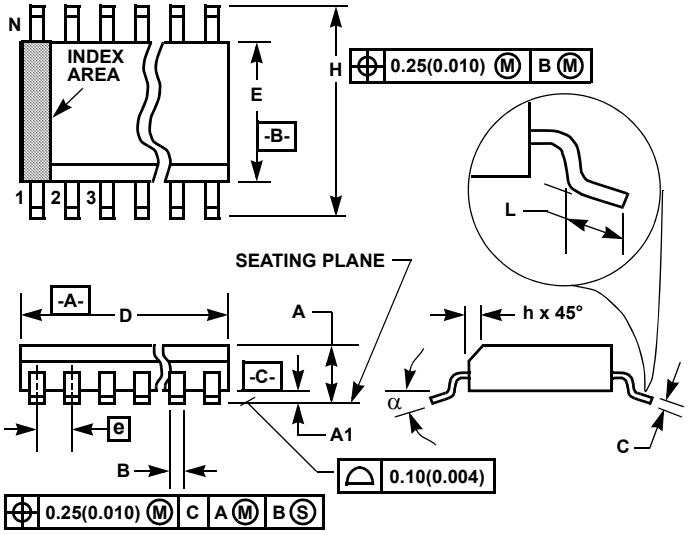
Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

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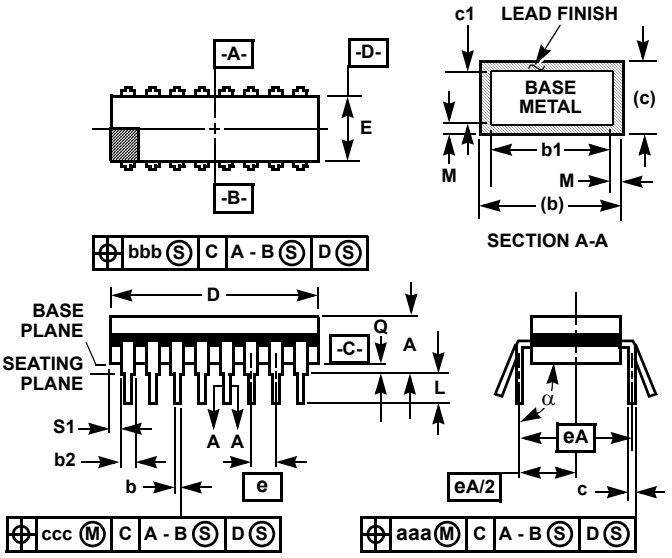
Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

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