Low Skew, 1-to-8 Differential-to-3.3V LVPECL/ECL Fanout Buffer

ICS853S310I

DATA SHEET

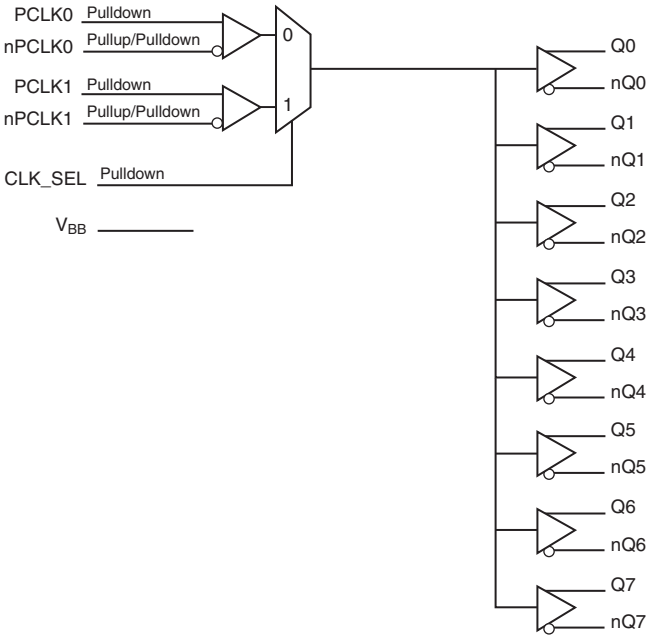
General Description

The ICS853S310I is a low skew, high performance 1-to-8 Differential-to-3.3V LVPECL/ECL Fanout Buffer. The PCLKx, nPCLKx pairs can accept LVPECL, LVDS, CML and SSTL differential input levels. The ICS853S310I is characterized to operate from a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the ICS853S310I ideal for those clock distribution applications demanding well defined performance and repeatability.

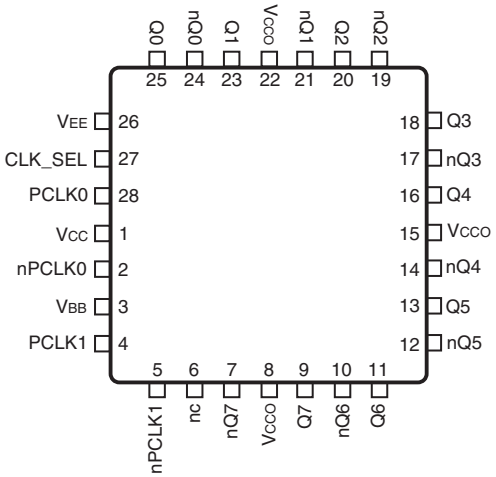
Features

- Eight differential 3.3V LVPECL/ECL outputs
- Two selectable differential input pairs
- PCLKx, nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Maximum output frequency: 2GHz
- Translates any single-ended input signal to 3.3V LVPECL levels with resistor bias on nPCLKx input
- Output skew: 20ps (typical)
- Propagation delay: 825ps (typical)
- Additive phase jitter, RMS: 0.14ps (typical)
- LVPECL mode operating voltage supply range: V_{CC} = 3.0V to 3.8V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3.0V to -3.8V
- -40°C to 85°C ambient operating temperature
- Available lead-free (RoHS 6) package

Block Diagram



Pin Assignment



ICS853S310I

28-Lead PLCC

11.6mm x 11.4mm x 4.1mm package body

V Package

Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{CC}	Power		Positive supply pin.
2	nPCLK0	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{CC}/2 default when left floating.
3	V_{BB}	Output		Bias voltage to be connected for single-ended applications.
4	PCLK1	Input	Pulldown	Non-inverting differential LVPECL clock input.
5	nPCLK1	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{CC}/2 default when left floating.
6	nc	Unused		No connect
7, 9	nQ7, Q7	Output		Differential output pair. LVPECL/ECL interface levels.
8, 15, 22	V_{CCO}	Power		Output supply pins.
10, 11	nQ6, Q6	Output		Differential output pair. LVPECL/ECL interface levels.
12, 13	nQ5, Q5	Output		Differential output pair. LVPECL/ECL interface levels.
14, 16	nQ4, Q4	Output		Differential output pair. LVPECL/ECL interface levels.
17, 18	nQ3, Q3	Output		Differential output pair. LVPECL/ECL interface levels.
19, 20	nQ2, Q2	Output		Differential output pair. LVPECL/ECL interface levels.
21, 23	nQ1, Q1	Output		Differential output pair. LVPECL/ECL interface levels.
24, 25	nQ0, Q0	Output		Differential output pair. LVPECL/ECL interface levels.
26	V_{EE}	Power		Negative supply pin.
27	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects PCLK1, nPCLK1 inputs. When LOW, selects PCLK0, nPCLK0 inputs. LVPECL single-ended interface levels. Also accepts standard LVCMOS input levels.
28	PCLK0	Input	Pulldown	Non-inverting differential LVPECL clock input.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor			75		kΩ
$R_{VCC/2}$	Pullup/Pulldown Resistors			50		kΩ

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V (LVPECL mode, V_{EE} = 0V)
Negative Supply Voltage, V_{EE}	-4.6V (ECL mode, V_{CC} = V_{CCO} = 0V)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5V
Inputs, V_I (ECL mode)	0.5V to V_{EE} – 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
V_{BB} Sink/Source, I_{BB}	± 0.5mA
Operating Temperature Range, T_A	-40°C to +85°C
Package Thermal Impedance, θ_{JA}	50.4°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. LVPECL Power Supply DC Characteristics, V_{CC} = V_{CCO} = 3.0V to 3.8V, V_{EE} = 0V; T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.0	3.3	3.8	V
V_{CCO}	Output Supply Voltage		3.0	3.3	3.8	V
I_{EE}	Power Supply Current				65	mA

Table 3B. ECL Power Supply DC Characteristics, V_{EE} = -3.8V to -3.0V, V_{CC} = V_{CCO} = 0V; T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{EE}	Supply Voltage		-3.0	-3.3	-3.8	V
I_{EE}	Power Supply Current				65	mA

Table 3C. LVPECL DC Characteristics, $V_{CC} = V_{CCO} = 3.0V$ to $3.8V$; $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.15	V_{CC} - 0.94	V_{CC} - 0.86	V_{CC} - 1.14	V_{CC} - 0.96	V_{CC} - 0.88	V_{CC} - 1.13	V_{CC} - 0.97	V_{CC} - 0.89	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 1.835	V_{CC} - 1.73	V_{CC} - 1.63	V_{CC} - 1.875	V_{CC} - 1.75	V_{CC} - 1.665	V_{CC} - 1.87	V_{CC} - 1.765	V_{CC} - 1.67	V
V_{IH}	Input High Voltage (Single-ended); NOTE 2		V_{CC} - 1.225		V_{CC} - 0.94	V_{CC} - 1.225		V_{CC} - 0.94	V_{CC} - 1.225		V_{CC} - 0.94	V
V_{IL}	Input Low Voltage (Single-ended); NOTE 2		V_{CC} - 1.87		V_{CC} - 1.535	V_{CC} - 1.87		V_{CC} - 1.535	V_{CC} - 1.87		V_{CC} - 1.535	V
V_{BB}	Output Voltage Reference		V_{CC} - 1.44		V_{CC} - 1.30	V_{CC} - 1.44		V_{CC} - 1.30	V_{CC} - 1.44		V_{CC} - 1.30	V
V_{PP}	Peak-to-Peak Input Voltage		150		1000	150		1000	150		1000	mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3		1.2		V_{CC}	1.2		V_{CC}	1.2		V_{CC}	V
I_{IH}	Input High Current	PCLK[0:1], nPCLK[0:1], CLK_SEL			150			150			150	µA
I_{IL}	Input Low Current	PCLK[0:1], CLK_SEL	-10			-10			-10			µA
		nPCLK[0:1]	-150			-150			-150			µA

NOTE 1: Outputs terminated with 50Ω to $V_{CCO} – 2V$.
NOTE 2: Applies to CLK_SEL, PCLK0, nPCLK0, PCLK1, and nPCLK1 if connected to V_{BB} per Figure 2.
NOTE 3: Common mode voltage is defined as V_{IH}.

Table 3D. ECL DC Characteristics, $V_{CC} = V_{CCO} = 0V$; $V_{EE} = -3.8V$ to $-3.0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		-1.15	-0.94	-0.86	-1.14	-0.96	-0.88	-1.13	-0.97	-0.89	V
V_{OL}	Output Low Voltage; NOTE 1		-1.835	-1.73	-1.63	-1.875	-1.75	-1.665	-1.87	-1.765	-1.67	V
V_{IH}	Input High Voltage (Single-ended); NOTE 2		-1.225		-0.94	-1.225		- 0.94	-1.225		- 0.94	V
V_{IL}	Input Low Voltage (Single-ended); NOTE 2		-1.87		-1.535	-1.87		-1.535	-1.87		-1.535	V
V_{BB}	Output Voltage Reference		-1.44		-1.30	-1.44		-1.30	-1.44		-1.30	V
V_{PP}	Peak-to-Peak Input Voltage		150		1000	150		1000	150		1000	mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3		V_{EE} + 1.2		V_{CC}	V_{EE} + 1.2		V_{CC}	V_{EE} + 1.2		V_{CC}	V
I_{IH}	Input High Current	PCLK[0:1], nPCLK[0:1], CLK_SEL			150			150			150	µA
I_{IL}	Input Low Current	PCLK[0:1], CLK_SEL	-10			-10			-10			µA
		nPCLK[0:1]	-150			-150			-150			µA

For NOTES, see Table 3C above.

AC Electrical Characteristics

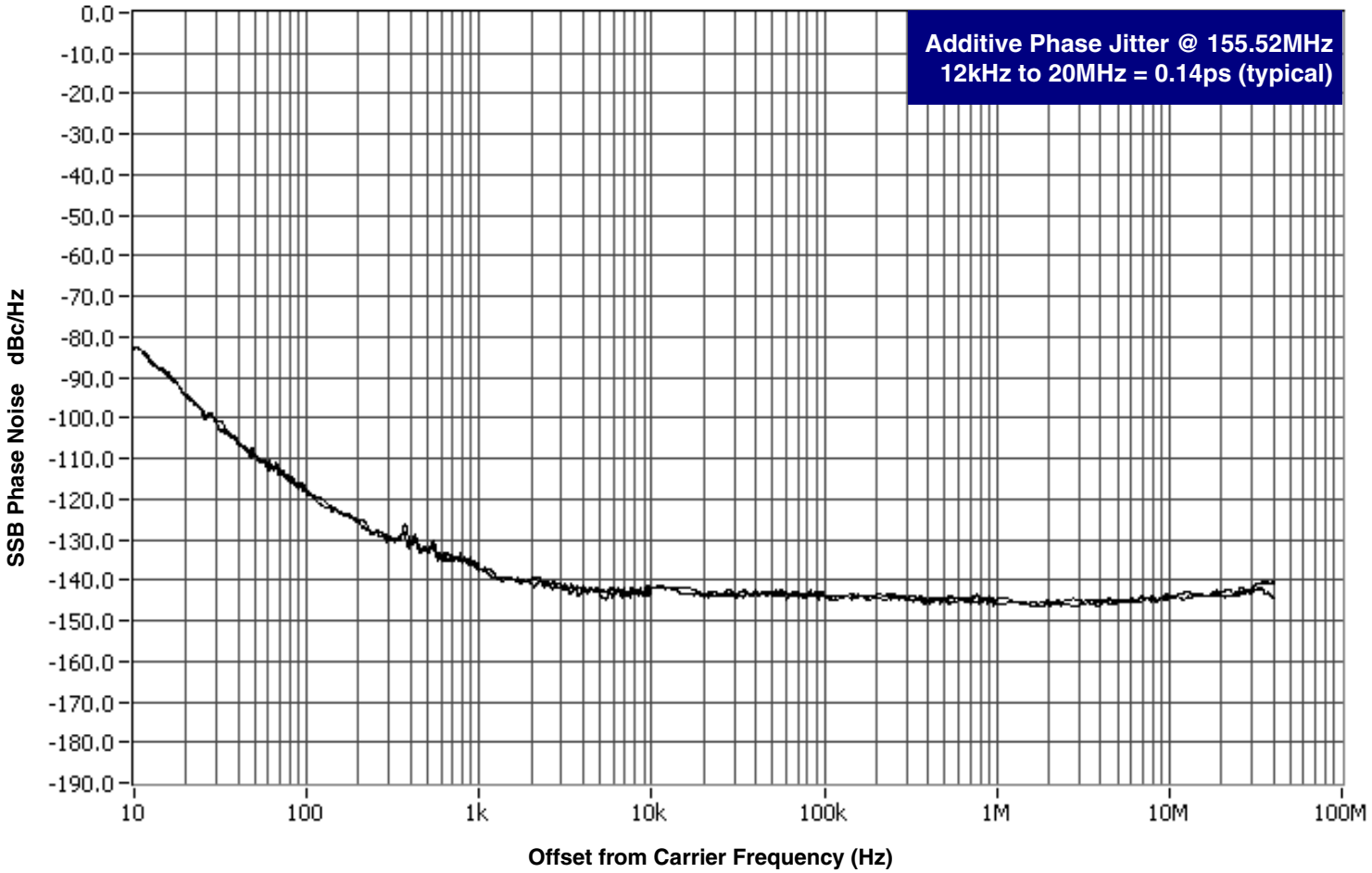
Table 4. AC Characteristics, V_{CC} = V_{CCO} = 3.0V to 3.8V, V_{EE} = 0V; or V_{EE} = -3.8V to -3.0V, V_{CC} = V_{CCO} = 0V; T_A = -40°C to 85°C

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{OUT}	Output Frequency				2			2			2	GHz
t_{PD}	Propagation Delay; NOTE 1		550	750	975	600	825	1050	625	885	1150	ps
*t*sk(o)	Output Skew; NOTE 2, 4			20	40		20	40		20	40	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				275			275			320	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section						0.14					ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	90		375	90		375	80		400	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters are measured at $f_{OUT} \leq$ 1.2GHz, unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

Additive Phase Jitter

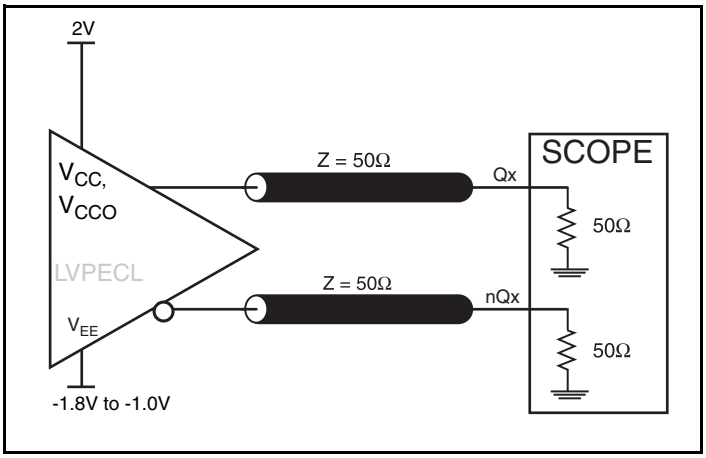
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



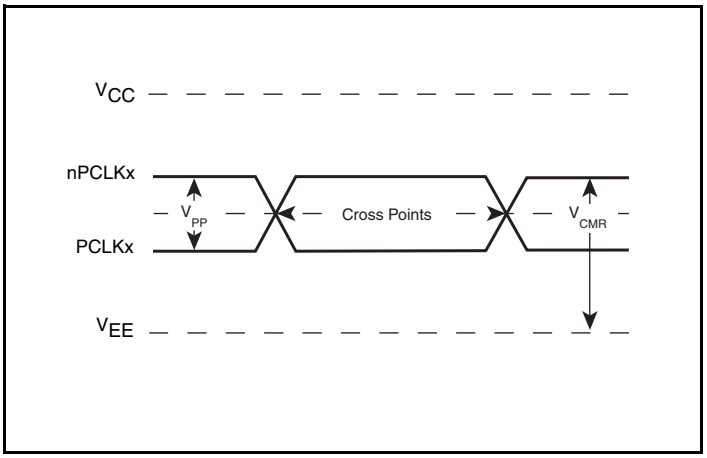
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator used is, "IFR2042 as the external input to a Hewlett Packard 8133A 3GHz Pulse Generator".

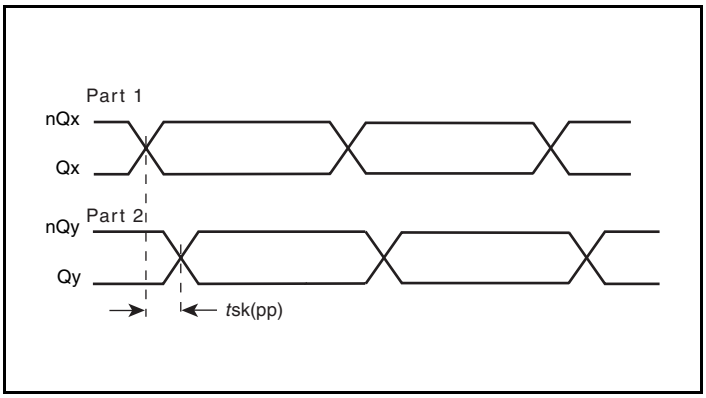
Parameter Measurement Information



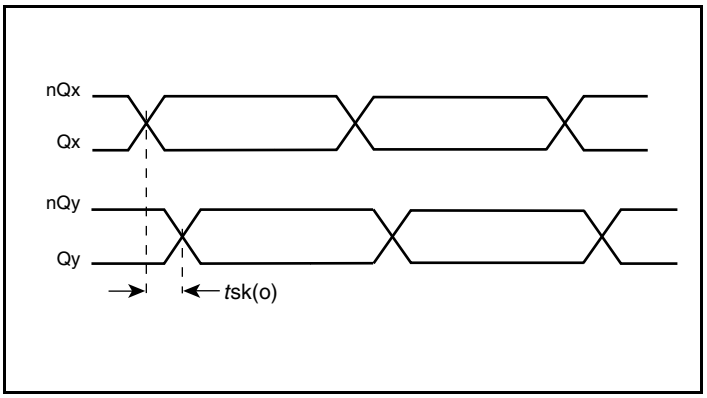
LVPECL Output Load AC Test Circuit



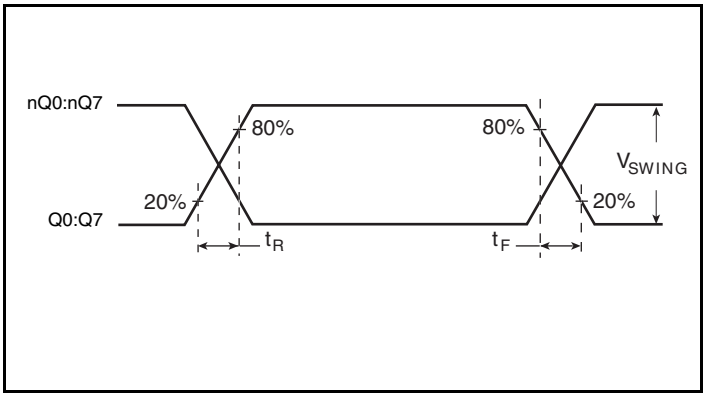
Differential Input Level



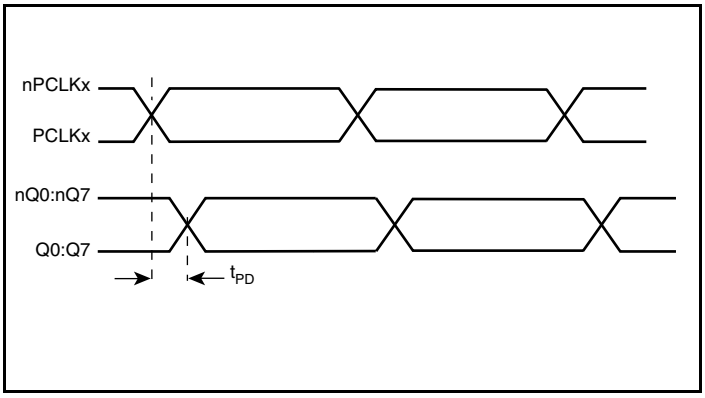
Part-to-Part Skew



Output Skew



Output Rise/Fall Time



Propagation Delay

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

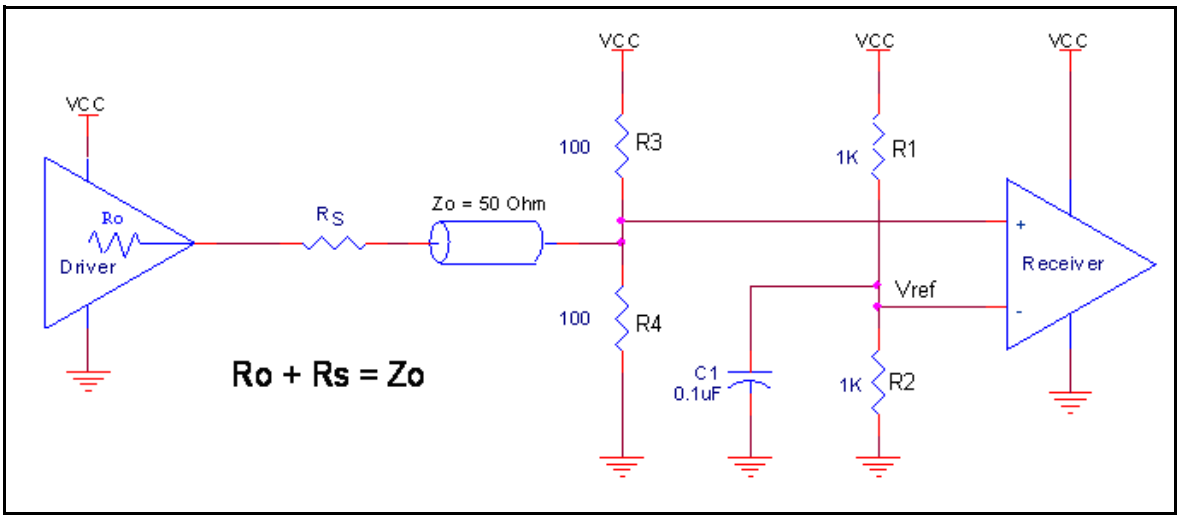


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Wiring the Differential Input to Accept Single-ended LVPECL Levels

Figure 2 shows an example of the differential input that can be wired to accept single-ended LVPECL levels. The reference voltage level V_{BB} generated from the device is connected to the negative input. The C1 capacitor should be located as close as possible to the input pin.

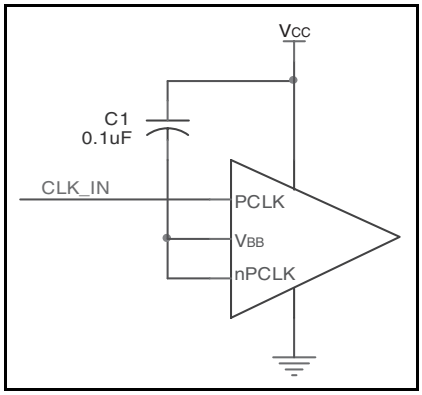


Figure 2. Single-Ended LVPECL Signal Driving Differential Input

LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the PCLK/nPCLK input driven by the most common driver types.

The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

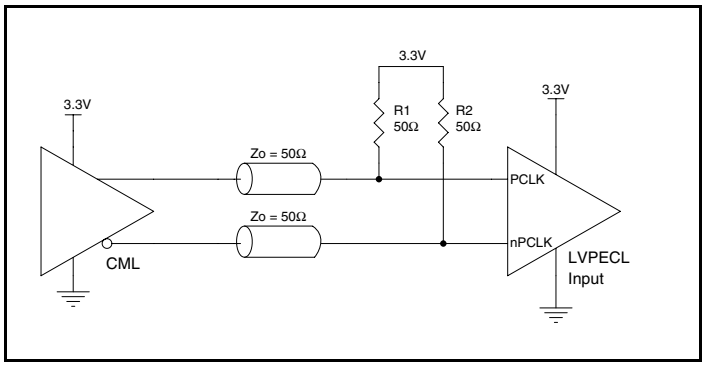


Figure 3A. PCLK/nPCLK Input Driven by a CML Driver

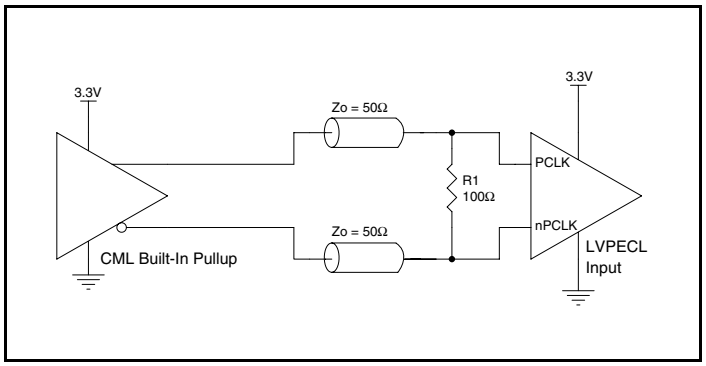


Figure 3B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

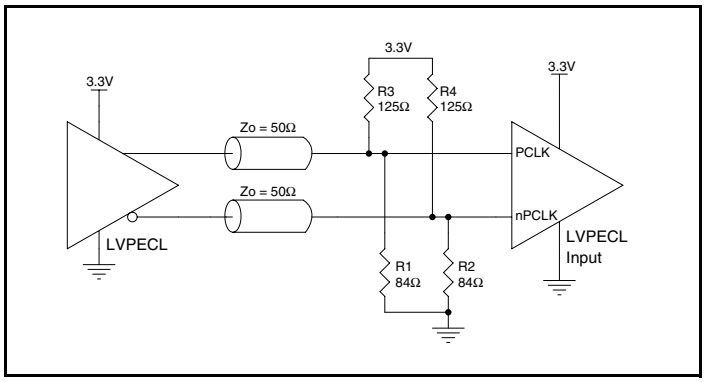


Figure 3C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

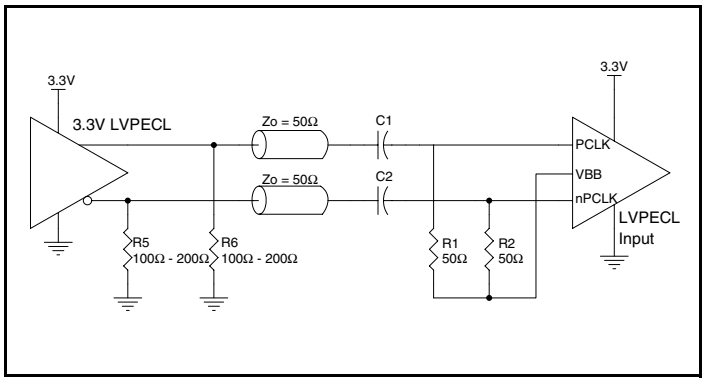


Figure 3D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

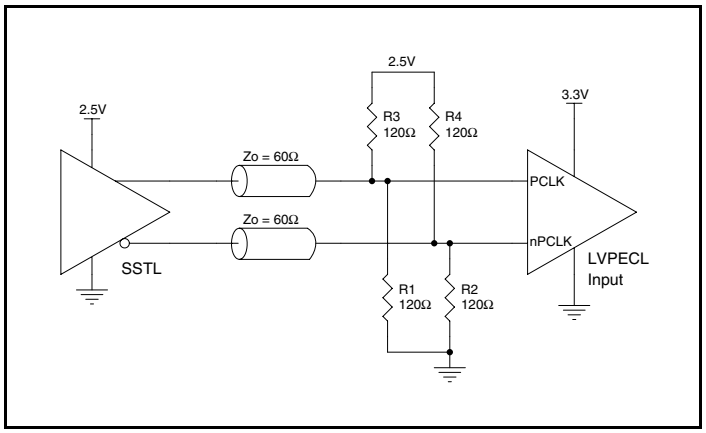


Figure 3E. PCLK/nPCLK Input Driven by an SSTL Driver

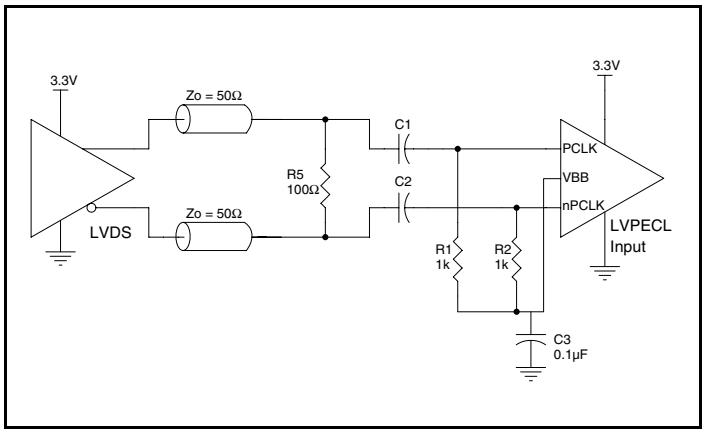


Figure 3F. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

Recommendations for Unused Output Pins

Inputs:

PCLK/nPCLK Inputs

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

LVPECL Control Pins

The control pin has an internal pulldown; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

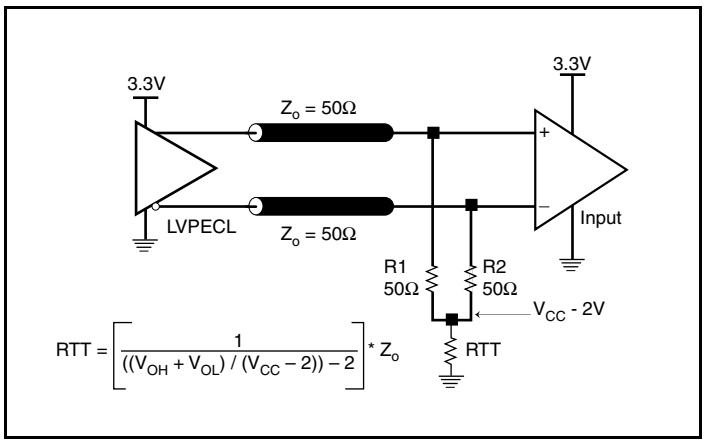


Figure 4A. 3.3V LVPECL Output Termination

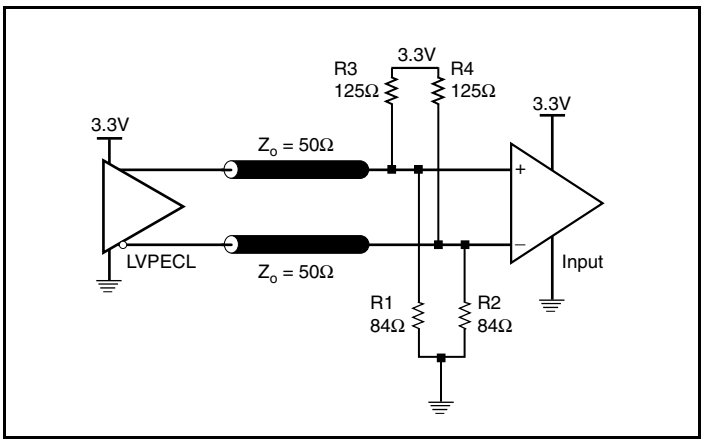


Figure 4B. 3.3V LVPECL Output Termination

Schematic Example

Figure 5A shows a schematic example of the ICS853S310I. In this example, the PCLK0, nPCLK0 input is selected. The decoupling capacitors should be physically located near the power pin. For ICS853S310I, the unused outputs can be left floating.

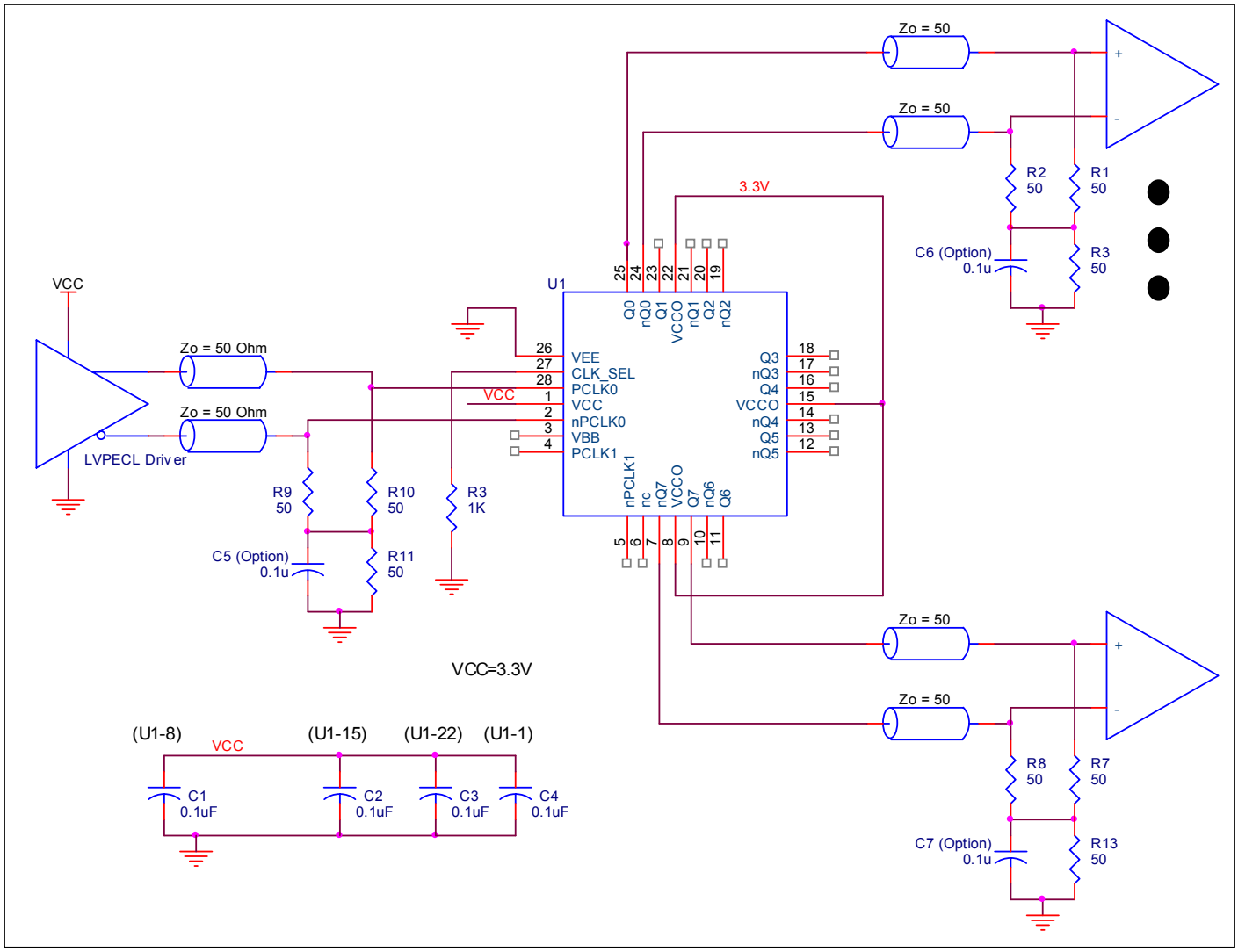


Figure 5A. ICS853S310I LVPECL Clock Output Buffer Schematic Example

Power, Ground and Bypass Capacitor

This section provides a layout guide related to power, ground and placement of bypass capacitors for a high-speed digital IC. This layout guide is a general recommendation. The actual board design will depend on the component types being used, the board density and cost constraints. This description assumes that the board has clean power and ground planes. The goal is to minimize the ESR between the clean power/ground plane and the IC power/ground pin.

A low ESR bypass capacitor should be used on each power pin. The value of bypass capacitors ranges from 0.01uF to 0.1uF. The bypass capacitors should be located as close to the power pin as possible. It is preferable to locate the bypass capacitor on the same side as the IC. *Figure 5B* shows suggested capacitor placement. Placing the bypass capacitor on the same side as the IC allows the capacitor to have direct contact with the IC power pin. This can avoid any vias between the bypass capacitor and the IC power pins.

The vias should be placed at the Power/Ground pads. There should be a minimum of one via per pin. Increasing the number of vias from the Power/Ground pads to Power/Ground planes can improve the conductivity.

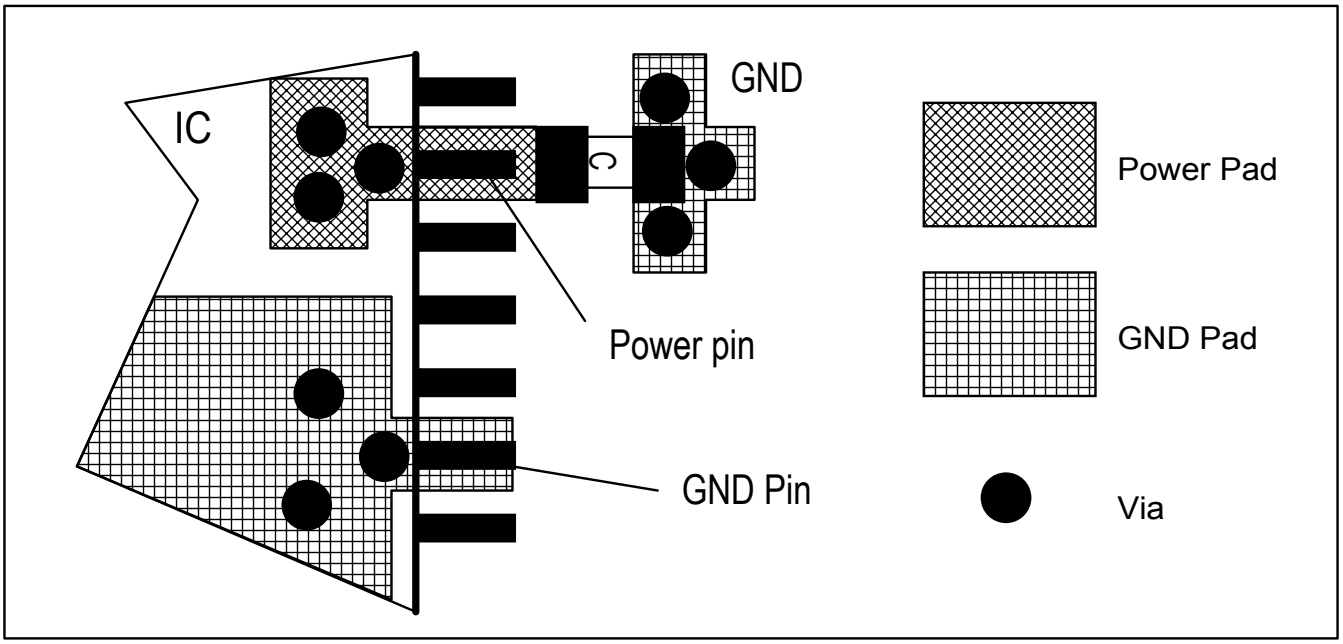


Figure 5B. Recommended Layout of Bypass Capacitor Placement

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS853S310I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS853S310I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.8V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.8V * 65mA = **247mW**
- Power $(outputs)_{MAX}$ = **30.78mW/Loaded Output pair**
  If all outputs are loaded, the total power is 8 * 30.78mW = **246.24mW**

Total Power$_{\_MAX}$ (3.8V, with all outputs switching) = 247mW + 246.24mW = **493.24mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and it directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 50.4°C/W per Table 5 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.493W * 50.4°C/W = 109.9°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 5. Thermal Resistance θ_{JA} for 28 Lead PLCC, Forced Convection

θ_{JA} by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	50.4°C/W	44.4°C/W	41.8°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 6.*

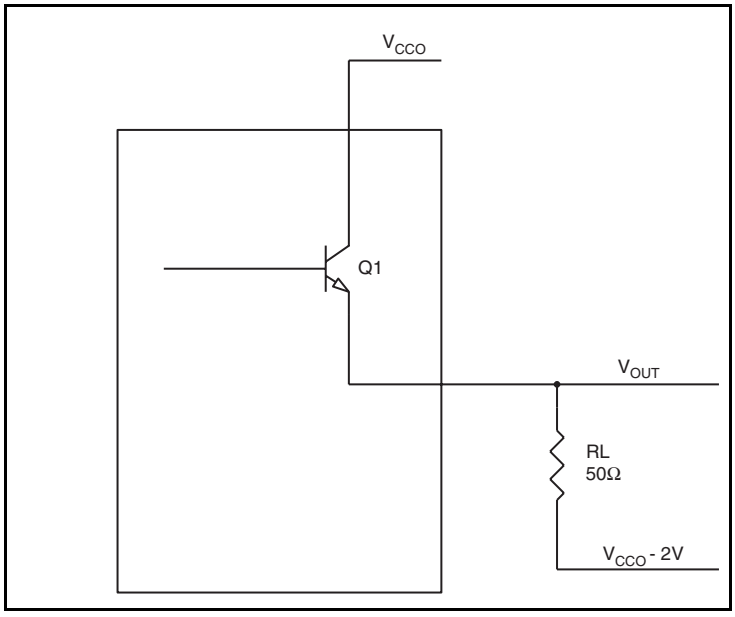


Figure 6. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} =$ **V_{CCO_MAX} – 0.89V**
  ($V_{CCO\_MAX} - V_{OH\_MAX}$) = **0.89V**
- For logic low, $V_{OUT} = V_{OL\_MAX} =$ **V_{CCO_MAX} – 1.67V**
  ($V_{CCO\_MAX} - V_{OL\_MAX}$) = **1.67V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.89V)/50\Omega] * 0.89V =$ **19.76mW**

$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.67V)/50\Omega] * 1.67V =$ **11.02mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.78mW**

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 28 Lead PLCC

θ_{JA} vs. Air Flow			
Linear Feet per Minute	**0**	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	50.4°C/W	44.4°C/W	41.8°C/W

Transistor Count

The transistor count for ICS853S310I is: 386

This device is pin and functional compatible with and is the suggested replacement for the ICS853310.

Package Outline and Package Dimensions

Package Outline - V Suffix for 28 Lead PLCC

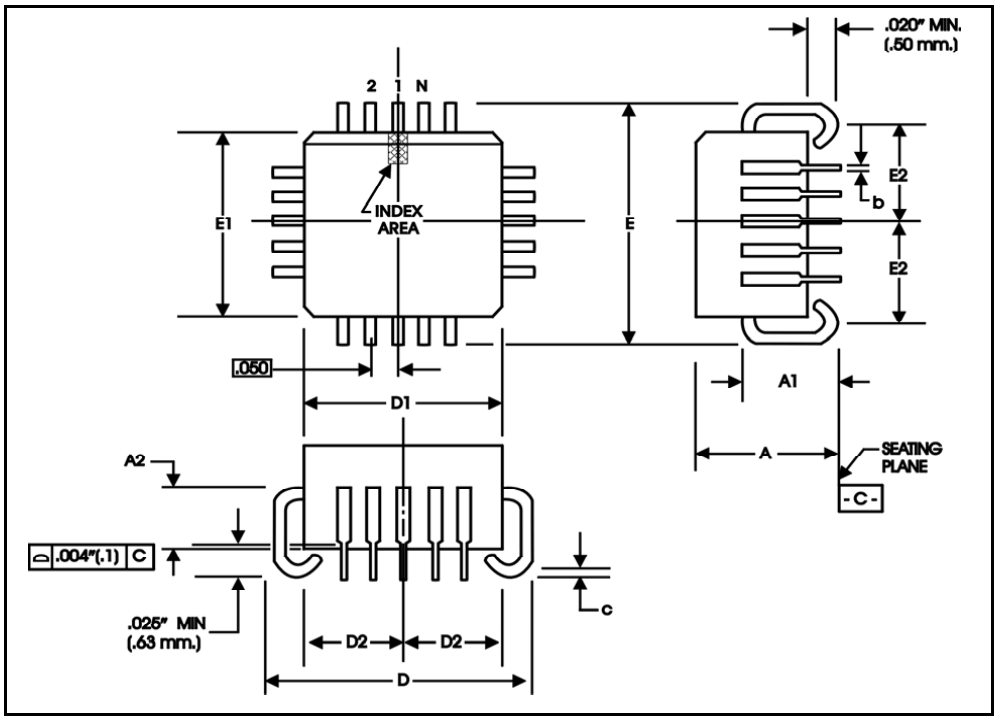


Table 7. Package Dimensions for 28 Lead PLCC

JEDEC: 300 MIL All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	28	
A	4.19	4.57
A1	2.29	3.05
A2	1.57	2.11
b	0.33	0.53
c	0.19	0.32
D/E	12.32	12.57
D1/E1	11.43	11.58
D2/E2	4.85	5.56

Reference Document: JEDEC Publication 95, MS-018

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
853S310CVILF	ICS853S310CVILF	28 Lead “Lead-Free” PLCC	Tube	-40°C to 85°C
853S310CVILFT	ICS853S310CVILF	28 Lead “Lead-Free” PLCC	500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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