47L64

64-Kbit I²C EERAM

Serial SRAM Features

- Unlimited Reads/Unlimited Writes:
  - Standard serial SRAM protocol
  - Symmetrical timing for reads and writes
- SRAM Array:
  - 8,192 x 8 bits
- High-Speed I²C Interface:
  - Industry standard: 1 MHz, 400 kHz, and 100 kHz
  - Zero cycle delay writes and reads to SRAM array
  - Schmitt Trigger inputs for noise suppression
- Low-Power CMOS Technology:
  - Active current: 1 mA (maximum)
  - Standby current: 200 µA (maximum)

Hidden EEPROM Backup Features

- Cell-Based Nonvolatile Backup:
  - Mirrors SRAM array cell-for-cell
  - Transfers all data to/from SRAM cells in parallel (all cells at same time)
- Invisible-to-User Data Transfers:
  - V_{CC} level monitored inside device
  - SRAM automatically saved on power disrupt
  - SRAM automatically restored on V_{CC} return
- 100,000 Backups Minimum
- 100 Years Retention (at 55°C)

Other Features of the 47L64

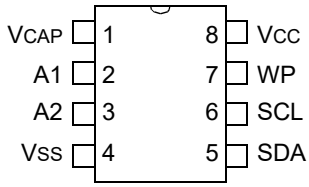
- Operating Voltage Range: 2.7V to 3.6V
- Temperature Ranges:
  - Industrial (I): -40°C to +85°C
- ESD protection: >2,000V

Packages

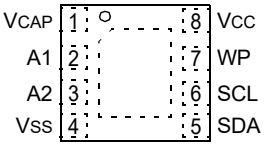
- 8-Lead SOIC
- 8-Lead TDFN

Package Types (not to scale)

8-Lead SOIC
(Top View)



TDFN[1]
(Top View)



Note 1: Includes Exposed Thermal Pad (EP)

Pin Descriptions

Pin Name	Description
V_{CAP}	External Capacitor
A1, A2	Hardware Address Pins
V_{SS}	Ground
SCL	Serial Clock Input
SDA	Serial Data Input/Output
WP	Write-Protect Input
V_{CC}	Power Supply

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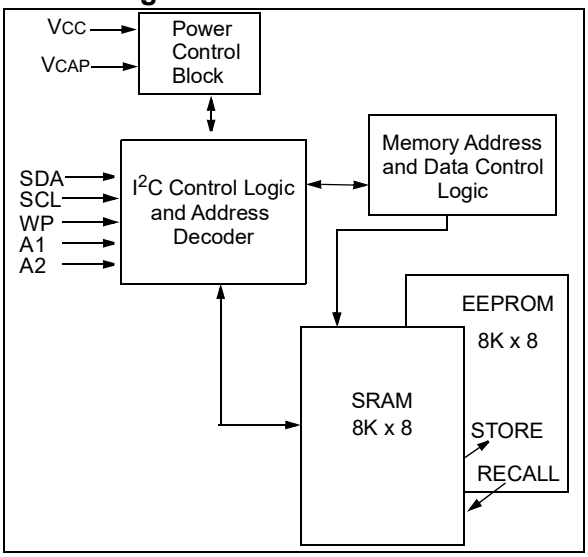
General Description

The Microchip Technology Inc. 47L64 serial EERAM has an SRAM memory core with hidden EEPROM backup. The device can be treated by the user as a full symmetrical read/write SRAM. Backup to EEPROM is handled by the device on any power disrupt, so the user can effectively view this device as an SRAM that never loses its data.

The device is structured as a 64-Kbit SRAM with EEPROM backup in each memory cell. The SRAM is organized as 8,192 x 8 bits and uses the I^2C serial interface. The I^2C bus uses two signal lines for communication: clock input (SCL) and data (SDA). Access to the device is controlled through a chip address and address pins, allowing up to four devices to share the same bus.

The SRAM is a conventional serial SRAM: it allows symmetrical reads and writes and has no limits on cell usage. The backup EEPROM is invisible to the user and cannot be accessed by the user independently. The device includes circuitry that detects VCC dropping below a certain threshold, shuts its connection to the outside environment, and transfers all SRAM data to the EEPROM portion of each cell for safe keeping. When VCC returns, the circuitry automatically returns the data to the SRAM and the user's interaction with the SRAM can continue with the same data set.

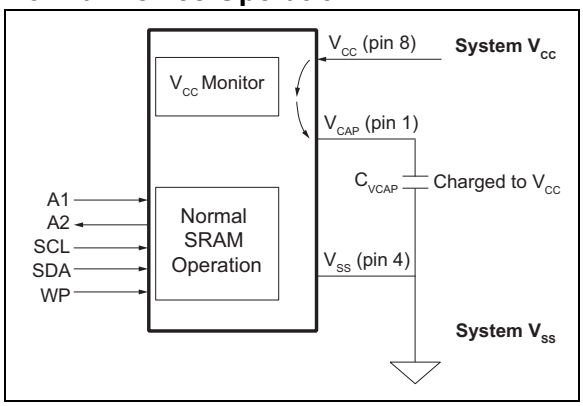
Block Diagram



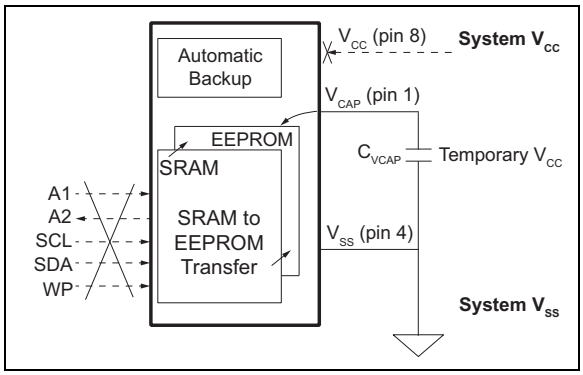
Powering the Device During SRAM to EEPROM Backup (VCAP)

A small capacitor (typically 22 µF) is required for the proper operation of the device. This capacitor is placed between VCAP (pin 1) and the system VSS (see Normal Device Operation). When power is first applied to the device, this capacitor is charged to VCC through the device (see Normal Device Operation). During normal SRAM operation, the capacitor remains charged to VCC and the level of system VCC is monitored by the device. If system VCC drops below a set threshold, the device interprets this as a power-off or brown-out event. The device suspends all I/O operation, shuts off its connection with the VCC pin, and uses the saved energy in the capacitor to power the device through the VCAP pin as it transfers all SRAM data to EEPROM (see Vcc Power-Off Event). On the next power-up of VCC, the data is transfered back to SRAM, the capacitor is recharged, and the SRAM operation continues.

Normal Device Operation



Vcc Power-Off Event



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

VCC.....4.5V

All inputs and outputs w.r.t. VSS ..... -0.6V to 4.5V

Storage temperature ..... -65°C to 150°C

Ambient temperature under bias..... -55°C to 85°C

ESD protection on all pins..... 2 kV

† NOTICE: Stresses above those listed under 'Maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			**Electrical Characteristics:** Industrial (I): TAMB = -40°C to +85°C, VCC = 2.7V to 3.6V				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
D1	VIH	High-Level input Voltage	0.8 X VCC	—	VCC+0.5	V	
D2	VIL	Low-Level Input Voltage	-0.5	—	0.2*VCC	V	
D3	VOL	Low-Level Output Voltage	—	—	0.4	V	IOL = 2.0 mA
D4	VHYS	Hysteresis of Schmitt Trigger Inputs (SDA, SCL pins)	0.05 X VCC	—	—	V	**Note 1**
D5	ILI	Input Leakage Current (SDA, SCL pins)	—	—	±3	µA	VIN = VSS or VCC
D6	ILO	Output Leakage Current (SDA pin)	—	—	±3	µA	VOUT = VSS or VCC
D7	RIN	Input Resistance to VSS (A1, A2, WP pins)	50	—	—	kΩ	VIN = VIL (max)
D8	CINT	Internal Capacitance (all inputs and outputs)	—	—	7	pF	TAMB = 25°C, FREQ = 1 MHz, VCC = 3.3V (**Note 1**)
D9	ICC Active 1	Operating Current @ 1 MHz	—	—	1	mA	VCC = 3.6 V, FCLK = 1 MHz
D10	ICC Active 2	Operating Current @ 400 kHz	—	—	700	µA	VCC = 3.6 V, FCLK = 400 kHz
D11	ICCS	Standby Current	—	—	200	µA	SCL, SDA, VCAP, VCC = 3.6V
D12	VTRIP	AutoStore/AutoRecall Trip Voltage	2.3	—	2.65	V	**Note 1**
D13	VPOR	Power-on Reset Voltage	—	—	2.1	V	
D14	CB	Bus Capacitance	—	—	400	pF	
D15	CVCAP	VCAP Capacitor	10	22	50	µF	**Note 1**

Note 1: This parameter is periodically sampled and not 100% tested.

1.1 AC CHARACTERISTICS

TABLE 1-1: AC CHARACTERISTICS

AC CHARACTERISTICS			Industrial (I):	T_{AMB} = -40°C to +85°C, V_{CC} = 2.7V to 3.6V		
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
1	F_{CLK}	Clock Frequency	—	1000	kHz	
2	T_{HIGH}	Clock High Time	400	—	ns	
3	T_{LOW}	Clock Low Time	600	—	ns	
4	T_R	SDA and SCL Input Rise Time	—	300	ns	**Note 1**
5	T_F	SDA and SCL Input Fall Time	—	100	ns	**Note 1**
6	$T_{HD:STA}$	Start Condition Hold Time	250	—	ns	
7	$T_{SU:STA}$	Start Condition Setup Time	250	—	ns	
8	$T_{HD:DAT}$	Data Input Hold Time	0	—	ns	
9	$T_{SU:DAT}$	Data Input Setup Time	100	—	ns	
10	$T_{SU:STO}$	Stop Condition Setup Time	250	—	ns	
11	T_{AA}	Output Valid from Clock	—	550	ns	
12	T_{BUF}	Bus Free Time: Time the bus must be free before a new transmission can start	500	—	ns	
13	T_{OF}	Output Fall Time from V_{IH} Minimum to V_{IL} Maximum $C_B \leq 100pF$	20+0.1C_B	250	ns	$C_B \leq 100$ pF (**Note 1**)
14	T_{SP}	Input Filter Spike Suppression (SDA and SCL pins)	—	50	ns	
15	$T_{RESTORE}$	Power-up Recall Operation Duration	—	550	µs	
16	T_{STORE}	Store Operation Duration	—	10	ms	
17	T_{VRISE}	V_{CC} Rise Rate	30	—	µs/V	**Note 1**
18	T_{VFALL}	V_{CC} Fall Rate	30	—	µs/V	**Note 1**
19	—	Endurance	100,000	—	Store Cycles	25°C, V_{CC} = 3.6V (**Note 1**, **Note 2**)
20		Retention	100		Years	55°C

Note 1: This parameter is not tested but ensured by characterization.

2: For endurance estimates in a specific application, consult the Total Endurance Model which can be obtained on Microchip's website at www.microchip.com.

FIGURE 1-1: BUS TIMING DATA

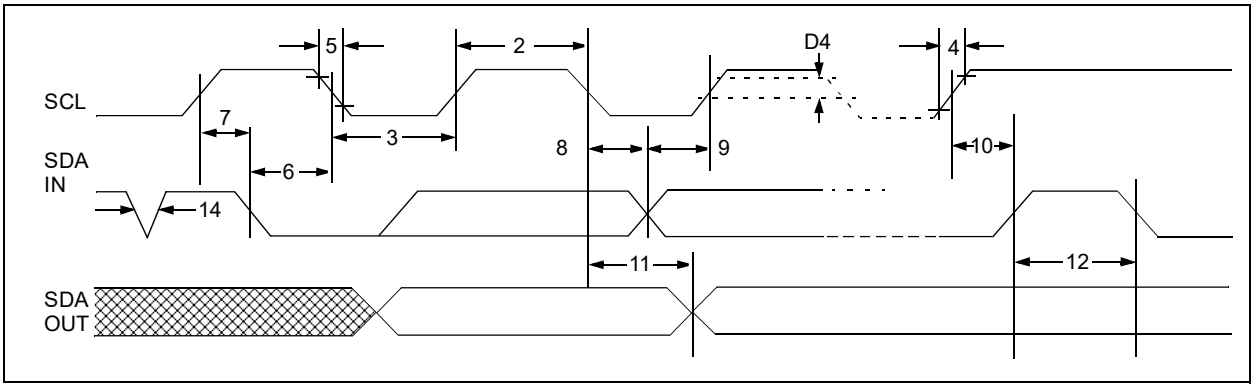
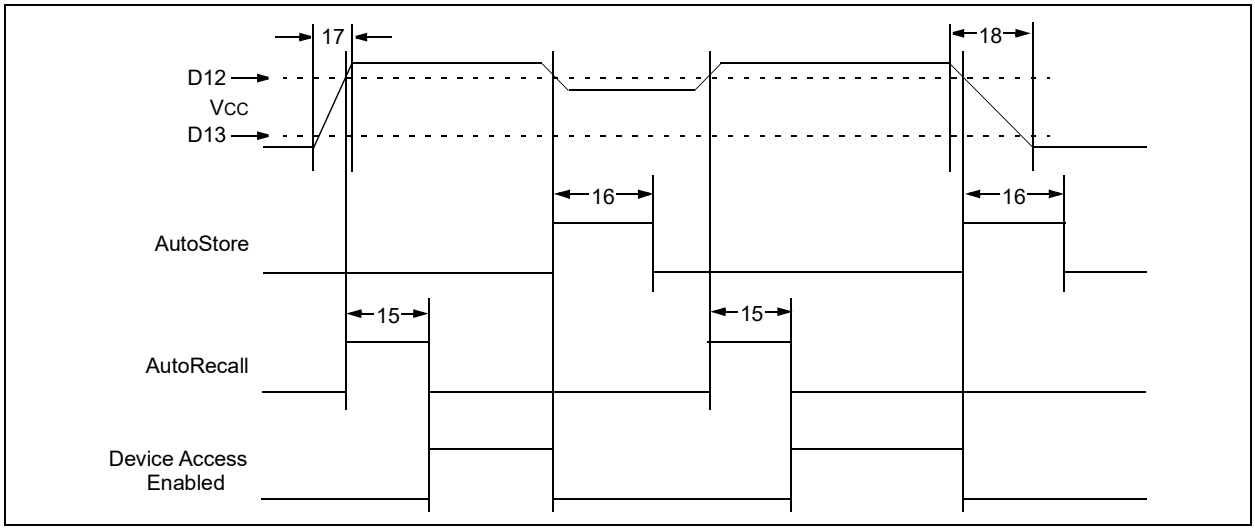


FIGURE 1-2: AUTOSTORE/AUTORECALL TIMING DATA



2.0 PIN DESCRIPTION

The description of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	8-Lead SOIC	8-Lead TDFN(1)	Function
VCAP	1	1	External Capacitor
A1	2	2	Chip Select Input
A2	3	3	Chip Select Input
Vss	4	4	Ground
SDA	5	5	Serial Data
SCL	6	6	Serial Clock
WP	7	7	Write Protect
Vcc	8	8	2.7V to 3.6V

Note 1: The exposed pad on the TDFN package can be connected to VSS or left floating.

2.1 A1, A2 Chip Address Inputs

The A1, A2 inputs are used by the 47L64 for multiple device operation. The levels on these inputs are compared with the corresponding Chip Select bits in the slave address. The chip is selected if the comparison is true.

Up to four devices may be connected to the same bus by using different Chip Select bit combinations. These pins are not pulled up or down internally, so they must be externally connected to VCC or VSS.

2.2 Serial Data (SDA)

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open-drain terminal, therefore, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz and 1 MHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

2.3 Serial Clock (SCL)

This input is used to synchronize the data transfer from and to the device.

2.4 Write-Protect Input

When the WP pin is set high, then writes within the upper 1/4 of memory will not be allowed. Attempts to write in that protected region over the I^2C bus will return an ACK (Acknowledge) for the `WRITE` instruction and address byte portions of the command, and will also return an ACK (Acknowledge) for the data portion of the command, despite the fact that no data will be written. See Table 4-1. The WP pin has no effect on random or sequential read operations. If left floating, this pin is internally pulled low.

3.0 MEMORY ORGANIZATION

3.1 Data Array Organization

The 47L64 is internally organized as a continuous SRAM array for both reading and writing, along with a nonvolatile EEPROM version that is not directly accessible to the user, but which can be refreshed or recalled on power cycles.

3.2 STORE/RECALL OPERATIONS

In order to provide nonvolatile storage of the SRAM data, an EEPROM array is included on the 47L64. During normal operation, the EEPROM array is not directly accessible to the user. Instead, the 47L64 preserves the SRAM data by automatically performing store and recall operations on power-down and power-up, respectively.

3.2.1 AUTOSTORE

To simplify device usage, the 47L64 features an AutoStore mechanism. To enable this feature, the user must place a capacitor on the VCAP pin. The capacitor is charged through the VCC pin. When the 47L64 detects a power-down event, the device automatically switches to the capacitor for power and initiates the AutoStore operation.

To avoid extraneous store operations, the AutoStore will only be initiated if the SRAM array has been modified since the last Store or Recall operation.

The AutoStore is initiated when VCAP falls below VTRIP. Even if power is restored, the 47L64 cannot be accessed for TSTORE time and TRESTORE after the AutoStore is initiated.

Note:	If power is restored during an AutoStore operation, the AutoStore will continue and then the AutoRecall will be performed.

3.2.2 AUTORECALL

The 47L64 devices features an AutoRecall mechanism that is performed on power-up. This feature ensures that the SRAM data duplicates the EEPROM data on power-up. The AutoRecall is initiated when VCAP rises above VTRIP, and the 47L64 cannot be accessed for TRESTORE time after the AutoRecall is initiated.

Note 1:	If power is lost during an AutoRecall operation, the AutoRecall is aborted and the AutoStore is not performed.
2:	AutoRecall is performed every time VCAP rises above VTRIP.

3.2.3 POLLING ROUTINE

Since the device will not acknowledge during store and recall operations, checking for the Acknowledge signal can be used to determine when those events are complete. Once such an event has started, Acknowledge polling can be initiated immediately. This involves the master sending a Start condition, followed by the write control byte (R/$\overline{W}$ = 0) for the SRAM array. If the device is still busy, then no Acknowledge will be returned. In this case, the Start condition and control byte must be resent. If the Store or Recall are complete, then the device will return an Acknowledge, and the master can then proceed with the next read or write command. See Figure 3-1 for flow diagram.

FIGURE 3-1: POLLING FLOW

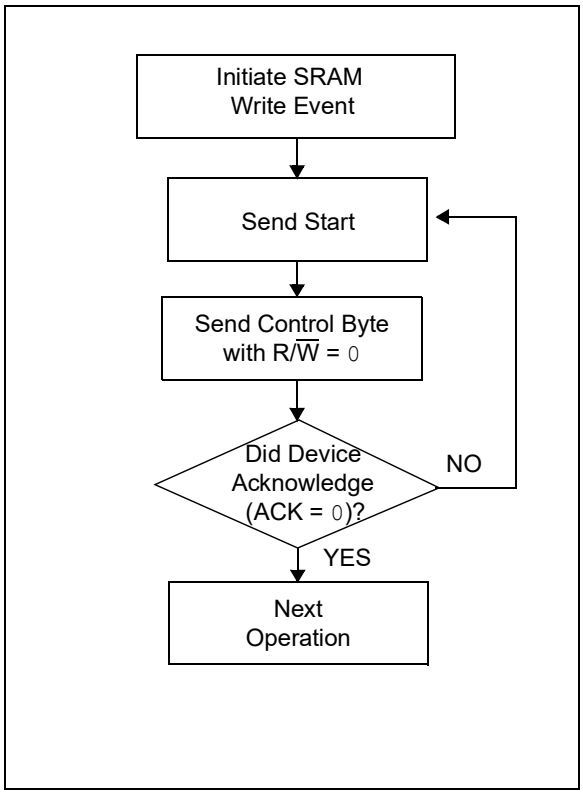
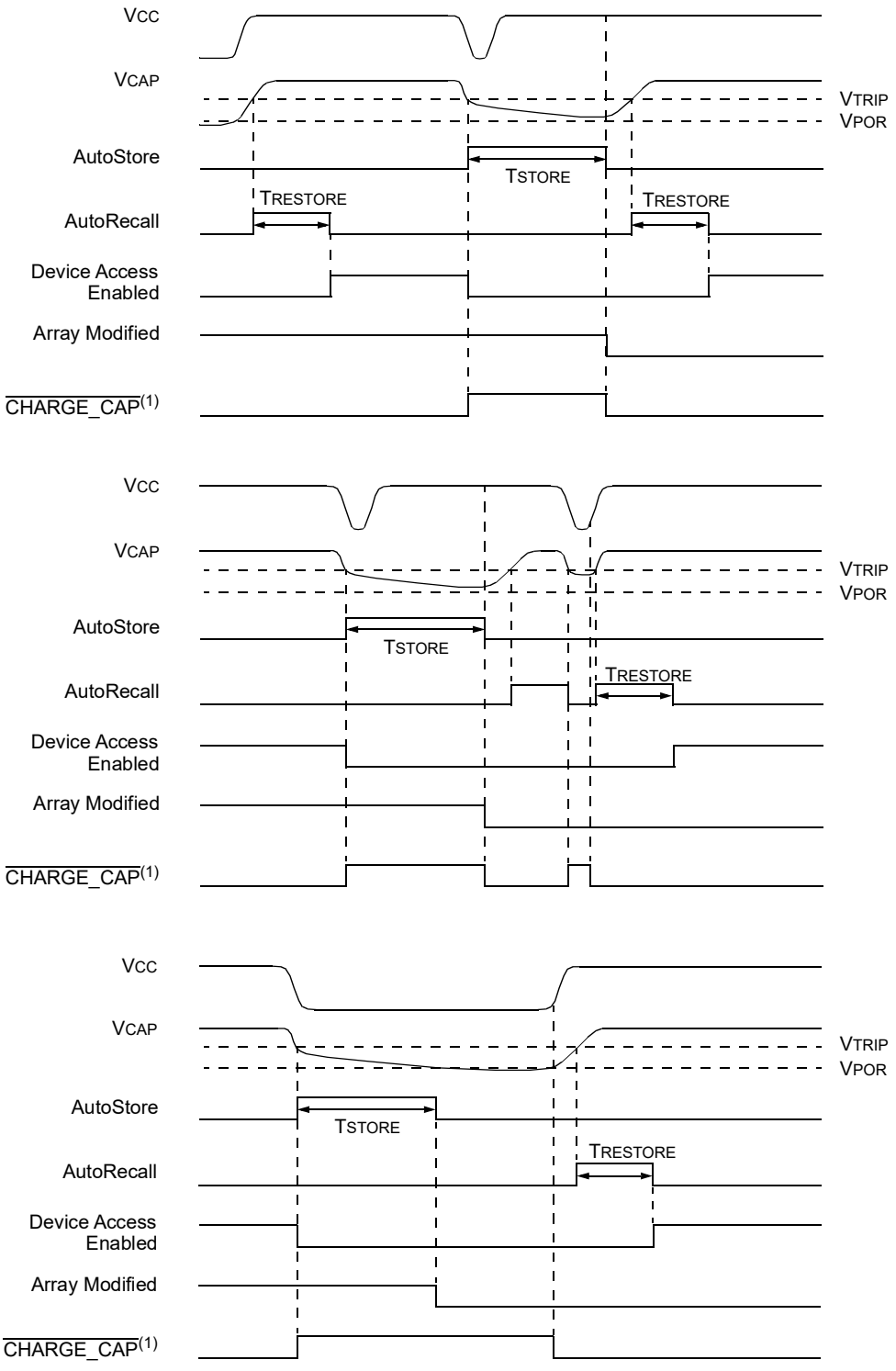
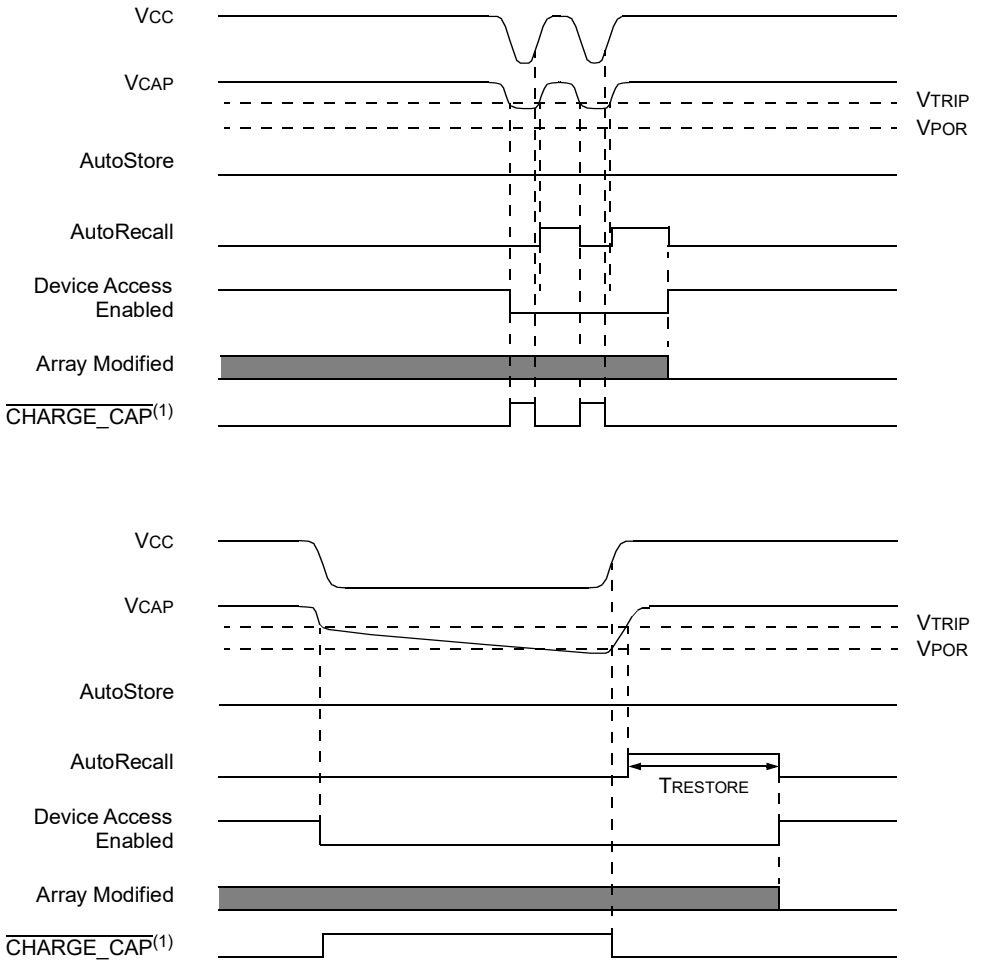


FIGURE 3-2: AUTOSTORE/AUTORECALL SCENARIOS (WITH ARRAY MODIFIED)



Note 1: When $\overline{\text{CHARGE\_CAP}}$ is a '0', VCC is connected to VCAP, allowing VCC to charge the external capacitor. See **Section 3.2.5 "Power Switchover"** for details.

FIGURE 3-3: AUTOSTORE/AUTORECALL SCENARIOS (WITH ARRAY NOT MODIFIED)



Note 1: When $\overline{\text{CHARGE\_CAP}}$ is a '0', VCC is connected to VCAP, allowing VCC to charge the external capacitor. See **Section 3.2.5 "Power Switchover"** for details.

3.2.4 TRIP VOLTAGE

The 47L64 has an internal voltage reference that is used to create a trip voltage threshold (VTRIP). When VCAP rises above VTRIP, a power-up event is detected. If this is the first power-up event after a POR, then an AutoRecall operation is initiated. When VCAP falls below VTRIP, a power-down event is detected and an AutoStore operation is initiated if the array has been modified.

Note:	When VCAP is below VTRIP, the 47L64 cannot be accessed and will not acknowledge any commands.

3.2.5 POWER SWITCHOVER

To support the AutoStore feature, the 47L64 must be able to charge the capacitor connected to the VCAP pin when power is available on VCC, and also automatically switch to being powered from the VCAP pin when power is removed from VCC. Since the VCAP pin is used as part of the internal power bus, this means that VCC must be disconnected when power is removed.

To accomplish this, the 47L64 has an intelligent power switchover circuit that continuously monitors the voltages on both VCC and VCAP.

During a power-up event, VCC is initially disconnected, allowing it to rise above VCAP. Once VCC is above VCAP, VCAP is connected to the VCC, charging the external capacitor. When VCAP reaches VTRIP, the AutoRecall operation is triggered.

During a power-down event, VCC is initially connected to the internal power bus. As Vcc falls, it discharges the external cap, causing VCAP to also fall. Once VCAP falls below VTRIP, the AutoStore operation is triggered, and VCC is disconnected to prevent discharging the capacitor further through VCC.

Once V_{CC} is disconnected, it will not be reconnected until both V_{CC} is greater than V_{CAP} and any internal store cycles (AutoStore) is complete. This guards against continuously connecting and disconnecting V_{CC} when V_{CAP} falls faster than V_{CC}.

4.0 FUNCTIONAL DESCRIPTION

4.0.1 PRINCIPLES OF OPERATION

The 47L64 is a 64-Kbit serial EERAM designed to support a bidirectional two-wire bus and data transmission protocol (I^2C). A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the Start and Stop conditions, while the 47L64 works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is active.

4.1 BUS CHARACTERISTICS

4.1.1 SERIAL INTERFACE

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1.1.1 Bus Not Busy (A)

Both data and clock lines remain high.

4.1.1.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

4.1.1.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must end with a Stop condition.

4.1.1.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the master device.

4.1.1.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (47L64) will leave the data line high to enable the master to generate the Stop condition.

The 47L64 will generate an Acknowledge bit on receiving a correct control byte and following address and data bytes. Table 4-1 summarizes these situations. The device will not generate Acknowledge bits for any bytes following if the control byte is incorrect, such as when the address bits do not match the A1, A2 pins, see **Section 4.2 “Device Addressing”**.

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

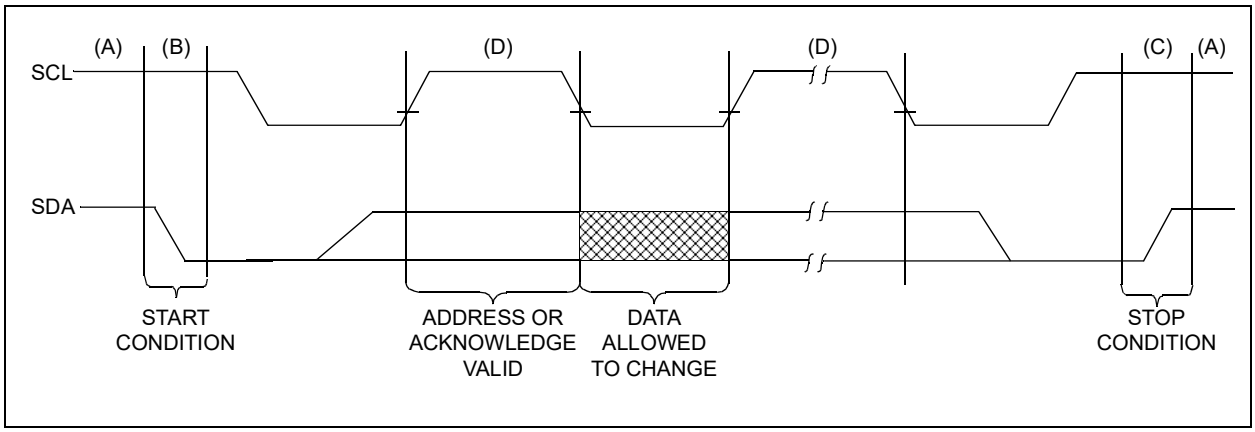


FIGURE 4-2: ACKNOWLEDGE TIMING

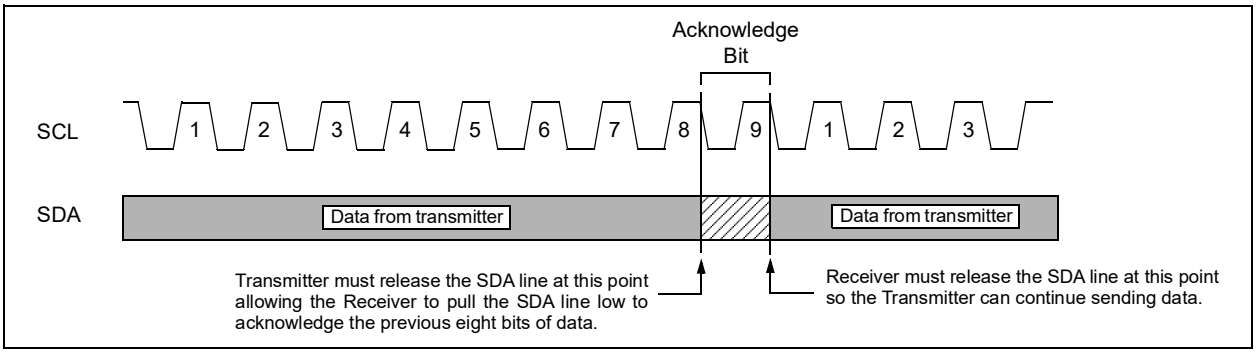


TABLE 4-1: ACKNOWLEDGE TABLE FOR SRAM WRITES

Instruction	ACK	Address MSB	ACK	Address LSB	ACK	Data Byte	ACK
SRAM Write in Unprotected Block	ACK	Address	ACK	Address	ACK	Data	ACK
SRAM Write in Protected Block	ACK	Address	ACK	Address	ACK	Data	ACK

4.2 DEVICE ADDRESSING

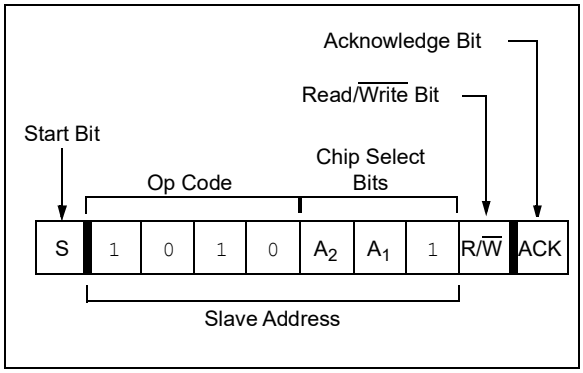
The control byte is the first byte received following the Start condition from the master device (Figure 4-3). The control byte begins with a 4-bit op code. The next two bits are the user-configurable chip select bits, A_2 and A_1. The next bit is a non-configurable chip select bit that must always be set to '1'. The chip select bits A_2 and A_1 in the control byte must match the logic levels on the corresponding A2 and A1 pins for the device to respond.

The last bit of the control byte defines the operation to be performed. When set to a '1' a read operation is selected, and when set to a '0' a write operation is selected.

The combination of the 4-bit op code and the three chip select bits is called the slave address. Upon receiving a valid slave address, the slave device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 47L64 will select a read or a write operation.

Note:	When VCAP is below VTRIP, the 47L64 cannot be accessed and will not acknowledge any commands.

FIGURE 4-3: CONTROL BYTE FORMAT



The 47L64 is divided into two functional units: the SRAM array and the Control registers. **Section 4.3 "SRAM Array"** describes the functionality for the SRAM array.

The 4-bit op code in the control byte determines which unit will be accessed during an operation. Table 4-2 shows the standard control bytes used by the 47L64.

TABLE 4-2: CONTROL BYTES

Operation	Op Code	Chip Select	R/$\overline{W}$ Bit
SRAM Read	1010	A_2 A_1 1	1
SRAM Write	1010	A_2 A_1 1	0

4.3 SRAM ARRAY

The SRAM array is the only user-accessible memory panel available on the 47L64. The EEPROM array, which can only be directly accessed through test mode operations, provides nonvolatile storage to back up the SRAM data.

To select the SRAM array, the master device must use the respective 4-bit op code, '1010', when transmitting the control byte.

Note: If an AutoStore is triggered during an SRAM read or write operation, the operation is aborted in order to execute the Store.

4.3.1 WRITE OPERATION

When the SRAM array is selected and the R/$\overline{W}$ bit in the control byte is set to '0', a write operation is selected and the next two bytes received are interpreted as the array address. The Most Significant address bits are transferred first, followed by the Least Significant bits, and are shifted directly into the internal Address Pointer. The Address Pointer determines where in the SRAM array the next read or write operation begins.

Data is stored into the SRAM array as soon as it is received, specifically on the rising edge of SCL during each Acknowledge bit. If a write operation is aborted for any reason, all received data will already be stored in SRAM, except for the last data byte if the rising edge of SCL during the Acknowledge for that byte has not yet been reached.

Note: If an attempt is made to write to a protected portion of the array, the device will not respond with an Acknowledge after the data byte is received, the current operation will be terminated without incrementing the Address Pointer, and any data transmitted on the SDA line will be ignored until a new operation is begun with a Start condition.

4.3.1.1 Byte Write

After the 47L64 has received the 2-byte array address, responding with an Acknowledge after each address byte, the master device will transmit the data byte to be written into the addressed memory location. The 47L64 acknowledges again and the master generates a Stop condition (Figure 4-4). The data byte is latched into the SRAM array on the rising edge of SCL during the Acknowledge.

After a byte write command, the internal Address Pointer will point to the address location following the location that was just written.

4.3.1.2 Sequential Write

To write multiple data bytes in a single operation, the SRAM write control byte, array address, and the first data byte are transmitted to the 47L64 in the same way as for a byte write. However, instead of generating a Stop condition, the master transmits additional data bytes (Figure 4-5). Upon receipt of each byte, the 47L64 responds with an Acknowledge, during which the data is latched into the SRAM array on the rising edge of SCL, and the Address Pointer is incremented by one. Sequential write operations are limited to the address 0x1FFF, and if the master should transmit enough bytes further, the Address Pointer will roll over to 0x0000 and continue writing. There is no limit to the number of bytes that can be written in a single command.

In the event that the WP pin is set high, writes to addresses in the upper 1/4 portion of the array will not be allowed. Attempts to write in that region will receive an ACK response from the device for the address bytes, but will receive a NACK for data bytes written (see Table 4-1).

FIGURE 4-4: SRAM BYTE WRITE

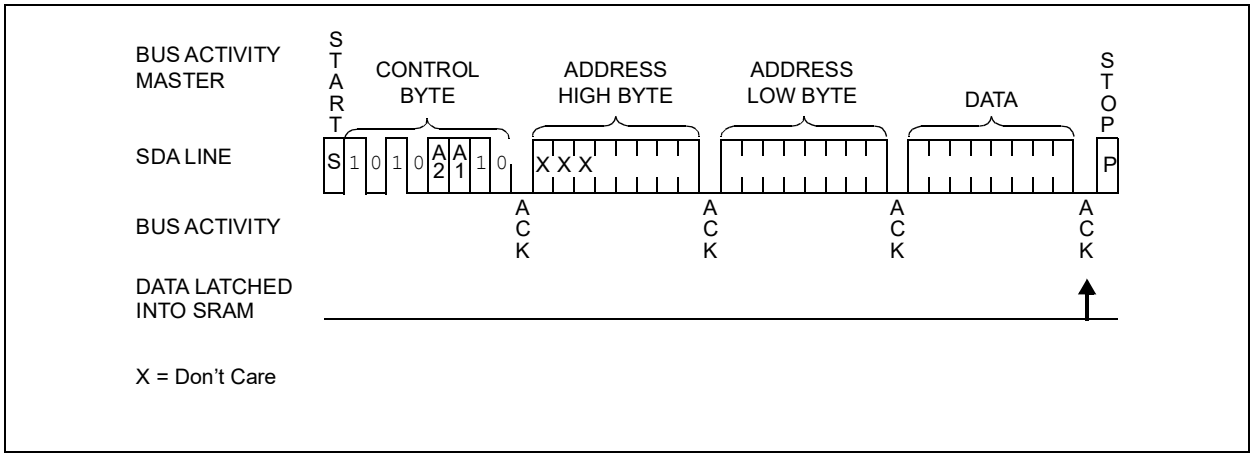
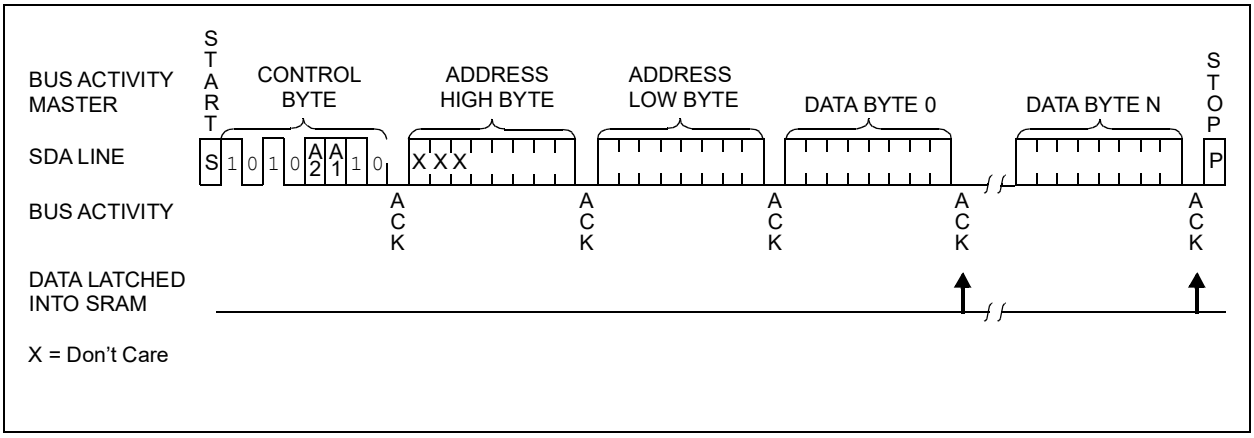


FIGURE 4-5: SRAM SEQUENTIAL WRITE



4.3.2 READ OPERATION

When the SRAM array is selected and the R/$\overline{W}$ bit is set to '1', a read operation is selected. For read operations, the array address is not transmitted, instead, the internal Address Pointer is used to determine where the read starts.

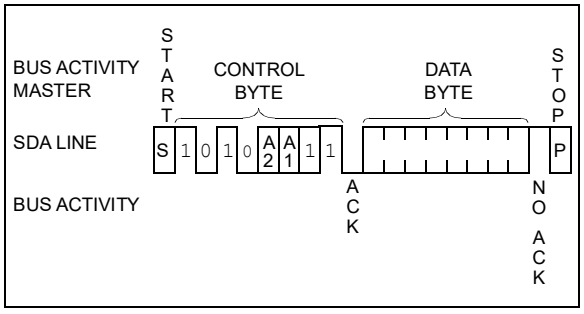
During read operations, the master device generates the Acknowledge bit after each data byte, and it is this bit which determines whether the operation will continue or end. A '0' (Acknowledge) bit requests more data and continues the read, while a '1' (No Acknowledge) bit ends the read operation.

4.3.2.1 Current Address Read

The current address read operation relies on the current value of the Address Pointer to determine from where to start reading. The Address Pointer is automatically incremented after each data byte is read or written. Therefore, if the previous access was to address n (where n is any legal address), the next current address read operation would access data beginning with address n+1.

Upon receipt of the control byte with the R/$\overline{W}$ bit set to '1', the 47L64 issues an Acknowledge and transmits the 8-bit data byte. The master will not acknowledge the transfer, but does generate a Stop condition and the 47L64 discontinues transmission (Figure 4-6).

FIGURE 4-6: SRAM CURRENT ADDRESS READ



4.3.2.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the Address Pointer must be set. This is done by sending the array address to the 47L64 as part of a write operation (R/$\overline{W}$ bit set to '0'). After the array address is sent, the master generates a Start condition following the Acknowledge. This terminates the write operation, but not before the Address Pointer has been set. Then, the master issues the SRAM control byte again but with the R/$\overline{W}$ bit set to a '1'. The 47L64 will then issue an Acknowledge and transmit the 8-bit data byte. The master will not Acknowledge the transfer but does generate a Stop condition, which causes the 47L64 to discontinue transmission (Figure 4-7). After a random read operation, the Address Pointer will point to the address location following the one that was just read.

4.3.2.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 47L64 transmits the first data byte, the master issues an Acknowledge as opposed to the Stop condition used in a random read. The Acknowledge directs the 47L64 to transmit the next sequentially addressed 8-bit byte (Figure 4-8). Following the final byte transmitted to the master, the master will NOT generate an Acknowledge but will generate a Stop condition. To provide sequential reads, the 47L64 increments the internal Address Pointer by one after the transfer of each data byte. This allows the entire memory contents to be serially read during one operation. The Address Pointer will automatically roll over at the end of the array to address 0x0000 after the last data byte in the array has been transferred.

FIGURE 4-7: SRAM RANDOM READ

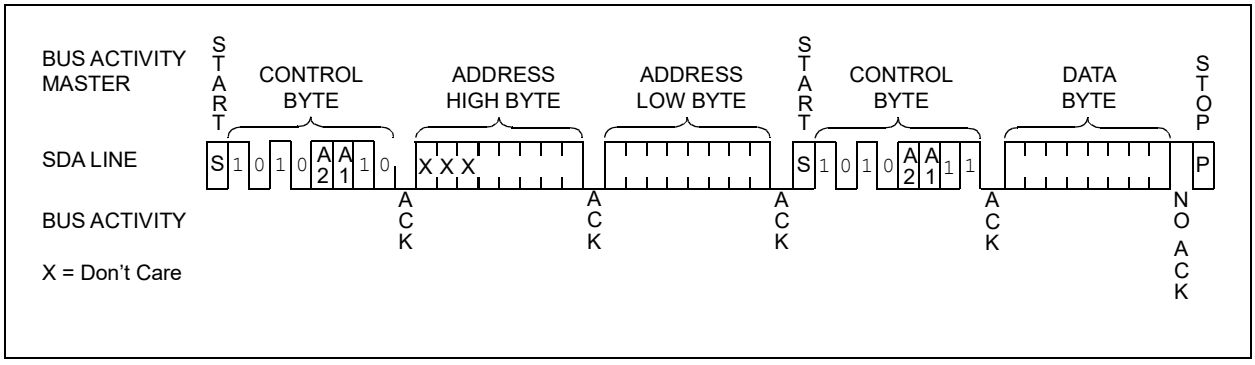
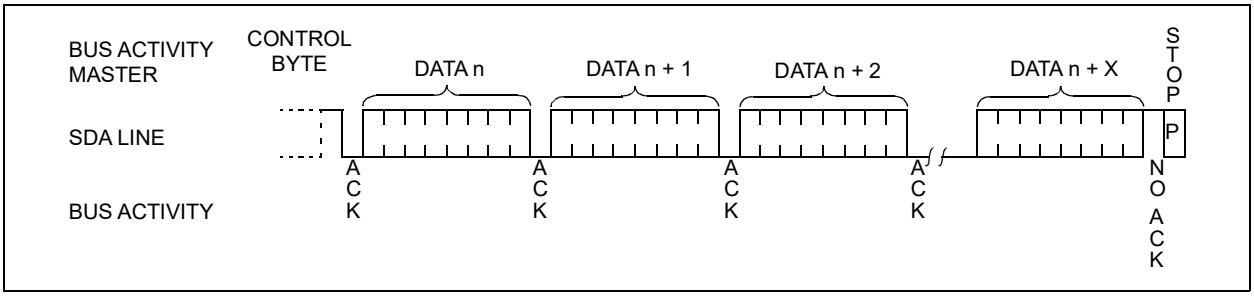


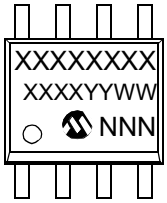
FIGURE 4-8: SRAM SEQUENTIAL READ



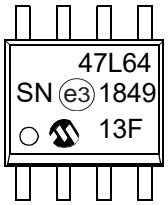
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

8-Lead SOIC (3.90 mm)



Example



8-Lead 2x3 TDFN

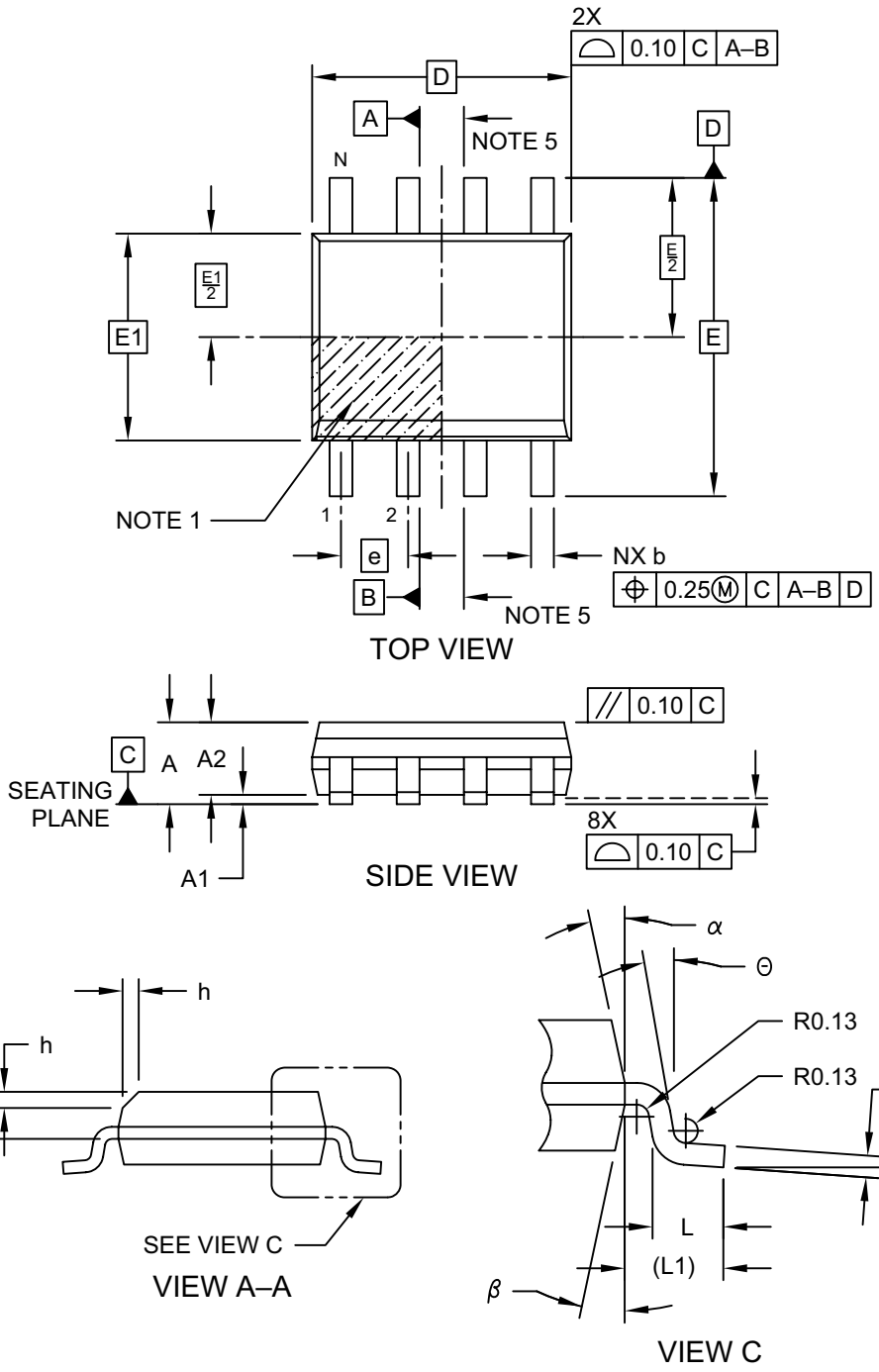
Example

1st Line Marking		
Part No.	**SOIC**	**TDFN**
47L64	47L64	EK4

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	JEDEC® designator for Matte Tin (Sn)

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

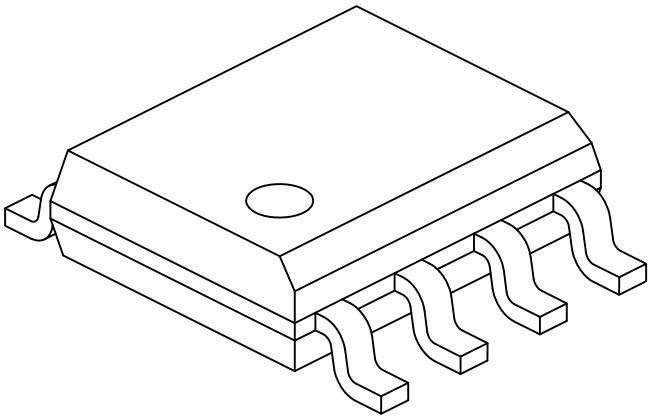
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev E Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

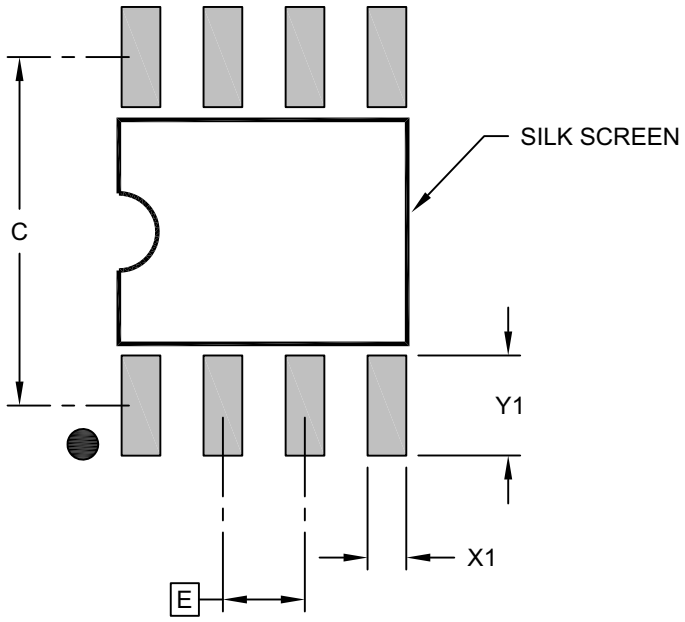
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev E Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

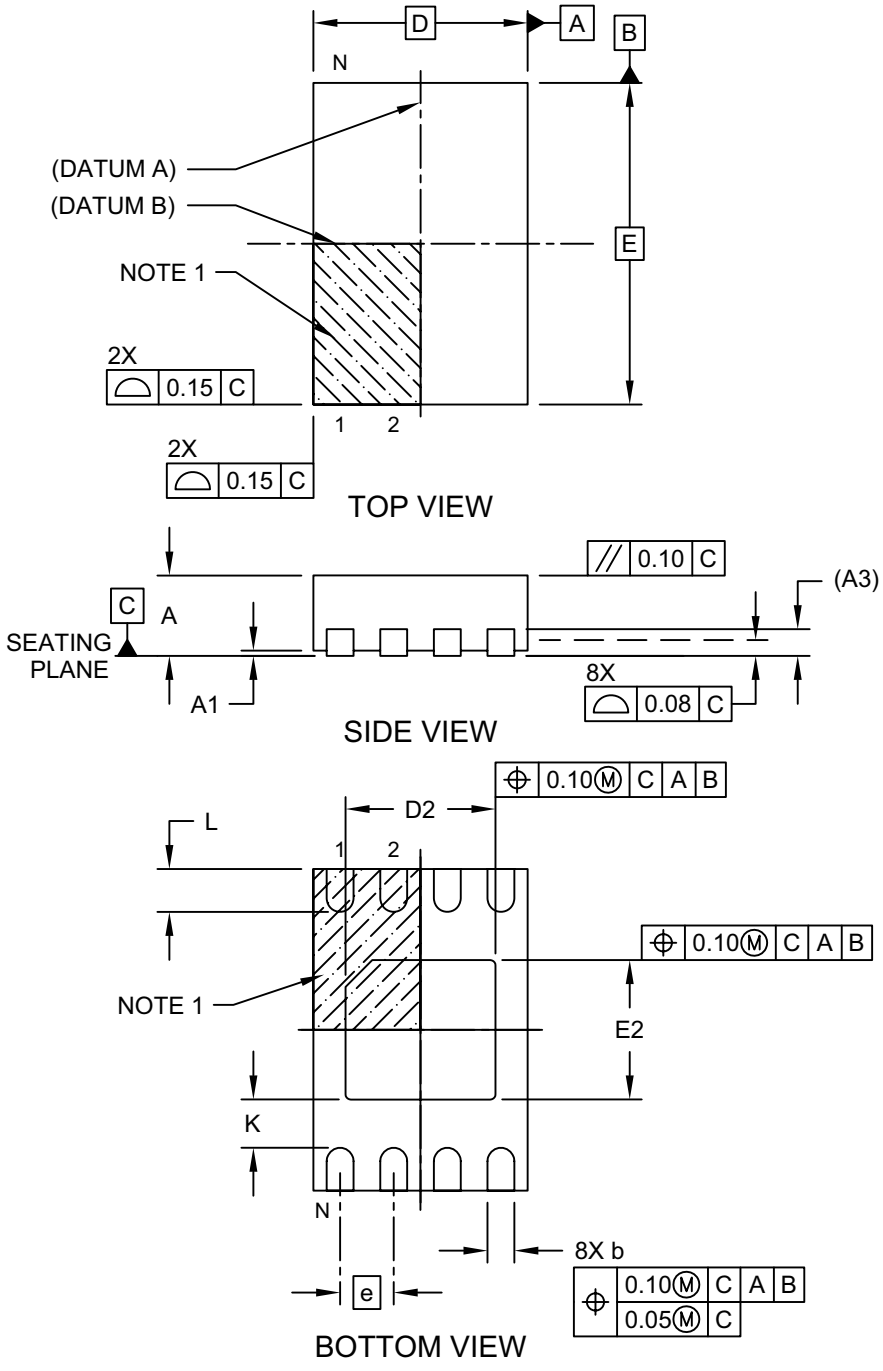
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev E

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN]
With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

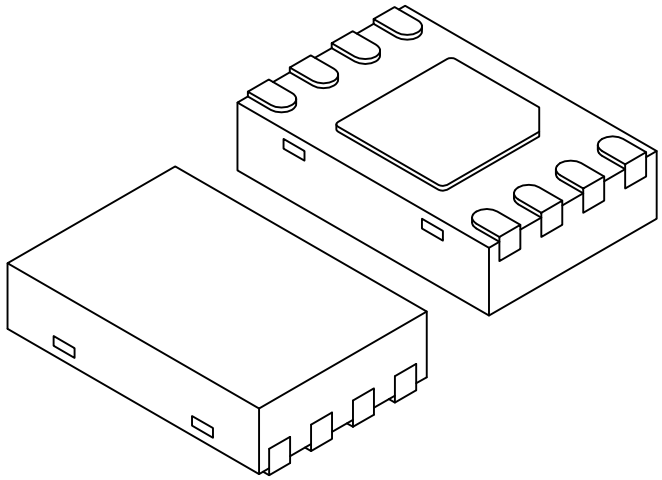
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-129-MN Rev E Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.35	1.40	1.45
Exposed Pad Width	E2	1.25	1.30	1.35
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

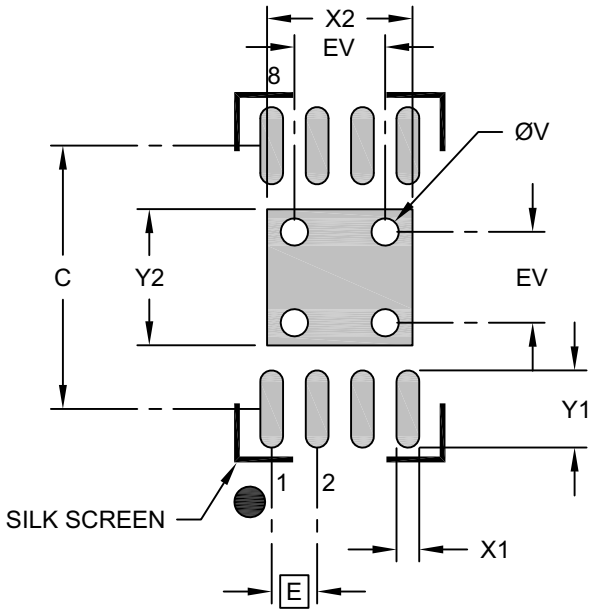
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129-MN Rev E Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			1.60
Optional Center Pad Length	Y2			1.50
Contact Pad Spacing	C		2.90	
Contact Pad Width (X8)	X1			0.25
Contact Pad Length (X8)	Y1			0.85
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing No. C04-129-MN Rev. B

APPENDIX A: REVISION HISTORY

Revision B (01/2020)

Updated V_{CAP} Capacitor values and Section 2.4 Write-Protect Input; Updated Section 4.1.1.5.

Revision A (03/2019)

Initial release of the document.

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PART NO.	[X](1)	X	/XX	XXX
Device	Tape and Reel Option	Temperature Range	Package	Pattern

Device:	47L64 = 64 Kbit I^2C EERAM	
Tape and Reel Option:	Blank = Standard packaging (tube or tray) T = Tape and Reel(1)	
Temperature Range:	I = -40°C to +85°C (Industrial)	
Package:	SN = Plastic Small Outline - Narrow, 3.90 mm Body, 8-lead (SOIC) MNY = Plastic Dual Flat, No Lead Package - 2x3x0.8 mm Body, 8-lead (TDFN)	

Examples:

a) 47L64T-I/SN = Tape and Reel, Industrial temp., SOIC package,

b) 47L64-I/SN = Industrial temp., SOIC package

c) 47L64T-I/MNY = Tape and Reel, Industrial temp., TDFN package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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