# MxFE Quad, 16-Bit, 12 GSPS RF DAC and Dual, 12-Bit, 6 GSPS RF ADC

Data Sheet **AD9082**

## FEATURES

- Flexible reconfigurable common platform design
  - 4 DACs and 2 ADCs (4D2A)
  - Supports single, dual, and quad band
  - Maximum DAC/ADC sample rate up to 12 GSPS/6 GSPS
    - DAC to ADC sample rate ratios of 1, 2, 3, and 4
    - ADC and DAC datapath bypass option
    - Analog bandwidth to 8 GHz
    - Full-scale output current range, ac coupling: 7 mA to 40 mA
  - On-chip PLL with multichip synchronization
    - External RFCLK input option
- ADC ac performance at 6 GSPS
  - Full-scale input voltage: 1.475 V p-p
  - Full-scale sine wave input power: 4.4 dBm
  - Noise density: −153 dBFS/Hz
  - Noise figure: 25.3 dB
  - HD2: −65.2 dBFS at 2.7 GHz
  - HD3: −70.8 dBFS at 2.7 GHz
  - Worst other (excluding HD2 and HD3): −68.5 dBFS at 2.7 GHz
- DAC ac performance at 3.7 GHz output
  - 2-tone IMD3 (−7 dBFS per tone): −78.9 dBc
  - NSD, single-tone, $f_{DAC}$ = 12 GSPS: −155.1 dBc/Hz
  - SFDR, single-tone, $f_{DAC}$ = 12 GSPS: −70 dBc
- Versatile digital features
  - Supports real or complex digital data (8-, 12-, 16-, or 24-bit)
  - Selectable interpolation and decimation filters
  - Configurable DDC and DUC
    - 8 fine complex DUCs and 4 coarse complex DUCs
    - 8 fine complex DDCs and 4 coarse complex DDCs
    - 48-bit NCO per DUC/DDC
    - Option to bypass fine and coarse DUC/DDC
  - Programmable 192-tap PFIR filter for receive equalization
    - Supports 4 different profile settings loaded via GPIO
  - Programable delay per data path
  - Receive AGC support
    - Fast detect with low latency for fast AGC control
    - Signal monitor for slow AGC control
    - Dedicated AGC support pins
  - Transmit DPD support
    - Fine DUC channel gain control and delay adjust
    - Coarse DDC delay adjust for DPD observation path
- Auxiliary features
  - Fast frequency hopping
  - Direct digital synthesis (DDS)
  - Low latency digital loopback mode (ADC to DAC)
  - ADC clock driver with selectable divide ratios
  - Power amplifier downstream protection circuitry
  - On-chip temperature monitoring unit
  - Flexible GPIOx pins
  - TDD power savings option
- SERDES JESD204B/JESD204C interface, 16 lanes up to 16.22 Gbps
  - 8 lanes per DACs and ADCs
  - JESD204B compatible with the maximum 15.5 Gbps lane rate
  - JESD204C compatible with the maximum 16.22 Gbps lane rate
  - Sample and bit repeat mode for lane rate matching
- Total power consumption: 11.45 W typical
- 15 mm × 15 mm, 324-ball BGA with 0.8 mm pitch

## APPLICATIONS

- Wireless communications infrastructure
- Microwave point-to-point, E-band and 5G mmWave
- Broadband communications systems
- DOCSIS 3.1 and 4.0 CMTS
- Phased array radar and electronic warfare
- Electronic test and measurement systems

## GENERAL DESCRIPTION

The mixed signal front-end (MxFE®) is a highly integrated device with a 16-bit, 12 GSPS maximum sample rate, RF digital-to-analog converter (DAC) core, and 12-bit, 6 GSPS rate, RF analog-to-digital converter (ADC) core. The AD9082 supports four transmitter channels and two receiver channels. The AD9082 is well suited for applications requiring both wideband ADCs and DACs to process signal(s) having wide instantaneous bandwidth. The device features a 16 lane, 16.22 Gbps JESD204C or 15.5 Gbps JESD204B data transceiver port, an on-chip clock multiplier, and a digital signal processing (DSP) capability targeted at either wideband or multiband, direct to RF applications. The AD9082 also features a bypass mode that allows the full bandwidth capability of the ADC and/or DAC cores to bypass the DSP datapaths. The device also features low latency loopback and frequency hopping modes targeted at phase array radar system and electronic warfare applications.

Rev. A Document Feedback


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## REVISION HISTORY

**9/2020—Rev. 0 to Rev. A**

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**6/2020—Revision 0: Initial Version**

# FUNCTIONAL BLOCK DIAGRAM

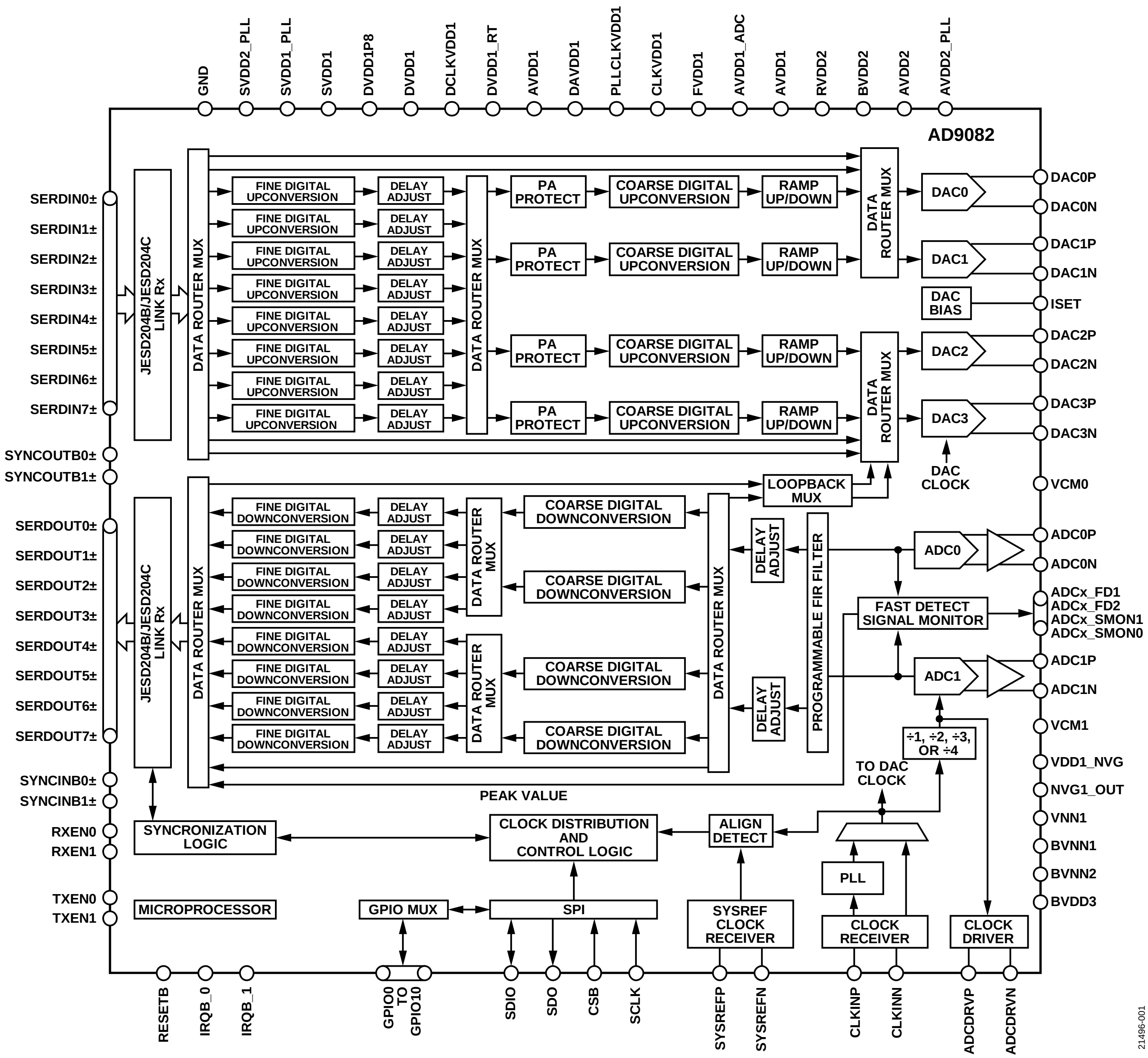



*Figure 1.*

# SPECIFICATIONS

## RECOMMENDED OPERATING CONDITIONS

Successful DAC calibration is required during the device initialization phase that occurs shortly after power-up to ensure long-term reliability of the DAC core circuitry. Refer to UG-1578, the device user guide, for more information on device initialization.

**Table 1.**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| OPERATING JUNCTION TEMPERATURE ($T_J$) | | | 120 | °C |
| ANALOG SUPPLY VOLTAGE RANGE | | | | |
| AVDD2, BVDD2, RVDD2 | 1.9 | 2.0 | 2.1 | V |
| AVDD1, AVDD1_ADC, CLKVDD1, FVDD1, VDD1_NVG1 | 0.95 | 1.0 | 1.05 | V |
| DIGITAL SUPPLY VOLTAGE RANGE | | | | |
| DVDD1, DVDD1_RT, DCLKVDD1, DAVDD1 | 0.95 | 1.0 | 1.05 | V |
| DVDD1P8 | 1.7 | 1.8 | 2.1 | V |
| SERIALIZER/DESERIALIZER (SERDES) SUPPLY VOLTAGE RANGE | | | | |
| SVDD2_PLL | 1.9 | 2.0 | 2.1 | V |
| SVDD1, SVDD1_PLL | 0.95 | 1.0 | 1.05 | V |

## DC SPECIFICATIONS

Nominal supplies with DAC output full-scale current ($I_{OUTFS}$) = 26 mA, unless otherwise noted. For the minimum and maximum values, $T_J$ = −40°C to +120°C, and for the typical values, $T_A$ = 25°C, unless otherwise noted.

**Table 2.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DAC RESOLUTION | | 16 | | | Bit |
| ADC RESOLUTION | | 12 | | | Bit |
| DAC ACCURACY | | | | | |
| Gain Error | | | 1.5 | | %FSR |
| Gain Matching | | | 0.1 | | %FSR |
| Integral Nonlinearity (INL) | Shuffling disabled | | 8.0 | | LSB |
| Differential Nonlinearity (DNL) | Shuffling disabled | | 3.5 | | LSB |
| ADC ACCURACY | | | | | |
| No Missing Codes | | | Guaranteed | | |
| Offset Error | | | 0.57 | | %FSR |
| Offset Matching | | | 0.26 | | %FSR |
| Gain Error | | | 5.34 | | %FSR |
| Gain Matching | | | 1.06 | | %FSR |
| DNL | Dithering enabled | | 0.32 | | LSB |
| INL | Dithering enabled | | 1.38 | | LSB |
| DAC ANALOG OUTPUTS | DACxP and DACxN | | | | |
| Full-Scale Output Current Range | AC coupling, setting resistance ($R_{SET}$) = 5 kΩ | | | | |
| AC Coupling | Output common-mode voltage ($V_{CM}$) = 0 V | 7 | 26 | 40 | mA |
| DC Coupling | $V_{CM}$ = 0.3 V | | 20 | | mA |
| Full-Scale Sinewave Output Power with AC Coupling[1] | Ideal 2:1 balun interface to 50 Ω | | | | |
| $I_{OUTFS}$ = 26 mA | | | 3.3 | | dBm |
| $I_{OUTFS}$ = 40 mA | | | 7 | | dBm |
| Common-Mode Output Voltage ($VCM_{OUT}$) | | | 0 | | V |
| Differential Impedance | | | 100 | | Ω |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ADC ANALOG INPUTS | ADCxP and ADCxN | | | | |
| Differential Input Voltage | | | 1.475 | | V p-p |
| Full-Scale Sine Wave Input Power | Input power level resulting 0 dBFS tone level on fast Fourier transform (FFT) | | 4.4 | | dBm |
| Common-Mode Input Voltage ($VCM_{IN}$) | AC-coupled, equal to voltage at VCMx for ADCx input | | 1 | | V |
| Differential Input | | | | | |
| Resistance | | | 100 | | Ω |
| Capacitance | | | 0.4 | | pF |
| Return Loss | <2.7 GHz | | −4.3 | | dB |
| | 2.7 GHz to 3.8 GHz | | −3.6 | | dB |
| | 3.8 GHz to 5.4 GHz | | −2.9 | | dB |
| CLOCK INPUTS | CLKINP and CLKINN | | | | |
| Differential Input Power | | | | | |
| Direct RF Clock | | | 0 | | dBm |
| CLK Synchronization Enabled | | | 0 | | dBm |
| Differential Input Impedance[1] | | | 100//0.3 | | Ω//pF |
| Common-Mode Voltage | AC coupled | | 0.5 | | V |
| ADC CLOCK OUTPUTS | ADCDRVP and ADCDRVN | | | | |
| Differential Output Voltage Magnitude[2] | 1.5 GHz | | 740 | | mV p-p |
| | 2.0 GHz | | 690 | | mV p-p |
| | 3 GHz | | 640 | | mV p-p |
| | 6 GHz | | 490 | | mV p-p |
| Differential Output Resistance | | | 100 | | Ω |
| Common-Mode Voltage | AC coupled | | 0.5 | | V |

[1] The actual measured full-scale power is frequency dependent due to DAC sinc response, impedance mismatch loss, and balun insertion loss.
[2] Measured with differential 100 Ω load and less than 2 mm of printed circuit board (PCB) trace from package ball.

## DAC AND ADC SAMPLING SPECIFICATIONS

Nominal supplies. For the minimum and maximum values, $T_J$ = −40°C to +120°C and ±5% of nominal supply. For the typical values, $T_A$ = 25°C, unless otherwise noted.

**Table 3.**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| DAC UPDATE RATE[1] | | | | |
| Minimum | | | 2.9 | GSPS |
| Maximum | 12 | | | GSPS |
| ADC SAMPLE RATE[1] | | | | |
| Minimum | | | 1.45 | GSPS |
| Maximum | 6 | | | GSPS |
| Aperture Jitter[2] | | 65 | | fs rms |

[1] Pertains to the update rate of the DAC and ADC cores independent of datapath and JESD mode configuration.
[2] Measured using a signal-to-noise ratio (SNR) degradation method with the DAC disabled, clock divider = 1, ADC frequency ($f_{ADC}$) = 6 GSPS, and input frequency ($f_{IN}$) = 5.55 GHz.

## POWER CONSUMPTION

Typical at nominal supplies and maximum at 5% supplies. DAC datapath with a complex I/Q data rate frequency ($f_{IQ\_DATA}$) = 375 MSPS and DAC frequency ($f_{DAC}$) of 12 GSPS with interpolate by 32× with JRx mode of 16B (L = 8, M = 16). ADC datapath with $f_{IQ\_DATA}$ = 375 MSPS and $f_{ADC}$ of 6 GSPS with decimate by 16× with JTx mode of 17B (L = 8, M = 16). For the minimum and maximum values, $T_J$ = −40°C to +120°C. For the typical values, $T_A$ = 25°C, unless otherwise noted.

See the UG-1578 user guide for further information on the JESDB or JESDC mode configurations and detailed settings referred to throughout this data sheet.

**Table 4.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| CURRENTS | | | | | |
| AVDD2 ($I_{AVDD2}$) | 2.0 V supply | | 190 | | |
| BVDD2 ($I_{BVDD2}$) + RVDD2 ($I_{RVDD2}$) | 2.0 V supply | | 292 | | mA |
| AVDD2_PLL ($I_{AVDD2\_PLL}$) + SVDD2_PLL ($I_{SVDD2\_PLL}$) | 2.0 V supply | | 44 | | mA |
| Power Dissipation for 2 V Supplies | 2.0 V supply total power dissipation | | 1.05 | | W |
| PLLCLKVDD1 ($I_{PLLCLKVDD1}$) | 1.0 V supply | | 43 | | mA |
| AVDD1 ($I_{AVDD1}$) + DCLKVDD1($I_{DCLKVDD1}$) | 1.0 V supply | | 1541 | | mA |
| AVDD1_ADC ($I_{AVDD1\_ADC}$) | 1.0 V supply | | 1700 | | mA |
| CLKVDD1 ($I_{CLKVDD1}$) | 1.0 V supply | | 96 | | mA |
| FVDD1 ($I_{FVDD1}$) | 1.0 V supply | | 72.5 | | mA |
| VDD1_NVG ($I_{VDD1\_NVG}$) | 1.0 V supply | | 290 | | mA |
| DAVDD1 ($I_{DAVDD1}$) | 1.0 V supply | | 985 | | mA |
| DVDD1 ($I_{DVDD1}$) | 1.0 V supply | | 3555 | | mA |
| DVDD1_RT ($I_{DVDD1\_RT}$) | 1.0 V supply | | 461 | | mA |
| SVDD1 ($I_{SVDD1}$) + SVDD1_PLL ($I_{SVDD1\_PLL}$) | 1.0 V supply | | 1626 | | mA |
| Power Dissipation for 1 V Supplies | 1.0 V supply total power dissipation | | 10.4 | | W |
| DVDD1P8 ($I_{DVDD1P8}$) | 1.8 V supply | | 6.8 | | mA |
| Total Power Dissipation | Total power dissipation of 2 and 1 V supplies | | 11.45 | | W |

## CLOCK INPUT AND PHASE-LOCKED LOOP (PLL) FREQUENCY SPECIFICATIONS

For the minimum and maximum values, $T_J$ = −40°C to +120°C and ±5% of nominal supply, unless otherwise noted.

**Table 5.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| PLL VOLTAGE CONTROLLED OSCILLATOR (VCO) FREQUENCY RANGES | | | | | |
| VCO Output | | | | | |
| Divide by 1 | | 6 | | 12 | GSPS |
| Divide by 2 | | 3 | | 6 | GSPS |
| Divide by 4 | | 1.5 | | 3 | GSPS |
| PHASE FREQUENCY DETECT INPUT FREQUENCY RANGES | | 25 | | 750 | MHz |
| CLOCK INPUTS (CLKINP, CLKINN) FREQUENCY RANGES | | | | | |
| PLL Off | | 1.45 | | 12 | GHz |
| PLL On | M divider set to divide by 1 | 25 | | 750 | MHz |
| | M divider set to divide by 2 | 50 | | 1500 | MHz |
| | M divider set to divide by 3 | 75 | | 2250 | MHz |
| | M divider set to divide by 4 | 100 | | 3000 | MHz |

## INPUT AND OUTPUT DATA RATES AND SIGNAL BANDWIDTH SPECIFICATIONS

For the minimum and maximum values, $T_J$ = −40°C to +120°C and ±5% of nominal supply, unless otherwise noted.

**Table 6.**

| Parameter[1] | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DATA RATE PER INPUT CHANNEL | | | | | |
| | Channel datapaths bypassed (1× interpolation), single DAC mode only, 16-bit resolution (JR mode = 19C) | | | 12,000 | MSPS |
| | Channel datapaths bypassed (1× interpolation), dual DAC or dual ADC, 16-bit resolution (JRxmode = 18C and JTx mode = 28C) | | | 6000 | MSPS |
| | Channel datapaths bypassed (1× interpolation), quad DAC mode , 12-bit resolution (JRx mode = 35C) | | | 4000 | MSPS |
| | 1 complex channel enabled, 16-bit resolution (JRx mode = 18C and JTx mode = 19C) | | | 6000 | MSPS |
| | 2 complex channels enabled, 12-bit resolution (JRx mode = 23C and JTx mode = 27C) | | | 4000 | MSPS |
| | 4 complex channels enabled, 12-bit resolution (JRx mode = 24C and JTx mode = 26C) | | | 2000 | MSPS |
| | 8 complex channels enabled, 16-bit resolution (JRx mode = 16C and JTx mode = 16C) | | | 750 | MSPS |
| COMPLEX SIGNAL BANDWIDTH PER CHANNEL | | | | | |
| | 1 complex channel enabled (0.8 × data frequency ($f_{DATA}$)) | | | 4800 | MHz |
| | 2 complex channels enabled (0.8 × $f_{DATA}$) | | | 3200 | MHz |
| | 4 complex channels enabled (0.8 × $f_{DATA}$) | | | 1600 | MHz |
| | 8 complex channels enabled (0.8 × $f_{DATA}$) | | | 600 | MHz |
| MAXIMUM NUMERICALLY CONTROLLED OSCILLATOR (NCO) CLOCK RATE | | | | | |
| Channel NCO | | | | 1500 | MHz |
| Main DAC NCO | | | | 12 | GHz |
| Main ADC NCO | | | | 6 | GHz |
| MAXIMUM NCO SHIFT FREQUENCY RANGE | | | | | |
| Channel NCO | Channel summing node = 1.5 GHz, channel interpolation rate > 1× | −750 | | +750 | MHz |
| Main DAC NCO | $f_{DAC}$ = 12 GHz, main interpolation rate > 1× | −6 | | +6 | GHz |
| Main ADC NCO | $f_{ADC}$ = 6 GHz, main decimation rate > 1× | −3 | | +3 | GHz |
| MAXIMUM FREQUENCY SPACING ACROSS INPUT CHANNELS | Maximum NCO output frequency × 0.8 | | | 1200 | MHz |

[1] The values listed for these parameters are the maximum possible when considering all JESD204B modes of operation. Some modes are more limiting, based on other parameters.

## JESD204B AND JESD204C INTERFACE ELECTRICAL AND SPEED SPECIFICATIONS

Nominal supplies. For the minimum and maximum values, $T_J$ = −40°C to +120°C and ±5% of nominal supply, and for the typical values, $T_A$ = 25°C, unless otherwise noted.

**Table 7.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| JESD204B SERIAL INTERFACE RATE | Serial lane rate (bit repeat option disabled) | 8.11 | | 15.5 | Gbps |
| Unit Interval | | 168.35 | | 64.5 | ps |
| JESD204C SERIAL INTERFACE RATE | Serial lane rate (bit repeat option disabled) | 8.11 | | 16.22 | Gbps |
| Unit Interval | | 123.3 | | 61.65 | ps |
| JESD204x DATA INPUTS | SERDINx±, where x = 0 to 7 | | | | |
| Differential Voltage, $R_{VDIFF}$ | | | 800 | | mV p-p |
| Differential Impedance, $Z_{RDIFF}$ | At dc | | 98 | | Ω |
| Termination Voltage, $V_{TT}$ | AC-coupled | | 0.97 | | V |
| JESD204x DATA OUTPUTS | SERDOUTx±, where x = 0 to 7 | | | | |
| Logic Compliance | | | JESD204B/JESD204C compliant | | |
| Differential Output Voltage | Maximum strength | | 675 | | mV p-p |
| Differential Termination Impedance | | 80 | 108 | 120 | Ω |
| Rise Time, $t_R$ | 20% to 80% into 100 Ω load | | 18 | | ps |
| Fall Time, $t_F$ | 20% to 80% into 100 Ω load | | 18 | | ps |
| SYSREFP AND SYSREFN INPUTS | | | | | |
| Logic Compliance | | | LVDS/LVPECL[1] | | |
| Differential Input Voltage | | | 0.7 | 1.9 | V p-p |
| Input Common-Mode Voltage Range | DC-coupled | | 0.675 | 2 | V |
| Input Reference, $R_{IN}$ (Differential) | | | 100 | | Ω |
| Input Capacitance (Differential) | | | 1 | | pF |
| SYNCxOUTB± OUTPUTS[2] | Where x = 0 or1 | | | | |
| Output Differential Voltage, $V_{OD}$ | Driving 100 Ω differential load | | 400 | | mV |
| Output Offset Voltage, $V_{OS}$ | | | DVDD1P8/2 | | V |
| SYNCxOUTB+ | CMOS output option | | Refer to CMOS pin specification | | |
| SYNCxINB± INPUT[2] | Where x = 0 or1 | | | | |
| Logic Compliance | | | LVDS | | |
| Differential Input Voltage | | | 0.7 | 1.9 | mV p-p |
| Input Common-Mode Voltage | DC-coupled | | 0.675 | 2 | V |
| $R_{IN}$ (Differential) | 18 | | 18 | | kΩ |
| Input Capacitance (Differential) | 1 | | 1 | | pF |
| SYNCxINB+ INPUT | CMOS input option | | Refer to CMOS pin specification | | |

[1] LVDS means low voltage differential signaling and LVPECL means low voltage positive/pseudo emitter-coupled logic.
[2] IEEE 1596.3 Standard LVDS compatible.

## CMOS PIN SPECIFICATIONS

Nominal supplies. For the minimum and maximum values, $T_J$ = −40°C to +120°C and DVDD1P8 = 2.0 V ± 5%, and for the typical values, $T_A$ = 25°C, unless otherwise noted.

**Table 8.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| INPUTS | | SDIO, SCLK, CSB, RESETB, RXEN0, RXEN1, TXEN0, TXEN1, SYNC0INB±, SYNC1INB±, and GPIOx | | | | |
| Logic 1 Voltage | $V_{IH}$ | | 0.70 × DVDD1P8 | | | V |
| Logic 0 Voltage | $V_{IL}$ | | | | 0.3 × DVDD1P8 | V |
| Input Resistance | | | | 30 | | kΩ |
| OUTPUTS | | SDIO, SDO, GPIOx, ADCx_FDx, SYNC0INB±, and SYNC1INB±, 4 mA load | | | | |
| Logic 1 Voltage | $V_{OH}$ | | DVDD1P8 − 0.45 | | | V |
| Logic 0 Voltage | $V_{OL}$ | | | | 0.45 | V |
| INTERRUPT OUTPUTS | | IRQB_0 and IRQB_1, pull-up resistor of 5 kΩ | | | | |
| Logic 1 Voltage | $V_{OH}$ | | 1.45 | | | V |
| Logic 0 Voltage | $V_{OL}$ | | | | 0.35 | V |

## DAC AC SPECIFICATIONS

Nominal supplies with $T_A$ = 25°C. $f_{IQ\_DATA}$ = 1500 MSPS. Specifications represent the average of all four DAC channels with the DAC $I_{OUTFS}$ = 26 mA and ADC powered down, unless otherwise noted.

**Table 9.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SPURIOUS-FREE DYNAMIC RANGE (SFDR) | | | | | |
| Single-Tone, $f_{DAC}$ = 12 GSPS | −7 dBFS, shuffle enabled | | | | |
| Output Frequency ($f_{OUT}$) = 100 MHz | | | −70.7 | | dBc |
| $f_{OUT}$ = 500 MHz | | | −69.2 | | dBc |
| $f_{OUT}$ = 900 MHz | | | −69.7 | | dBc |
| $f_{OUT}$ = 1900 MHz | | | −68.5 | | dBc |
| $f_{OUT}$ = 2600 MHz | | | −73.1 | | dBc |
| $f_{OUT}$ = 3700 MHz | | | −70 | | dBc |
| $f_{OUT}$ = 4500 MHz | | | −66.5 | | dBc |
| Single-Tone, $f_{DAC}$ = 9 GSPS | −7 dBFS, shuffle enabled | | | | |
| $f_{OUT}$ = 100 MHz | | | −74.4 | | dBc |
| $f_{OUT}$ = 500 MHz | | | −72.5 | | dBc |
| $f_{OUT}$ = 900 MHz | | | −72.50 | | dBc |
| $f_{OUT}$ = 1900 MHz | | | −71.0 | | dBc |
| $f_{OUT}$ = 2600 MHz | | | −71.5 | | dBc |
| $f_{OUT}$ = 3700 MHz | | | −69.1 | | dBc |
| Single-Tone, $f_{DAC}$ = 6 GSPS | −7 dBFS, shuffle enabled | | | | |
| $f_{OUT}$ = 100 MHz | | | −77 | | dBc |
| $f_{OUT}$ = 500 MHz | | | −75.8 | | dBc |
| $f_{OUT}$ = 900 MHz | | | −75.3 | | dBc |
| $f_{OUT}$ = 1900 MHz | | | −75.3 | | dBc |
| SINGLE-BAND APPLICATION, BAND 3 | $f_{DAC}$ =9 GSPS, 500 MHz reference clock | | | | |
| Windowed SFDR Nonharmonics | −7 dBFS, shuffle enabled | | | | |
| In Band | 1842.5 MHz ± 37.5 MHz pass-band region | | −95.5 | | dBc |
| DPD Band | 1842.5 MHz, ± 200 MHz pass-band region | | −80.3 | | dBc |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ADJACENT CHANNEL LEAKAGE RATIO | | | | | |
| Single Carrier 20 MHz LTE Downlink Test Vector | −1 dBFS digital back off, 256QAM | | | | |
| $f_{DAC}$ = 12 GSPS | $f_{OUT}$ = 1840 MHz | | 77.3 | | dBc |
| | $f_{OUT}$ = 2650 MHz | | 76.3 | | dBc |
| | $f_{OUT}$ = 3500 MHz | | 73.3 | | dBc |
| $f_{DAC}$ = 9 GSPS | $f_{OUT}$ = 1900 MHz | | 77.0 | | dBc |
| | $f_{OUT}$ = 2650 MHz | | 77.1 | | dBc |
| $f_{DAC}$ = 6 GSPS | $f_{OUT}$ = 750 MHz | | 78.8 | | dBc |
| | $f_{OUT}$ = 1840 MHz | | 77.3 | | dBc |
| THIRD-ORDER INTERMODULATION DISTORTION (IMD3) | Two tone test, −6 dBFS per tone, 1 MHz spacing | | | | |
| $f_{DAC}$ = 12 GSPS | $f_{OUT}$ = 1900 MHz | | −74.5 | | dBc |
| | $f_{OUT}$ = 2600 MHz | | −75.5 | | dBc |
| | $f_{OUT}$ = 3700 MHz | | −77 | | dBc |
| $f_{DAC}$ = 9 GSPS | $f_{OUT}$ = 1900 MHz | | −83 | | dBc |
| | $f_{OUT}$ = 2600 MHz | | −86 | | dBc |
| $f_{DAC}$ = 6 GSPS | $f_{OUT}$ = 900 MHz | | −88.4 | | dBc |
| | $f_{OUT}$ = 1900 MHz | | −86.3 | | dBc |
| NOISE SPECTRAL DENSITY (NSD) | 0 dBFS, NSD measurement taken at 10% away from $f_{OUT}$, shuffle off | | | | |
| Single-Tone, $f_{DAC}$ = 12 GSPS | | | | | |
| $f_{OUT}$ = 150 MHz | | | −168 | | dBc/Hz |
| $f_{OUT}$ = 500 MHz | | | −166.7 | | dBc/Hz |
| $f_{OUT}$ = 950 MHz | | | −164.8 | | dBc/Hz |
| $f_{OUT}$ = 1840 MHz | | | −161.6 | | dBc/Hz |
| $f_{OUT}$ = 2650 MHz | | | −160 | | dBc/Hz |
| $f_{OUT}$ = 3700 MHz | | | −155.1 | | dBc/Hz |
| $f_{OUT}$ = 4500 MHz | | | −154.2 | | dBc/Hz |
| Single-Tone, $f_{DAC}$ = 9 GSPS | | | | | |
| $f_{OUT}$ = 150 MHz | | | −168 | | dBc/Hz |
| $f_{OUT}$ = 500 MHz | | | −166 | | dBc/Hz |
| $f_{OUT}$ = 950 MHz | | | −164 | | dBc/Hz |
| $f_{OUT}$ = 1840 MHz | | | −160.2 | | dBc/Hz |
| $f_{OUT}$ = 2650 MHz | | | −158.4 | | dBc/Hz |
| $f_{OUT}$ = 3700 MHz | | | −153.5 | | dBc/Hz |
| Single-Tone, $f_{DAC}$ = 6 GSPS | | | | | |
| $f_{OUT}$ = 150 MHz | | | −168 | | dBc/Hz |
| $f_{OUT}$ = 500 MHz | | | −165 | | dBc/Hz |
| $f_{OUT}$ = 950 MHz | | | −163 | | dBc/Hz |
| $f_{OUT}$ = 1840 MHz | | | −159 | | dBc/Hz |
| $f_{OUT}$ = 2650 MHz | | | −156.8 | | dBc/Hz |
| SINGLE SIDEBAND PHASE NOISE OFFSET (PLL DISABLED) | Direct RF clock input at 7 dBm | | | | |
| $f_{OUT}$ = 3 GHz, $f_{DAC}$ = 12 GSPS, CLKINx Frequency ($f_{CLKIN}$) = 12 GHz | R&S SMA100B B711 option | | | | |
| 1 kHz | | | −119 | | dBc/Hz |
| 10 kHz | | | −129 | | dBc/Hz |
| 100 kHz | | | −136 | | dBc/Hz |
| 600 kHz | | | −146 | | dBc/Hz |
| 1.2 MHz | | | −148 | | dBc/Hz |
| 1.8 MHz | | | −150 | | dBc/Hz |
| 6 MHz | | | −154 | | dBc/Hz |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SINGLE SIDEBAND PHASE NOISE OFFSET (PLL ENABLED) | Loop filter component values include C1 = 22 nF, R1 = 226 Ω, C2 = 2.2 nF, C3 = 33 nF, and phase detector frequency (PFD) = 500 MHz | | | | |
| $f_{OUT}$ = 1.8 GHz, $f_{DAC}$ = 12 GSPS, $f_{CLKIN}$ = 0.5 GHz | | | | | |
| 1 kHz | | | −103 | | dBc/Hz |
| 10 kHz | | | −111 | | dBc/Hz |
| 100 kHz | | | −119 | | dBc/Hz |
| 600 kHz | | | −127 | | dBc/Hz |
| 1.2 MHz | | | −132 | | dBc/Hz |
| 1.8 MHz | | | −137 | | dBc/Hz |
| 6 MHz | | | −148 | | dBc/Hz |

## ADC AC SPECIFICATIONS

Nominal supplies with $T_A$ = 25°C. Input amplitude ($A_{IN}$) = −1 dBFS, full bandwidth (no decimation) with dual link JTx mode of 13C. Specifications represent worst measured of any ADC channel with DACs powered down. See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.

**Table 10.**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| NOISE DENSITY[1] | | −153 | | dBFS/Hz |
| NOISE FIGURE[2] | | 25.3 | | dB |
| SIGNAL-TO-NOISE RATIO (SNR) | | | | |
| $f_{IN}$ = 253 MHz | | 56.7 | | dBFS |
| $f_{IN}$ = 450 MHz | | 56.9 | | dBFS |
| $f_{IN}$ = 900 MHz | | 56.2 | | dBFS |
| $f_{IN}$ = 1800 MHz | | 54.7 | | dBFS |
| $f_{IN}$ = 2700 MHz | | 52.4 | | dBFS |
| $f_{IN}$ = 3600 MHz | | 51.8 | | dBFS |
| $f_{IN}$ = 4500 MHz | | 50.4 | | dBFS |
| $f_{IN}$ = 5400 MHz | | 51.0 | | dBFS |
| SIGNAL-TO-NOISE-AND-DISTORTION (SINAD) RATIO | | | | |
| $f_{IN}$ = 253 MHz | | 56.6 | | dBFS |
| $f_{IN}$ = 450 MHz | | 56.6 | | dBFS |
| $f_{IN}$ = 900 MHz | | 55.7 | | dBFS |
| $f_{IN}$ = 1800 MHz | | 53.9 | | dBFS |
| $f_{IN}$ = 2700 MHz | | 52.0 | | dBFS |
| $f_{IN}$ = 3600 MHz | | 51.3 | | dBFS |
| $f_{IN}$ = 4500 MHz | | 49.6 | | dBFS |
| $f_{IN}$ = 5400 MHz | | 48.9 | | dBFS |
| EFFECTIVE NUMBER OF BITS (ENOB) | | | | |
| $f_{IN}$ = 253 MHz | | 9.1 | | Bits |
| $f_{IN}$ = 450 MHz | | 9.1 | | Bits |
| $f_{IN}$ = 900 MHz | | 9 | | Bits |
| $f_{IN}$ = 1800 MHz | | 8.7 | | Bits |
| $f_{IN}$ = 2700 MHz | | 8.3 | | Bits |
| $f_{IN}$ = 3600 MHz | | 8.2 | | Bits |
| $f_{IN}$ = 4500 MHz | | 7.9 | | Bits |
| $f_{IN}$ = 5400 MHz | | 7.8 | | Bits |
| WORST HD2 | | | | |
| $f_{IN}$ = 253 MHz | | −72.1 | | dBFS |
| $f_{IN}$ = 450 MHz | | −68.9 | | dBFS |
| $f_{IN}$ = 900 MHz | | −67.1 | | dBFS |
| $f_{IN}$ = 1800 MHz | | −64.6 | | dBFS |
| $f_{IN}$ = 2700 MHz | | −65.2 | | dBFS |
| $f_{IN}$ = 3600 MHz | | −58.1 | | dBFS |
| $f_{IN}$ = 4500 MHz | | −65 | | dBFS |
| $f_{IN}$ = 5400 MHz | | −54.1 | | dBFS |

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| WORST HD3 | | | | |
| $f_{IN}$ = 253 MHz | | −80.0 | | dBFS |
| $f_{IN}$ = 450 MHz | | −78.3 | | dBFS |
| $f_{IN}$ = 900 MHz | | −70.8 | | dBFS |
| $f_{IN}$ = 1800 MHz | | −66 | | dBFS |
| $f_{IN}$ = 2700 MHz | | −70.8 | | dBFS |
| $f_{IN}$ = 3600 MHz | | −69.2 | | dBFS |
| $f_{IN}$ = 4500 MHz | | −64.3 | | dBFS |
| $f_{IN}$ = 5400 MHz | | −62 | | dBFS |
| WORST OTHER, EXCLUDING HD2 OR HD3 HARMONIC | | | | |
| $f_{IN}$ = 253 MHz | | −85.3 | | dBFS |
| $f_{IN}$ = 450 MHz | | −81.4 | | dBFS |
| $f_{IN}$ = 900 MHz | | −76.5 | | dBFS |
| $f_{IN}$ = 1800 MHz | | −72.1 | | dBFS |
| $f_{IN}$ = 2700 MHz | | −68.5 | | dBFS |
| $f_{IN}$ = 3600 MHz | | −65.9 | | dBFS |
| $f_{IN}$ = 4500 MHz | | −64.2 | | dBFS |
| $f_{IN}$ = 5400 MHz | | −62.7 | | dBFS |
| TWO-TONE IMD3, Input Amplitude 1 ($A_{IN1}$) = Input Amplitude 2 ($A_{IN2}$) = −7 dBFS | | | | |
| Input Frequency 1 ($f_{IN1}$) = 890 MHz, Input Frequency 2 ($f_{IN2}$) = 910 MHz | | | | |
| $f_{IN1}$ = 1780 MHz, $f_{IN2}$ = 1820 MHz | | −78.9 | | dBFS |
| $f_{IN1}$ = 2680 MHz, $f_{IN2}$ = 2720 MHz | | −75 | | dBFS |
| $f_{IN1}$ = 3560 MHz, $f_{IN2}$ = 3640 MHz | | −73.2 | | dBFS |
| $f_{IN1}$ = 5360 MHz, $f_{IN2}$ = 5440 MHz | | −64.2 | | dBFS |
| ANALOG BANDWIDTH[3] | | 8 | | GHz |

[1] Noise density is measured at a low analog amplitude and/or frequency where timing jitter does not degrade noise floor.
[2] Noise figure is based on a nominal full-scale input power of 4.5 dBm with an input span of 1.5 V p-p and $R_{IN}$ = 100 Ω.
[3] Analog input bandwidth is the bandwidth of operation in which the full-scale input frequency response rolls off by −3 dB based on a de-embedded model of the ADC extracted from the measured frequency response on evaluation board. This bandwidth requires optimized matching network to achieve this upper bandwidth.

## TIMING SPECIFICATIONS

For the minimum and maximum values, $T_J$ = −40°C to +120°C and ±5% of nominal supply, unless otherwise noted.

**Table 11.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SERIAL PORT INTERFACE (SPI) WRITE OPERATION | | | | | | |
| Maximum SCLK Clock Rate | $f_{SCLK}$, $1/t_{SCLK}$ | | 33 | | | MHz |
| SCLK Clock High | $t_{PWH}$ | SCLK = 33 MHz | 5 | | | ns |
| SCLK Clock Low | $t_{PWL}$ | SCLK = 33 MHz | 5 | | | ns |
| SDIO to SCLK Setup Time | $t_{DS}$ | | 4 | | | ns |
| SCLK to SDIO Hold Time | $t_{DH}$ | | 4 | | | ns |
| CSB to SCLK Setup Time | $t_S$ | | 4 | | | ns |
| SCLK to CSB Hold Time | $t_H$ | | 4 | | | ps |

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SPI READ OPERATION | | | | | | |
| Maximum SCLK Clock Rate | $f_{SCLK}$, $1/t_{SCLK}$ | | 8 | | | MHz |
| SCLK Clock High | $t_{PWH}$ | | 50 | | | ns |
| SCLK Clock Low | $t_{PWL}$ | | 50 | | | ns |
| SDIO to SCLK Setup Time | $t_{DS}$ | | 4 | | | ns |
| SCLK to SDIO Hold Time | $t_{DH}$ | | 4 | | | ns |
| CSB to SCLK Setup Time | $t_S$ | | 4 | | | ns |
| SCLK to SDIO Data Valid Time | $t_{DV}$ | | 20 | | | ns |
| SCLK to SDO Data Valid Time | $t_{DV\_SDO}$ | | 20 | | | ns |
| CSB to SDIO Output Valid to High-Z | $t_Z$ | | 20 | | | ns |
| CSB to SDO Output Valid to High-Z | $t_{Z\_SDO}$ | | 20 | | | ns |

### *Timing Diagrams*

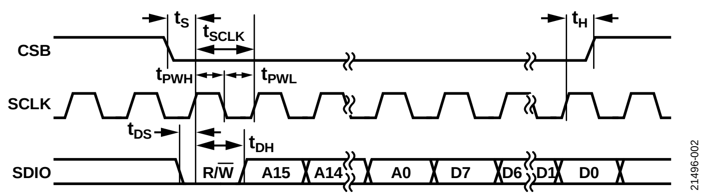



*Figure 2. Timing Diagram for 3-Wire Write Operation*

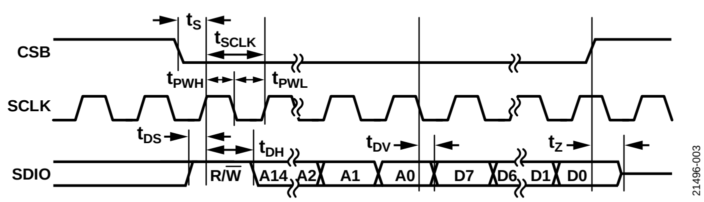



*Figure 3. Timing Diagram for 3-Wire Read Operation*

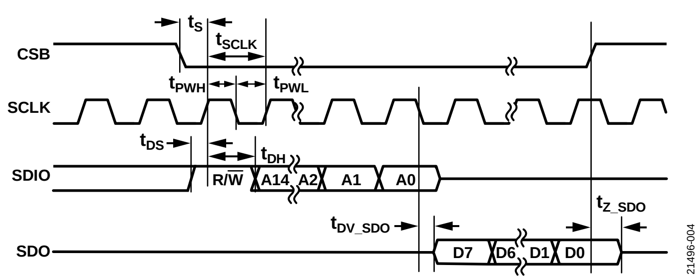



*Figure 4. Timing Diagram for 4-Wire Read Operation*

# ABSOLUTE MAXIMUM RATINGS

**Table 12.**

| Parameter | Rating |
|---|---|
| ISET, DACxP, DACxN, TDP, TDN | −0.3 V to AVDD2 + 0.3 V |
| VCO_COARSE, VCO_FINE, VCO_VCM, VCO_VREG | −0.3 V to AVDD2_PLL + 0.3 V |
| ADC0P, ADC0N, ADC1P, ADC1N | −0.3 V to BVDD2 + 0.3 V |
| VCM0, VCM1 | −0.3 V to RVDD2 + 0.3 V |
| CLKINP, CLKINN | −0.2 V to PLLCLKVDD1 + 0.2 V |
| ADCDRVN, ADCDRVP | −0.2 V to CLKVDD1 + 0.2 V |
| SERDINx±, SERDOUTx± | −0.2 V to SVDD1 + 0.2 V |
| SYSREFP, SYSREFN, and SYNCxINB± | −0.2 V to +2.5 V |
| SYNCxOUTB±, SYNCxINB±, RESETB, TXENx, RXENx, IRQB_x, CSB, SCLK, SDIO, SDO, TMU_REFN, TMU_REFP, ADCx_SMON0, ADCx_SMON1, ADCx_FD0, ADCx_FD1, GPIOx | −0.3 V to DVDD1P8 + 0.3 V |
| AVDD2, AVDD2_PLL, BVDD2, RVDD2, SVDD2_PLL, DVDD1P8 | −0.3 V to +2.2 V |
| PLLCLKVDD1, AVDD1, AVDD1_ADC, CLKVDD1, FVDD1, DAVDD1, DVDD1_RT, DCLKVDD1, SVDD1 | −0.2 V to +1.2 V |
| VNN1 | −1.1 V to +0.2 V |
| Temperature | |
| Junction ($T_J$)[1] | 125°C |
| Storage Range | −40°C to +150°C |

[1] Do not exceed this temperature for any duration of time when the device is powered.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## REFLOW PROFILE

The AD9082 reflow profile is in accordance with the JEDEC JESD 20 criteria for Pb-free devices. The maximum reflow temperature is 260°C.

## THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. The use of appropriate thermal management techniques is recommended to ensure that the maximum $T_J$ does not exceed the limits shown in Table 12.

$\theta_{JA}$ is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

$\theta_{JC\_TOP}$ is the junction to case, thermal resistance.

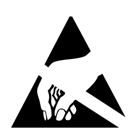
$\theta_{JB}$ is the junction to board, thermal resistance.

**Table 13. Simulated Thermal Resistance[1]**

| PCB Type | Airflow Velocity (m/sec) | $\theta_{JA}$ | $\theta_{JC\_TOP}$ | $\theta_{JB}$ | Unit |
|---|---|---|---|---|---|
| JEDEC 2s2p Board | 0.0 | 14.9 | 0.70 | 1.8 | °C/W |

[1] Thermal resistance values specified are simulated based on JEDEC specifications in compliance with JESD51-12 with the device power equal to 9 W.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

**AD9082**

TOP VIEW
(Not to Scale)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | GND | AVDD2 | GND | GND | NC | NC | GND | GND | ADC0N | ADC0P | GND | SYNC1INB– | SYNC0INB– | SERDOUT0– | SERDOUT0+ | SVDD1 | GND | GND |
| B | DAC0P | GND | GND | GND | GND | GND | DNC | VCM0 | GND | GND | RVDD2 | SYNC1INB+ | SYNC0INB+ | GND | GND | SVDD1 | SERDOUT7– | SERDOUT7+ |
| C | DAC0N | GND | ADCDRVN | ADCDRVP | GND | GND | GND | GND | BVNN2 | BVDD3 | GND | RESETB | DVDD1P8 | SERDOUT1– | SERDOUT1+ | SVDD1 | GND | GND |
| D | GND | AVDD1 | AVDD1 | AVDD1 | GND | FVDD1 | BVDD2 | VNN1 | GND | VDD1_NVG | ADC0_SMON1 | ADC0_SMON0 | RXEN1 | GND | GND | SVDD1 | SERDOUT6– | SERDOUT6+ |
| E | GND | AVDD2 | AVDD1 | GND | DAVDD1 | GND | BVDD2 | VNN1 | NVG1_OUT | VNN1 | ADC1_SMON1 | ADC1_SMON0 | RXEN0 | SERDOUT2– | SERDOUT2+ | SVDD1 | GND | GND |
| F | DAC1N | GND | AVDD1 | GND | DAVDD1 | GND | GND | GND | DVDD1P8 | DVDD1 | ADC0_FD1 | ADC0_FD0 | SDIO | GND | GND | SVDD1 | SERDOUT5– | SERDOUT5+ |
| G | DAC1P | GND | GND | GND | GND | CLKVDD1 | AVDD1_ADC | AVDD1_ADC | TMU_REFN | TMU_REFP | ADC1_FD1 | ADC1_FD0 | CSB | SERDOUT3– | SERDOUT3+ | SVDD1 | GND | GND |
| H | GND | AVDD2 | ISET | DNC | GND | GND | GND | GND | DVDD1 | GND | DVDD1 | GND | SCLK | GND | GND | SVDD1 | SERDOUT4– | SERDOUT4+ |
| J | CLKINP | GND | VCO_FINE | VCO_COARSE | PLLCLKVDD1 | DVDD1_RT | DVDD1_RT | GND | DVDD1 | GND | DVDD1 | GND | SDO | GND | GND | SVDD1_PLL | GND | GND |
| K | CLKINN | GND | VCO_VREG | VCO_VCM | DCLKVDD1 | DVDD1_RT | DVDD1_RT | GND | DVDD1 | GND | DVDD1 | GND | GPIO9 | GND | SVDD2_PLL | SVDD1_PLL | GND | GND |
| L | GND | AVDD2 | AVDD2_PLL | DNC | GND | GND | GND | GND | DVDD1 | GND | DVDD1 | GND | GPIO8 | GND | DNC | DNC | SERDIN0– | SERDIN0+ |
| M | DAC2P | GND | GND | GND | GND | CLKVDD1 | AVDD1_ADC | AVDD1_ADC | DVDD1 | GND | GPIO3 | GPIO1 | GPIO7 | SERDIN4– | SERDIN4+ | SVDD1 | GND | GND |
| N | DAC2N | GND | AVDD1 | GND | DAVDD1 | GND | GND | GND | TDP | TDN | GPIO2 | GPIO0 | GPIO6 | GND | GND | SVDD1 | SERDIN1– | SERDIN1+ |
| P | GND | AVDD2 | AVDD1 | GND | DAVDD1 | GND | BVDD2 | VNN1 | NVG1_OUT | VNN1 | GPIO4 | IRQB_0 | TXEN0 | SERDIN7– | SERDIN7+ | SVDD1 | GND | GND |
| R | GND | AVDD1 | AVDD1 | AVDD1 | GND | FVDD1 | BVDD2 | VNN1 | GND | VDD1_NVG | GPIO5 | IRQB_1 | TXEN1 | GND | GND | SVDD1 | SERDIN2– | SERDIN2+ |
| T | DAC3N | GND | SYSREFN | SYSREFP | GND | GND | GND | GND | BVNN2 | BVDD3 | GND | GPIO10 | DVDD1P8 | SERDIN6– | SERDIN6+ | SVDD1 | GND | GND |
| U | DAC3P | GND | GND | GND | GND | GND | DNC | VCM1 | GND | GND | RVDD2 | SYNC1OUTB+ | SYNC0OUTB+ | GND | GND | SVDD1 | SERDIN3– | SERDIN3+ |
| V | GND | AVDD2 | GND | GND | NC | NC | GND | GND | ADC1N | ADC1P | GND | SYNC1OUTB– | SYNC0OUTB– | SERDIN5– | SERDIN5+ | SVDD1 | GND | GND |

GND — ANALOG GROUND; GND — DIGITAL GROUND; GND — SERDES GROUND

21496-006

*Figure 5. 324-Ball Pin Configuration*

**Table 14. Pin Function Descriptions**

| Pin No. | Mnemonic | Type | Description |
|---|---|---|---|
| POWER SUPPLIES | | | |
| A2, E2, H2, L2, P2, V2 | AVDD2 | Input | Analog 2.0 V Supply Inputs for DAC. |
| L3 | AVDD2_PLL | Input | Analog 2.0 V Supply Input for Clock PLL Linear Dropout Regulator (LDO). |
| D7, E7, P7, R7 | BVDD2 | Input | Analog 2.0 V Supply Inputs for ADC Buffer. |
| B11, U11 | RVDD2 | Input | Analog 2.0 V Supply Inputs for ADC Reference. |
| J5 | PLLCLKVDD1 | Input | Analog 1.0 V Supply Input for Clock PLL. |
| D2 to D4, E3, F3, N3, P3, R2 to R4 | AVDD1 | Input | Analog 1.0 V Supply Inputs for DAC Clock. |
| G7, G8, M7, M8 | AVDD1_ADC | Input | Analog 1.0 V Supply Inputs for ADC. |
| G6, M6 | CLKVDD1 | Input | Analog 1.0 V Supply Inputs for ADC Clock. |
| D6, R6 | FVDD1 | Input | Analog 1.0 V Supply Inputs for ADC Reference. |
| D10, R10 | VDD1_NVG | Input | Analog 1.0 V Supply Inputs for Negative Voltage Generator (NVG) Used to Generate −1 V Output. |
| E9, P9 | NVG1_OUT | Output | Analog −1 V Supply Outputs from NVG. Decouple NVG1_OUT to GND with a 0.1 μF capacitor. |
| D8, E8, E10, P8, R8, P10 | VNN1 | Input | Analog −1 V Supply Inputs for ADC Buffer and Reference. Connect these pins to the adjacent, NVG1_OUT pins. |
| C9, T9, | BVNN2 | Output | Analog −2 V Supply Outputs for ADC Buffer. Decouple each BVNN2 pin to GND with a 0.1 μF capacitor. |
| C10, T10 | BVDD3 | Output | Analog 3 V Supply Output for ADC Buffer. Decouple BVDD3 to GND with 0.1 μF capacitor. |
| E5, F5, N5, P5 | DAVDD1 | Input | Digital Analog 1.0 V Supply Inputs. |
| F10, H9, H11, J9, J11, K9, K11, L9, L11, M9 | DVDD1 | Input | Digital 1.0 V Supply Inputs. |
| J6, J7, K6, K7 | DVDD1_RT | Input | Digital 1.0 Supply Inputs for Retimer Block. |
| K5 | DCLKVDD1 | Input | Digital 1.0 V Clock Generation Supply. |
| A16, B16, C16, D16, E16, F16, G16, H16, M16, N16, P16, R16, T16, U16, V16 | SVDD1 | Input | Digital 1.0 V Supply Inputs for SERDES Deserializer and Serializer. |
| K15 | SVDD2_PLL | Input | Digital 2.0 V Supply Input for SERDES LDO. |
| J16, K16 | SVDD1_PLL | Input | Digital 1.0 V Supply Inputs for SERDES Clock Generation and PLL. |
| C13, F9, T13 | DVDD1P8 | Input | Digital Interface and Temperature Monitoring Unit (TMU) Supply Inputs (Nominal 1.8 V). |
| A1, A3, A4, A7, A8, A11, A17, A18, B2 to B6, B9, B10, B14, B15, C2, C5 to C8, C11, C17, C18, D1, D5, D9, D14, D15, E1, E4, E6, E17, E18, F2, F4, F6 to F8, F14, F15, G2 to G5, G17, G18, H1, H5 to H8, H10, H12, H14, H15, J2, J8, J10, J12, J14, J15, J17, J18, K2, K8, K10, K12, K14, K17, K18, L1, L5 to L8, L10, L12, L14, M2 to M5, M10, M17, M18, N2, N4, N6 to N8, N14, N15, P1, P4, P6, P17, P18, R1, R5, R9, R14, R15, T2, T5 to T8, T11, T17, T18, U2 to U6, U9, U10, U14, U15, V1, V3, V4, V7, V8, V11, V17, V18 | GND | Input/output | Ground References. |

| Pin No. | Mnemonic | Type | Description |
|---|---|---|---|
| ANALOG OUTPUTS | | | |
| B1, C1 | DAC0P, DAC0N | Output | DAC0 Output Currents, Ground Referenced. |
| G1, F1 | DAC1P, DAC1N | Output | DAC1 Output Currents, Ground Referenced. |
| M1, N1 | DAC2P, DAC2N | Output | DAC2 Output Currents, Ground Referenced. |
| U1, T1 | DAC3P, DAC3N | Output | DAC3 Output Currents, Ground Referenced. |
| H3 | ISET | Output | DAC Bias Current Setting Pin. Connect this pin with a 5 kΩ resistor to GND. |
| C4, C3 | ADCDRVP, ADCDRVN | Output | ADC Clock Output Options. These pins are disabled by default. |
| B8, U8 | VCM0, VCM1 | Output | ADC Buffer Common-Mode Output Voltage. Decouple this pin to GND with a 0.1 μF capacitor. |
| K3 | VCO_VREG | Output | PLL LDO Regulator Output. Decouple this pin to GND with a 2.2 μF capacitor. |
| G9 | TMU_REFN | Output | TMU ADC Negative Reference. Connect this pin to GND. |
| G10 | TMU_REFP | Output | TMU ADC Positive Reference. Connect this pin to DVDD1P8. |
| ANALOG INPUTS | | | |
| A10, A9 | ADC0P, ADC0N | Input | ADC0 Differential Inputs with Internal 100 Ω Differential Resistor. |
| V10, V9 | ADC1P, ADC1N | Input | ADC1 Differential Inputs with Internal 100 Ω Differential Resistor. |
| J3 | VCO_FINE | Input | On-Chip Clock Multiplier and PLL Fine Loop Filter Input. |
| J4 | VCO_COARSE | Input | On-Chip DAC Clock Multiplier and PLL Coarse Loop Filter Input. |
| K4 | VCO_VCM | Input | On-Chip Clock Multiplier and VCO Common-Mode Input. |
| N9, N10 | TDP, TDN | Input | Anode and Cathode of Temperature Diodes. This feature is not supported. Tie TDP and TDN to GND. |
| J1, K1 | CLKINP, CLKINN | Input | Differential Clock Inputs with Nominal 100 Ω Termination. Self bias input requiring ac coupling. When the on-chip clock multiplier PLL is enabled, this input is the reference clock input. If the PLL is disabled, an RF clock equal to the DAC output sample rate is required. |
| CMOS INPUTS AND OUTPUTS[1] | | | |
| G13 | CSB | Input | Serial Port Enable Input. Active low. |
| H13 | SCLK | Input | Serial Plot Clock Input. |
| F13 | SDIO | Input/output | Serial Port Bidirectional Data Input/Output. |
| J13 | SDO | Output | Serial Port Data Output. |
| C12 | RESETB | Input | Active Low Reset Input. RESETB places digital logic and SPI registers in a known default state. RESETB must be connected to a digital IC that is capable of issuing a reset signal for the first step in the device initialization process. |
| E13, D13 | RXEN0, RXEN1 | Input | Active High ADC and Receive Datapath Enable Inputs. RXENx is also SPI configurable. |
| P13, R13 | TXEN0, TXEN1 | Input | Active High DAC and Transmit Datapath Enable Inputs. TXENx is also SPI configurable. |

| Pin No. | Mnemonic | Type | Description |
|---|---|---|---|
| D12, D11 | ADC0_SMON0, ADC0_SMON1 | Output | ADC0 Signal Monitoring Outputs by Default. Do not connect if unused. |
| E12, E11 | ADC1_SMON0, ADC1_SMON1 | Output | ADC1 Signal Monitoring Outputs by Default. Do not connect if unused. |
| F12, F11 | ADC0_FD0, ADC0_FD1 | Output | ADC0 Fast Detect Outputs by Default. Do not connect if unused. |
| G12, G11 | ADC1_FD0, ADC1_FD1 | Output | ADC1 Fast Detect Outputs by Default. Do not connect if unused. |
| P12, R12 | IRQB_0, IRQB_1 | Outputs | Interrupt Request 0 and 1 Outputs. These pins are an open-drain, active low output (CMOS levels with respect to DVDD1P8). Connect a 10 kΩ pull-up resistor to DVDD1P8 to prevent these pins from floating when unused. |
| K13, L13, M11 to M13, N11 to N13, P11, R11, T12 | GPIO0 to GPIO10 | Input/output | General-Purpose Input or Output Pins. |
| JESD204B or JESD204C COMPATIBLE SERDES DATA LANES AND CONTROL SIGNALS[2] | | | |
| L18, L17 | SERDIN0+, SERDIN0− | Input | JRx Lane 0 Inputs, Data True/Complement. |
| N18, N17 | SERDIN1+, SERDIN1− | Input | JRx Lane 1 Inputs, Data True/Complement. |
| R18, R17 | SERDIN2+, SERDIN2− | Input | JRx Lane 2 Inputs, Data True/Complement. |
| U18, U17 | SERDIN3+, SERDIN3− | Input | JRx Lane 3 Inputs, Data True/Complement. |
| M15, M14 | SERDIN4+, SERDIN4− | Input | JRx Lane 4 Inputs, Data True/Complement. |
| V15, V14 | SERDIN5+, SERDIN5− | Input | JRx Lane 5 Inputs, Data True/Complement. |
| T15, T14 | SERDIN6+, SERDIN6− | Input | JRx Lane 6 Inputs, Data True/Complement. |
| P15, P14 | SERDIN7+, SERDIN7− | Input | JRx Lane 7 Inputs, Data True/Complement. |
| U13, V13 | SYNC0OUTB+, SYNC0OUTB− | Output | JRx Link 0 Synchronization Outputs for JESD204B interface. These pins are LVDS or CMOS configurable. These pins can also provide differential 100 Ω output impedance in LVDS mode. |
| U12, V12 | SYNC1OUTB+, SYNC1OUTB− | Output | JRx Link 1 Synchronization Outputs for JESD204B interface or CMOS Input for Transmit Fast Frequency Hopping (FFH) via GPIOx pins. For sync output function, these pins are LVDS or CMOS output configurable and can provide differential 100 Ω output impedance in LVDS mode. |
| A15, A14 | SERDOUT0+, SERDOUT0− | Output | JTx Lane 0 Outputs, Data True/Complement. |
| C15, C14 | SERDOUT1+, SERDOUT1− | Output | JTx Lane 1 Outputs, Data True/Complement. |
| E15, E14 | SERDOUT2+, SERDOUT2− | Output | JTx Lane 2 Outputs, Data True/Complement. |
| G15, G14 | SERDOUT3+, SERDOUT3− | Output | JTx Lane 3 Outputs, Data True/Complement. |
| H18, H17 | SERDOUT4+, SERDOUT4− | Output | JTx Lane 4 Outputs, Data True/Complement. |

| Pin No. | Mnemonic | Type | Description |
|---|---|---|---|
| F18, F17 | SERDOUT5+, SERDOUT5− | Output | JTx Lane 5 Outputs, Data True/Complement. |
| D18, D17 | SERDOUT6+, SERDOUT6− | Output | JTx Lane 6 Outputs, Data True/Complement. |
| B18, B17 | SERDOUT7+, SERDOUT7− | Output | JTx Lane 7 Outputs, Data True/Complement. |
| B13, A13 | SYNC0INB+, SYNC0INB− | Input | JTx Link 0 Synchronization Inputs for JESD204B interface. These pins are LVDS or CMOS configurable. These pins are LVDS or CMOS configurable and have selectable internal 100 Ω input impedance for LVDS operation |
| B12, A12 | SYNC1INB+, SYNC1INB− | Input | JTx Link 1 Synchronization Inputs for JESD204B interface or CMOS Inputs for Receive FFH via GPIOx pins. These pins are LVDS or CMOS configurable and have selectable internal 100 Ω input impedance for LVDS operation. |
| T4, T3 | SYSREFP, SYSREFN | Input | Active High JESD204 System Reference Inputs. These pins are configurable for differential current mode logic (CML), PECL, and LVDS with internal 100 Ω termination or single-ended CMOS. |
| NO CONNECTS AND DO NOT CONNECTS | | | |
| A5, A6, V5, V6 | NC | | No Connect. These pins can be left open or connected. |
| B7, H4, L4, L15, L16, U7 | DNC | DNC | Do Not Connect. The pins must be kept open. |

[1] CMOS inputs do not have pull-up or pull-down resistors.
[2] SERDINx± and SERDOUTx± include 100 Ω internal termination resistors.

# TYPICAL PERFORMANCE CHARACTERISTICS

## DAC

$T_A$ = 25°C using the AD9082-FMCA-EBZ, data curves represent average performance of all DAC outputs with harmonics (or alias harmonics) and spurs falling in the first DAC Nyquist zone (<$f_{DAC}$/2), $I_{OUTFS}$ = 26 mA, PLL clock multiplier enabled, and ADC powered down, unless otherwise noted. See the UG-1578 user guide for additional information on the JESDB or JESDC mode configurations.

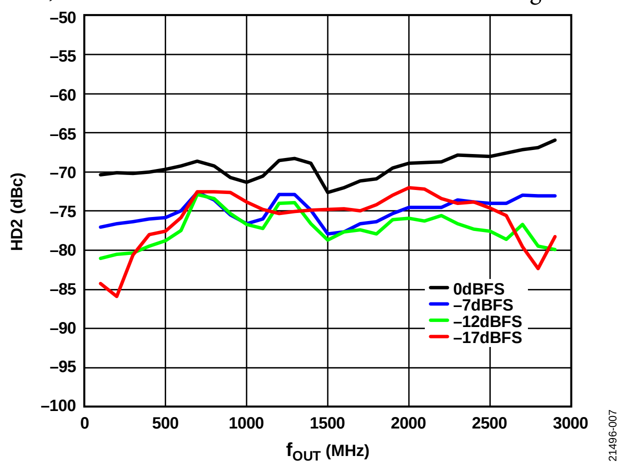



Figure 6. HD2 vs. $f_{OUT}$ over Digital Scale (Mode 17B), 6 GSPS DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 4×

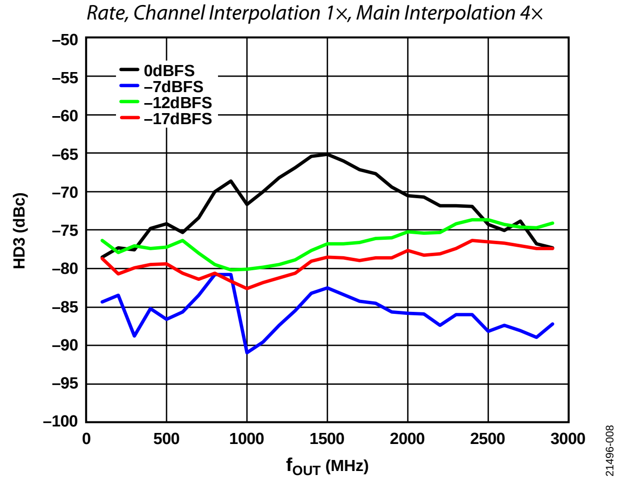



Figure 7. HD3 vs. $f_{OUT}$ over Digital Scale (Mode 17B), 6 GSPS DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 4×

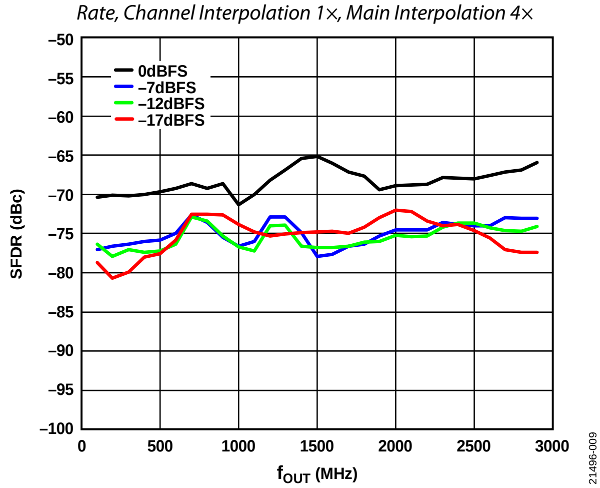



Figure 8. SFDR, Worst Spurious vs. $f_{OUT}$ over Digital Scale (Mode 17B), 6 GSPS DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 4×

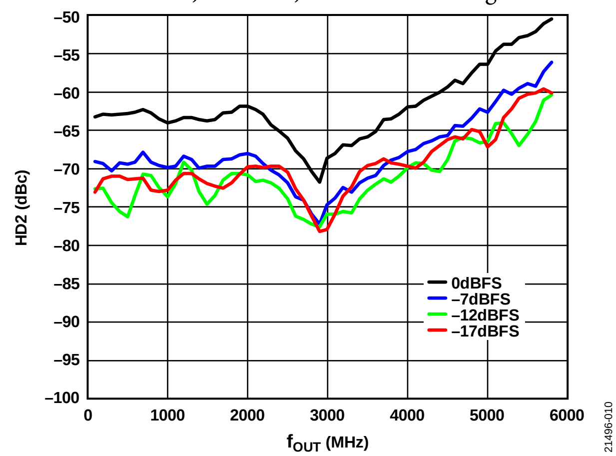



Figure 9. HD2 vs. $f_{OUT}$ over Digital Scale (Mode 16B), 12 GSPS DAC Sample Rate, Channel Interpolation 4×, Main Interpolation 8×

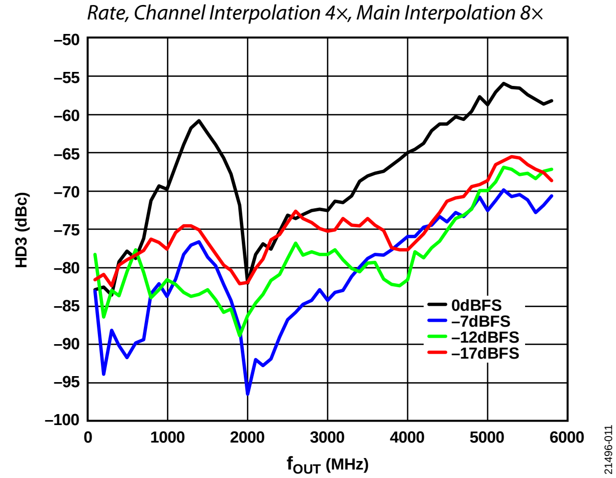



Figure 10. HD3 vs. $f_{OUT}$ over Digital Scale (Mode 16B), 12 GSPS DAC Sample Rate, Channel Interpolation 4×, Main Interpolation 8×

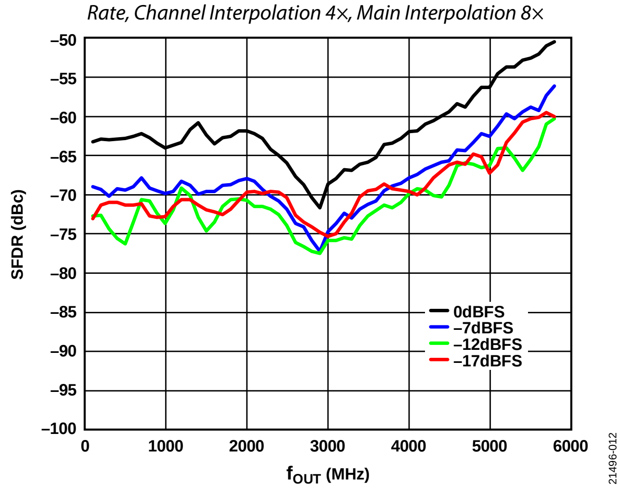



Figure 11. SFDR, Worst Spurious vs. $f_{OUT}$ over Digital Scale (Mode 16B), 12 GSPS DAC Sample Rate, Channel Interpolation 4×, Main Interpolation 8×

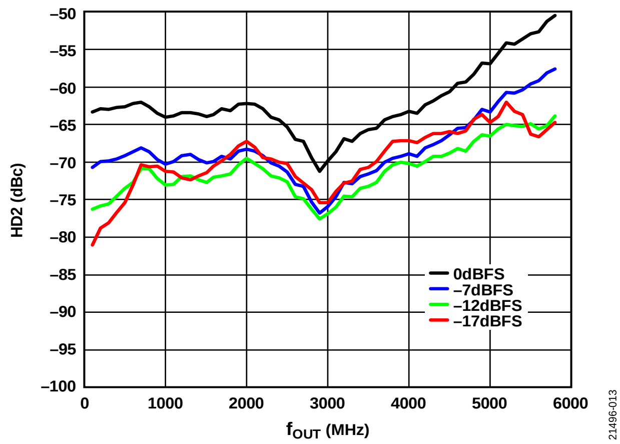



Figure 12. HD2 vs. $f_{OUT}$ over Digital Scale (Mode 17B), 12 GHz GSPS Sample Rate, Channel Interpolation 1×, Main Interpolation 8×

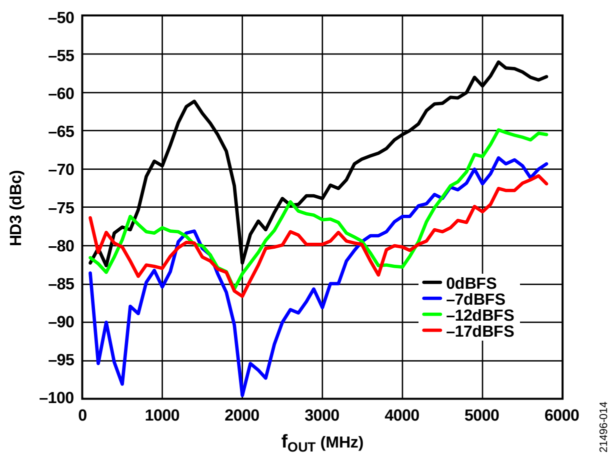



Figure 13. HD3 vs. $f_{OUT}$ over Digital Scale (Mode 17B), 12 GSPS DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 8×

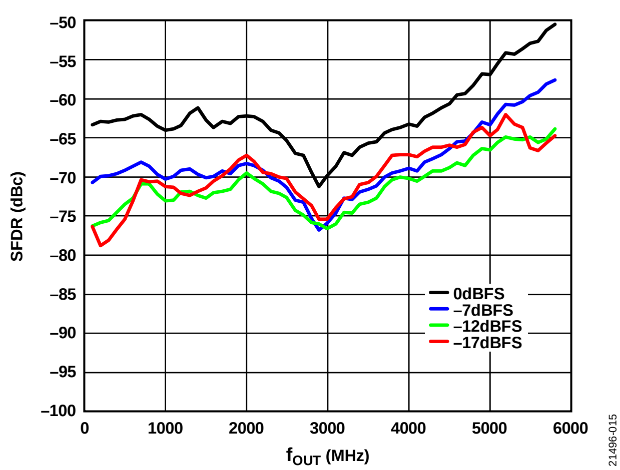



Figure 14. SFDR vs. $f_{OUT}$ over Digital Scale (Mode 17B), 12 GSPS DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 8×

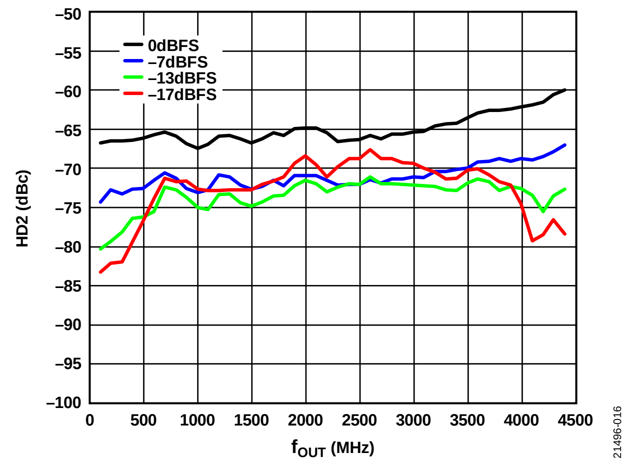



Figure 15. HD2 vs. $f_{OUT}$ over Digital Scale (Mode 17B), 9 GHz GSPS Sample Rate, Channel Interpolation 1×, Main Interpolation 6×

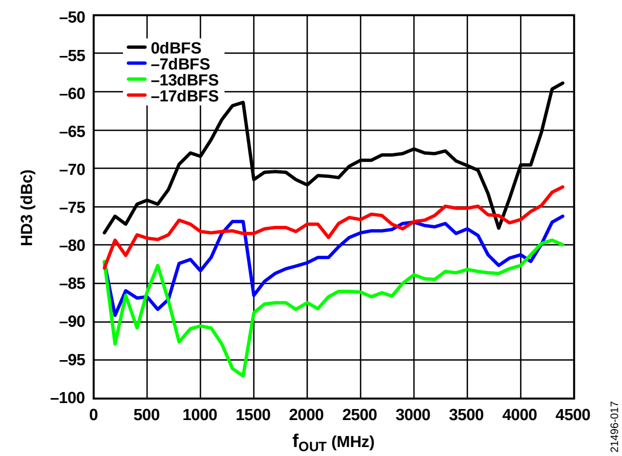



Figure 16. HD3 vs. $f_{OUT}$ over Digital Scale (Mode 17B), 9 GSPS DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 6×

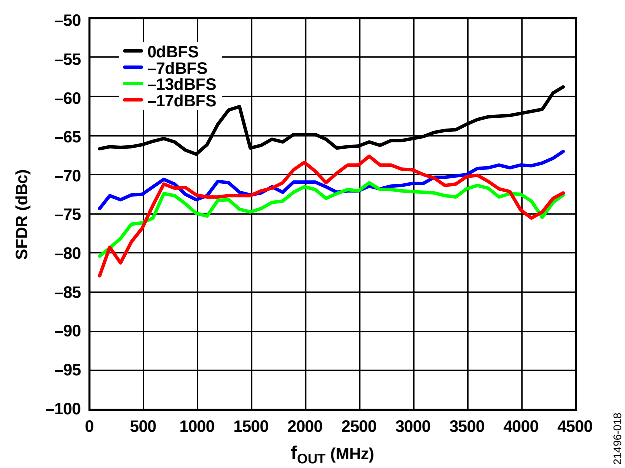



Figure 17. SFDR vs. $f_{OUT}$ over Digital Scale (Mode 17B), 9 GSPS DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 6×

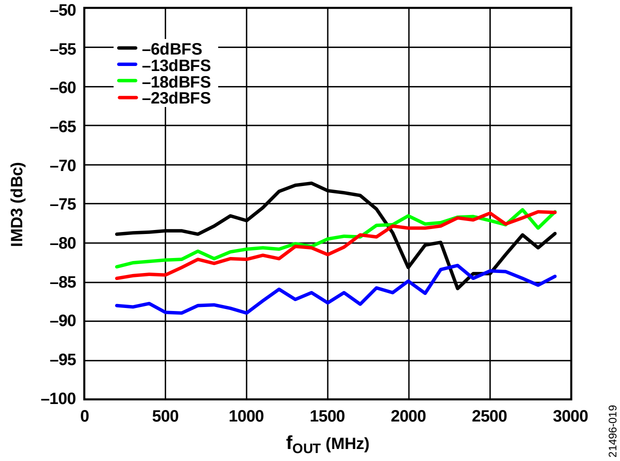


Figure 18. IMD3 vs. $f_{OUT}$ over Digital Scale (Mode 17B), 6 GSPS DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 4×

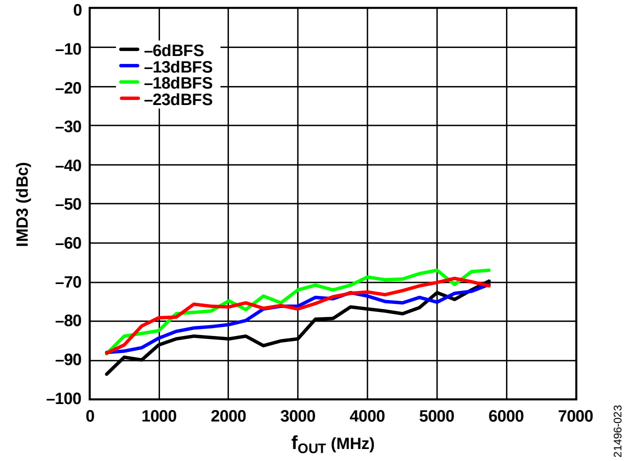


Figure 21. IMD3 vs. $f_{OUT}$ over Digital Scale (Mode 17B), 9 GSPS DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 6×, 1 MHz Tone Spacing

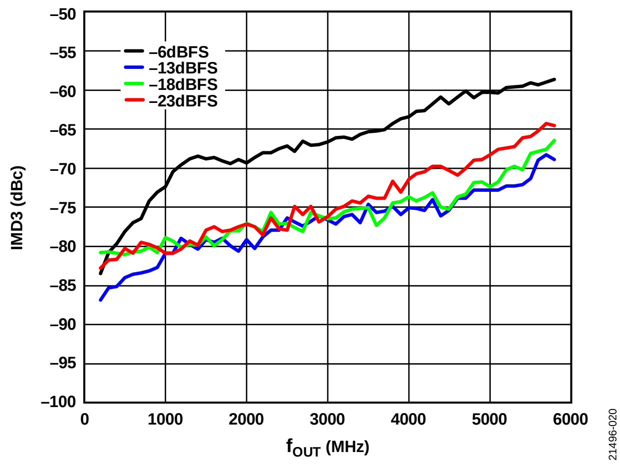


Figure 19. IMD3 vs. $f_{OUT}$ over Digital Scale (Mode 16B), 12 GHz DAC Sample Rate, Channel Interpolation 4×, Main Interpolation 8×

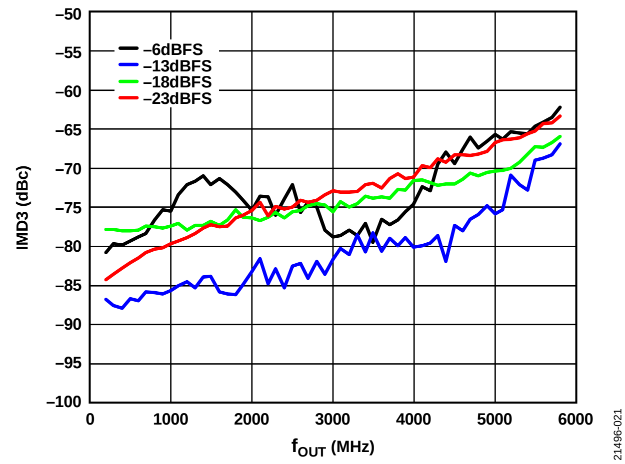


Figure 22. IMD3 vs. $f_{OUT}$ over Digital Scale (Mode 17B), 12 GSPS DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 8×

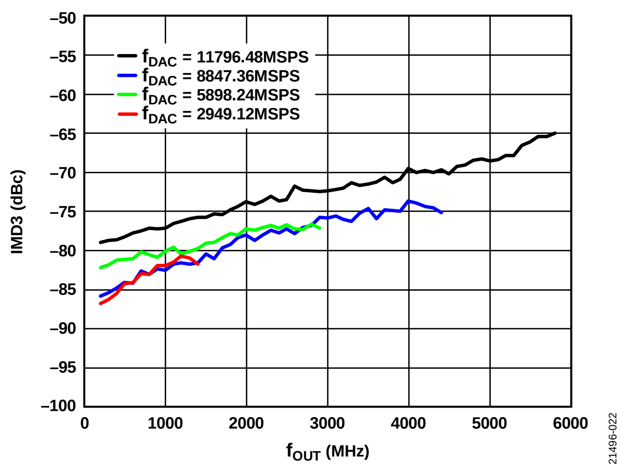


Figure 20. IMD3 vs. $f_{OUT}$ over $f_{DAC}$ (Mode 17B), 1 MHz Tone Spacing with –12 dBFS/Tone Level

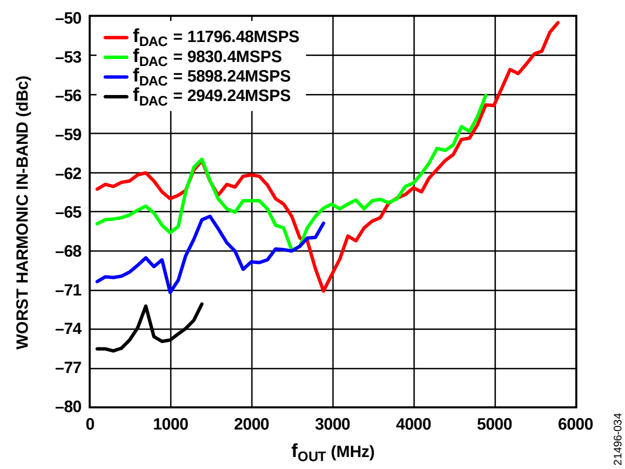


Figure 23. Worst Harmonic In-Band vs. $f_{OUT}$ Across $f_{DAC}$ with 0 dBFS Tone Level (Mode 17B)

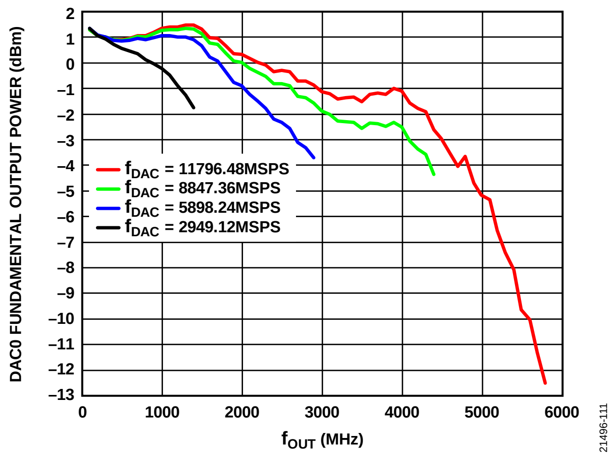



Figure 24. DAC0 Fundamental Output Power vs. $f_{OUT}$ for Different $f_{DAC}$ Sample Rates (Mode 17B), Channel Interpolation 1×, Main Interpolation 8×, 0 dBFS Digital Back Off)

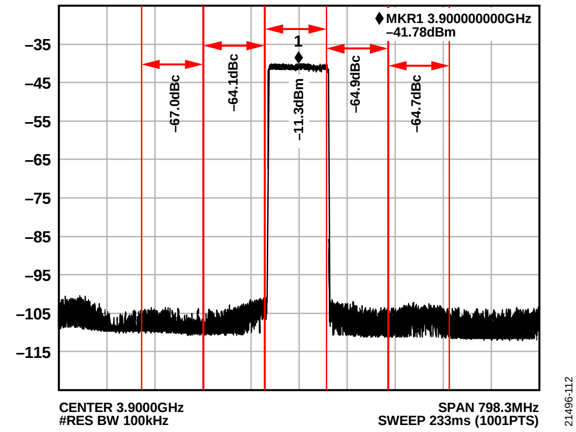



Figure 27. Adjacent Channel Leakage Ratio (ACLR) Performance for 100 MHz 5G Test Vector at $f_{OUT}$ = 3.9 GHz and $f_{DAC}$ = 11.898 GSPS, Test Vector Peak to RMS = 11.7 dB with −1 dBFS Back Off (Mode 9C), Channel Interpolation 3×, Main Interpolation 8×

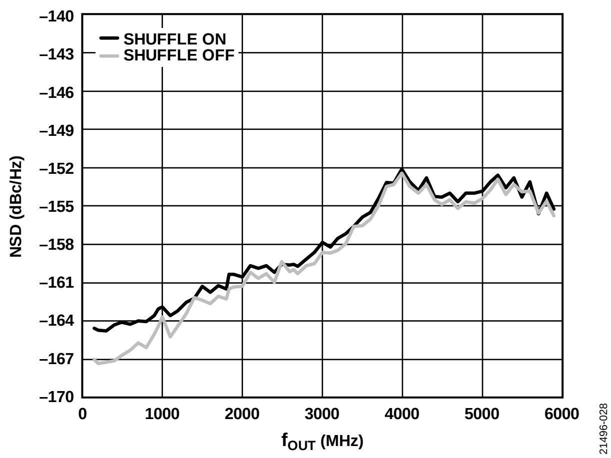



Figure 25. Single-Tone NSD Measured at 10% Offset from $f_{OUT}$ vs. $f_{OUT}$, 11796.48 MSPS $f_{DAC}$, 16-Bit Resolution, Shuffle Off vs. Shuffle On (Mode 17B)

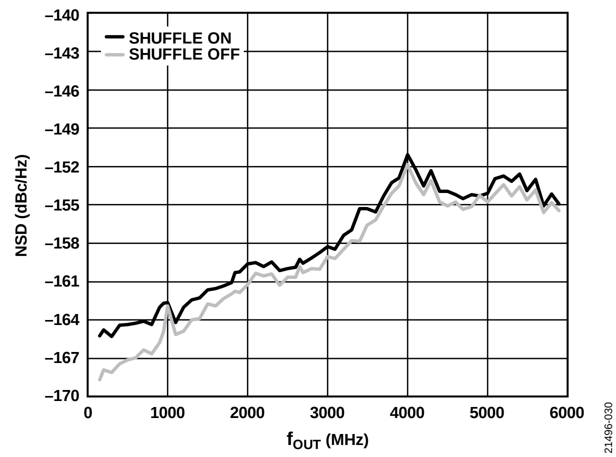



Figure 28. Single-Tone NSD Measured at 10% Offset from $f_{OUT}$ vs. $f_{OUT}$, 11796.48 MSPSz $f_{DAC}$, 12-Bit Resolution, Shuffle Off vs. Shuffle On (Mode 24C)

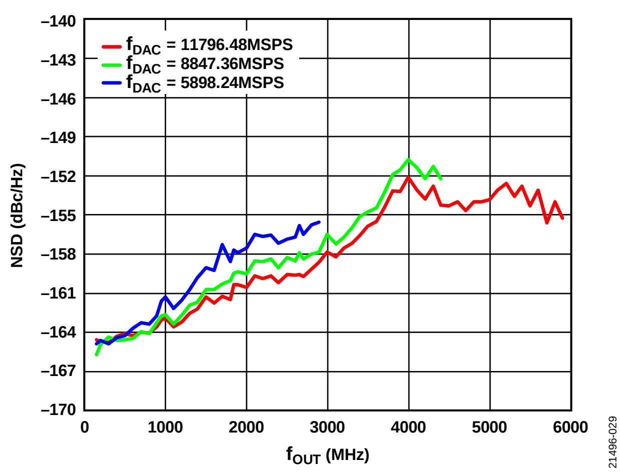



Figure 26. Single-Tone NSD Measured at 10% Offset from $f_{OUT}$ vs. $f_{OUT}$ over $f_{DAC}$, 16-Bit Resolution, Shuffle On (Mode 17B)

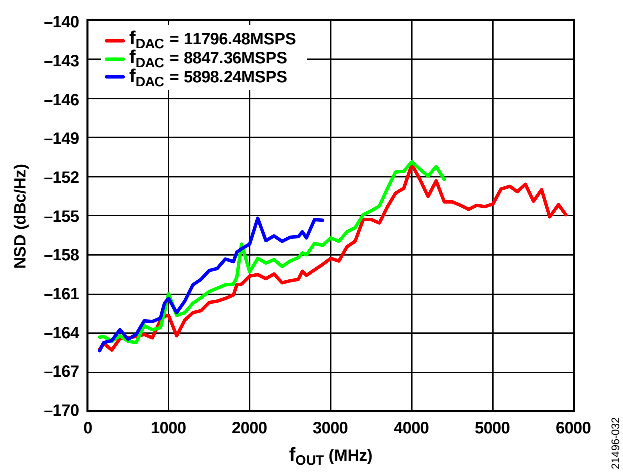



Figure 29. Single-Tone NSD Measured at 10% Offset from $f_{OUT}$ vs. $f_{OUT}$ over $f_{DAC}$, 12-Bit Resolution, Shuffle On (Mode 24C)

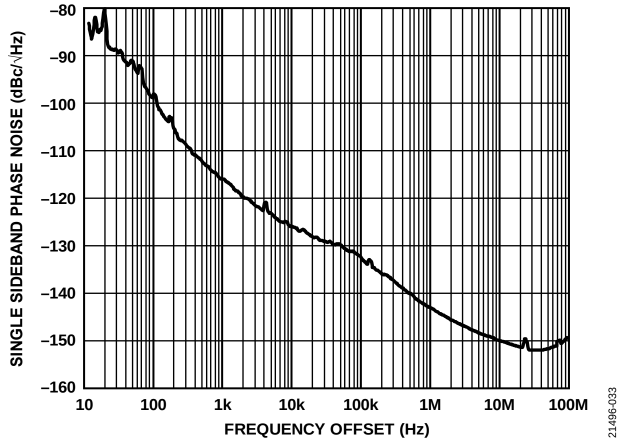



*Figure 30. Single Sideband Phase Noise vs. Frequency Offset with $f_{DAC}$ = 12 GSPS, $f_{OUT}$ = 3 GHz, Clock PLL Disabled with External 12 GHz Clock Input Using R&S SMA100B with B711 Option as Clock Source, Engineering Board Used*

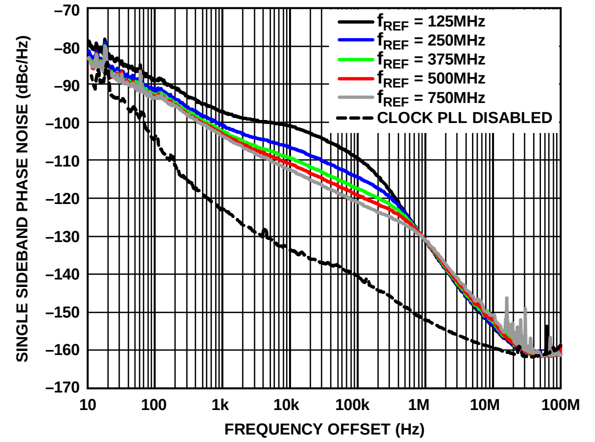



*Figure 33. Single Sideband Phase Noise vs. Frequency Offset for Different PLL Reference Clock ($f_{REF}$), $f_{OUT}$ = 1.8 GHz, $f_{DAC}$ = 12 GSPS, PLL Enabled with Exception of External 12 GHz Clock Input with Clock PLL Disabled, Engineering Board Used*

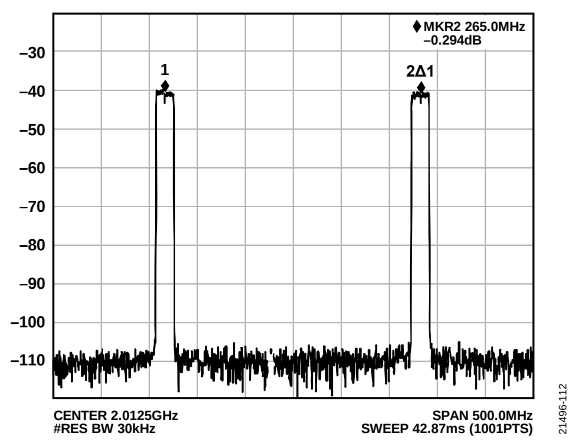



*Figure 31. Dual Band 3GPP B1 and B3 Wideband Plot for 20 MHz LTE at $f_{OUT}$ = 1.88 GHz and $f_{OUT}$ = 2.145 GHz with $f_{DAC}$ = 11.796 GSPS, Test Vector PAR = 7.7 dB with −1 dBFS Back Off (Mode 9C), Channel Interpolation 3×, Main Interpolation 8×*

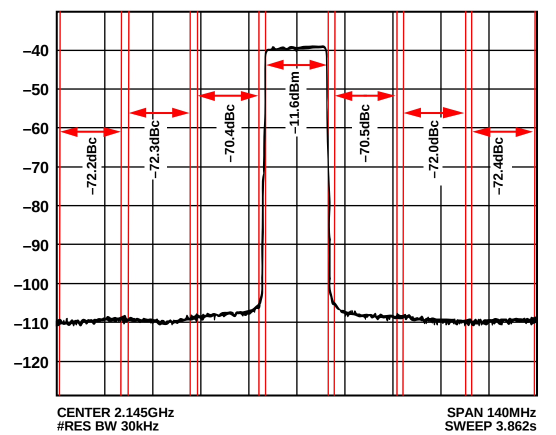



*Figure 34. Dual Band ACLR Performance for 20 MHz LTE at $f_{OUT}$ = 2.145 GHz and $f_{DAC}$ = 11.796 GSPS, Test Vector PAR = 7.7 dB with −1 dBFS Back Off (Mode 9C), Channel Interpolation 3×, Main Interpolation 8×*

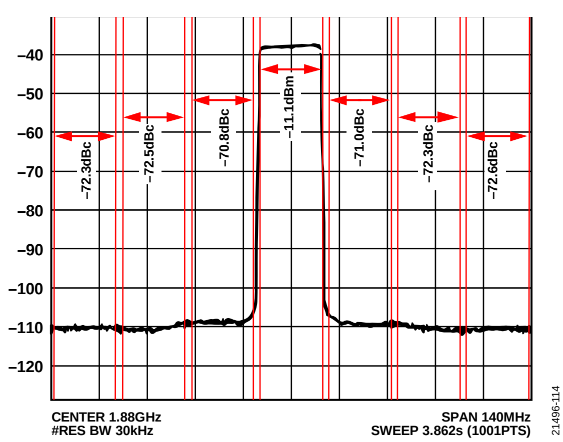



*Figure 32. Dual Band ACLR Performance for 20 MHz LTE at $f_{OUT}$ = 1.88 GHz and $f_{DAC}$ = 11.796 GSPS, Test Vector PAR = 7.7 dB with −1 dBFS Back Off (Mode 9C), Channel Interpolation 3×, Main Interpolation 8×*

## ADC

Sampling rate = 6 GSPS with clock frequency ($f_{CLK}$) = 6 GHz direct RF clock of 6 GHz, Nyquist mode operation (no decimation) with JESD204 interface mode = 19B, timing calibration disabled with ±100 MHz region centered on Nyquist zone transition, $T_A$ = 25°C, 128 K FFT sample with no averaging and $A_{IN}$ = −1 dBFS, ADCx input, and DAC powered down, unless otherwise noted.

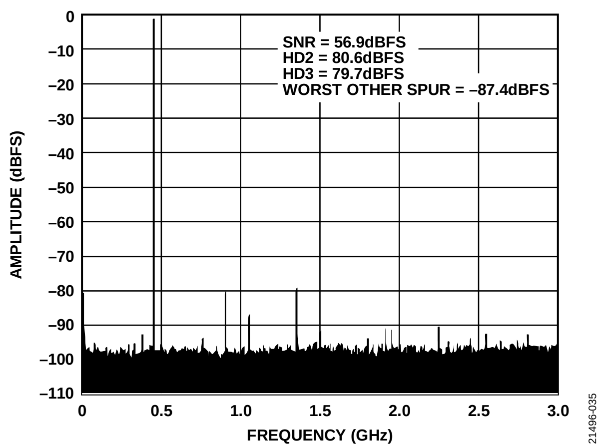



*Figure 35. Single-Tone FFT at $f_{IN}$ = 450 MHz*

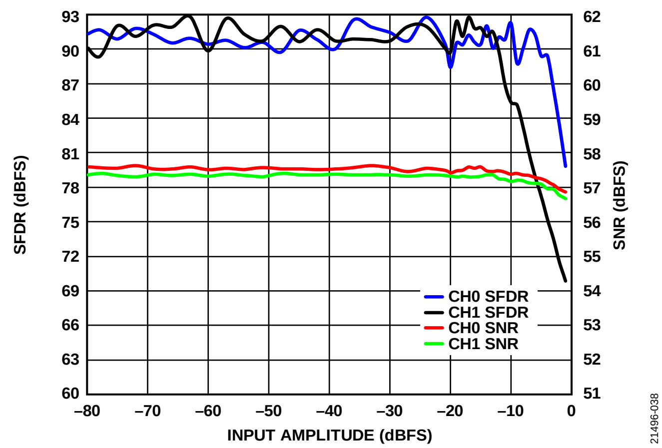



*Figure 38. Single-Tone SFDR and SNR vs. Input Amplitude at $f_{IN}$ = 450 MHz*

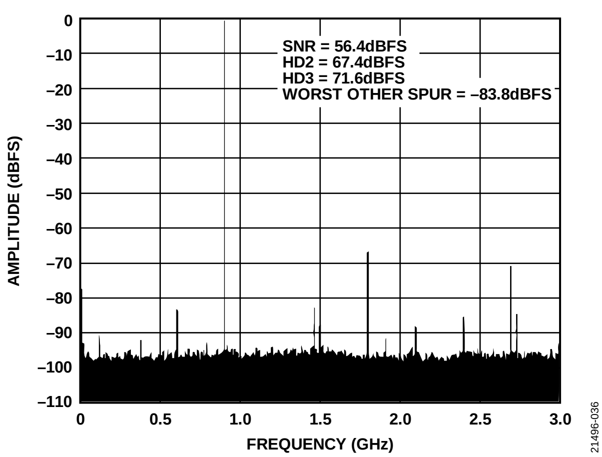



*Figure 36. Single-Tone FFT at $f_{IN}$ = 900 MHz*

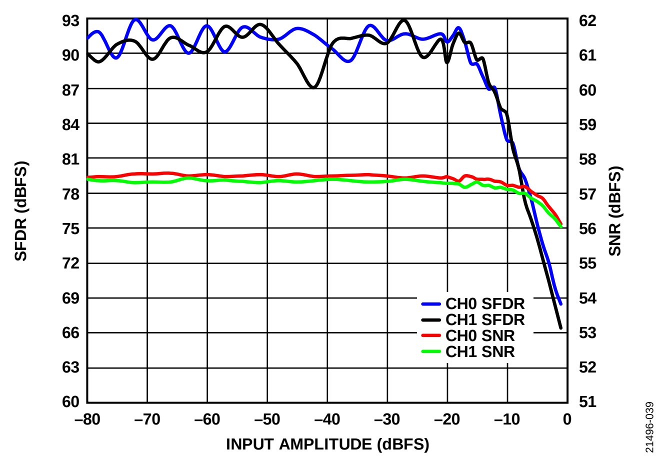



*Figure 39. Single-Tone SFDR and SNR vs. Input Amplitude at $f_{IN}$ = 900 MHz*

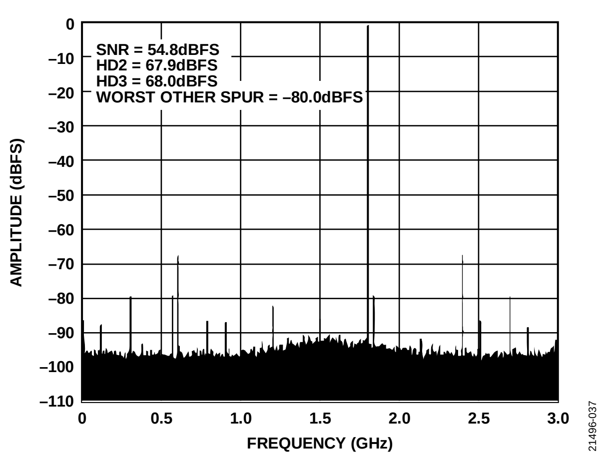



*Figure 37. Single-Tone FFT at $f_{IN}$ = 1.8 GHz*

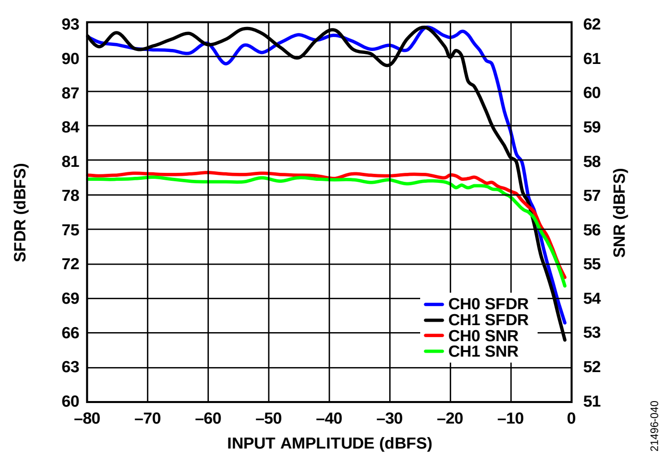



*Figure 40. Single-Tone SFDR and SNR vs. Input Amplitude at $f_{IN}$ = 1.8 GHz*

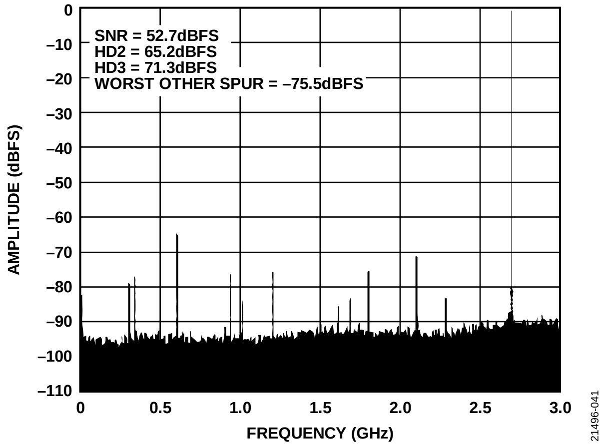



Figure 41. Single-Tone FFT at $f_{IN}$ = 2.7 GHz

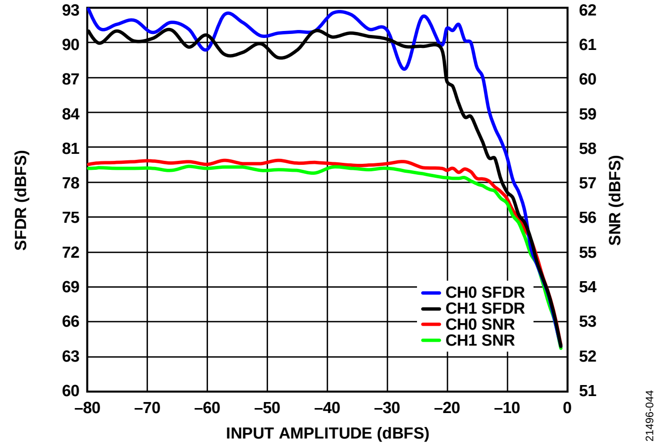



Figure 44. Single-Tone SFDR and SNR vs. Input Amplitude at $f_{IN}$ = 2.7 GHz

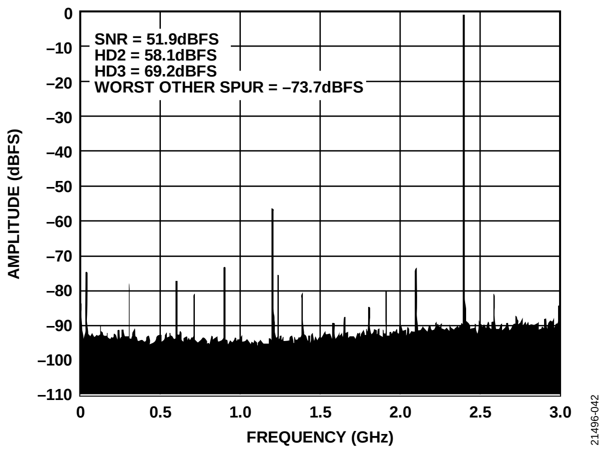



Figure 42. Single-Tone FFT at $f_{IN}$ = 3.6 GHz

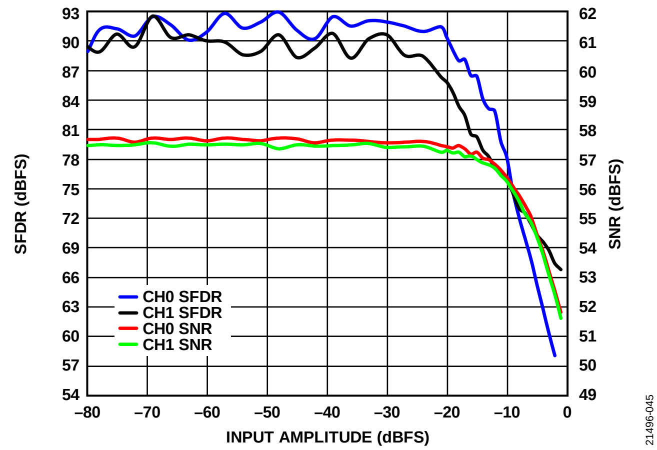



Figure 45. Single-Tone SFDR and SNR vs. Input Amplitude at $f_{IN}$ = 3.6 GHz

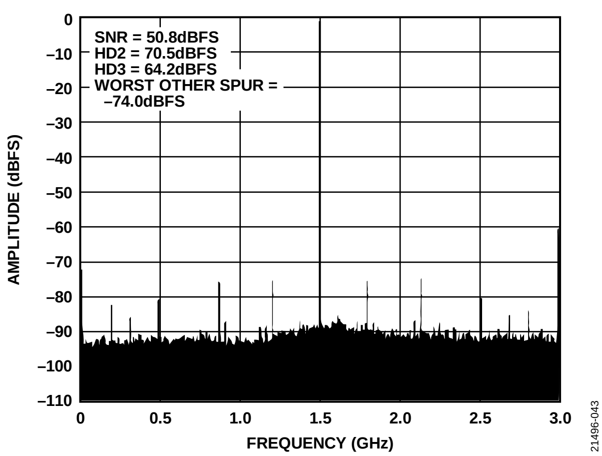



Figure 43. Single-Tone FFT at $f_{IN}$ = 4.5 GHz

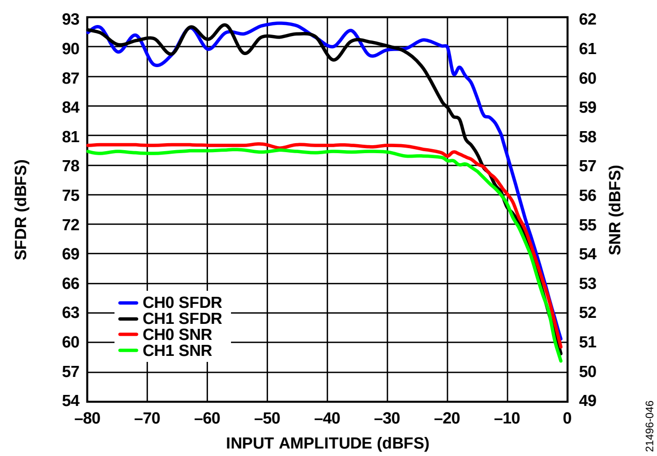



Figure 46. Single-Tone SFDR and SNR vs. Input Amplitude at $f_{IN}$ = 4.5 GHz

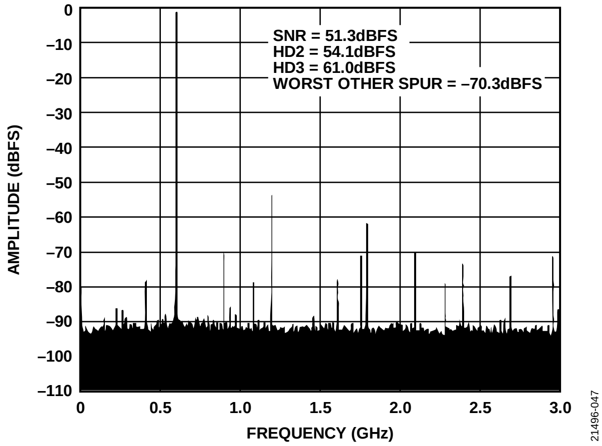



Figure 47. Single-Tone FFT at $f_{IN}$ = 5.4 GHz

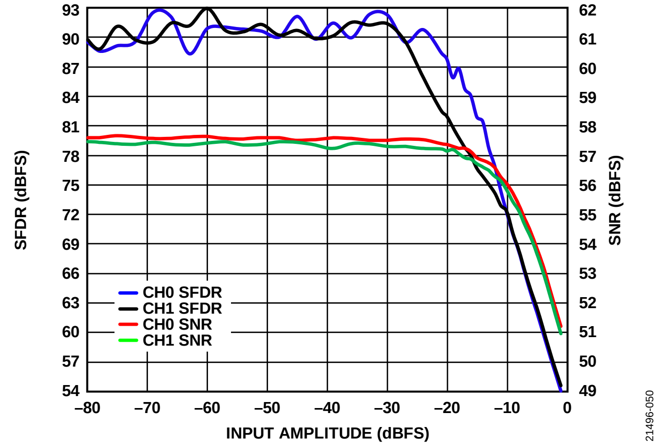



Figure 50. Single-Tone SFDR and SNR vs. Input Amplitude at $f_{IN}$ = 5.4 GHz

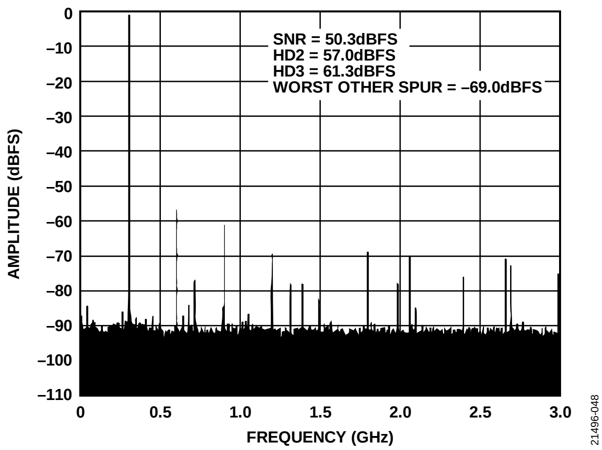



Figure 48. Single-Tone FFT at $f_{IN}$ = 6.3 GHz

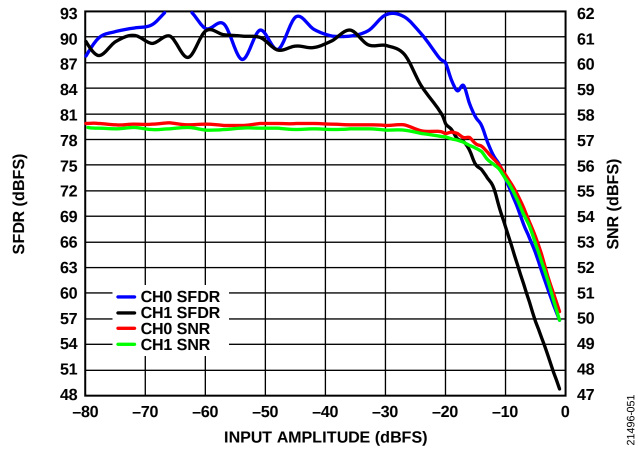



Figure 51. Single-Tone SNR/SFDR vs. Input Amplitude at $f_{IN}$ = 6.3 GHz

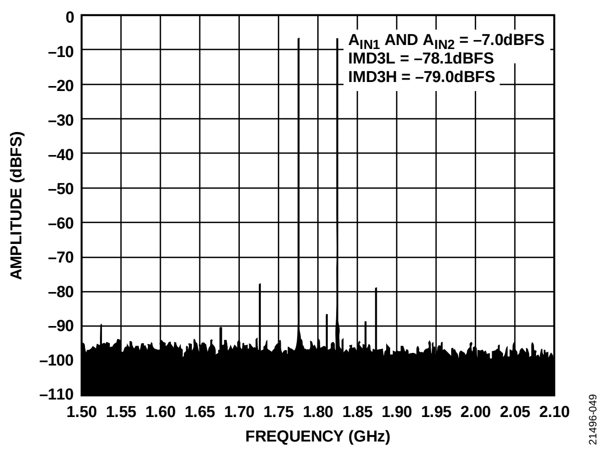



Figure 49. Two-Tone FFT, $f_{IN1}$ = 1.775 GHz, $f_{IN2}$ = 1.825 GHz, and $A_{IN1}$ and $A_{IN2}$ = −7 dBFS (Note That IMD3L and IMD3H Are the Lower and Higher IMD3 Product Components in dBFS.)

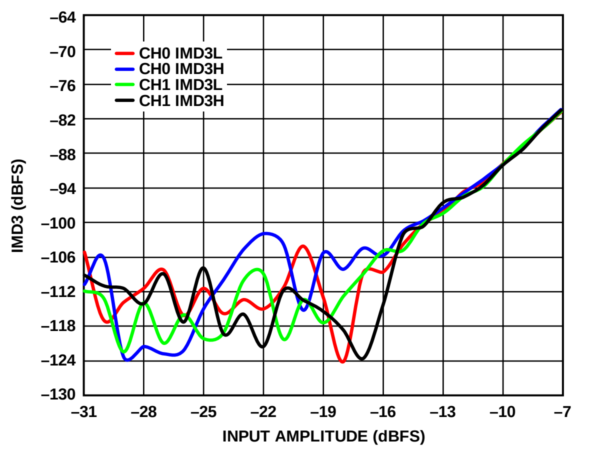



Figure 52. Two-Tone IMD3 vs. Input Amplitude with $f_{IN1}$ = 1.775 GHz, $f_{IN2}$ = 1.825 GHz

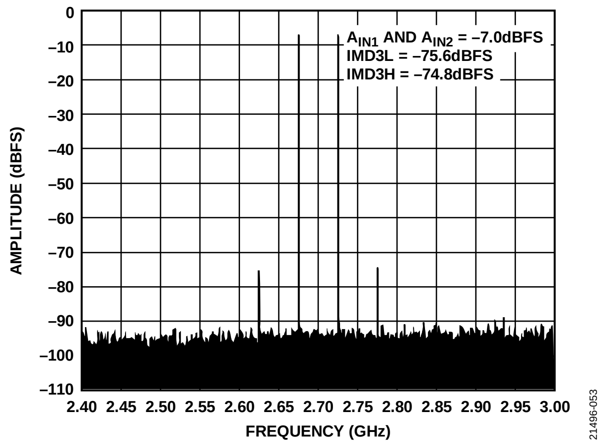



*Figure 53. Two-Tone FFT, $f_{IN1}$ = 2.675 GHz, $f_{IN2}$ = 2.725 GHz, and $A_{IN1}$ and $A_{IN2}$ = −7 dBFS*

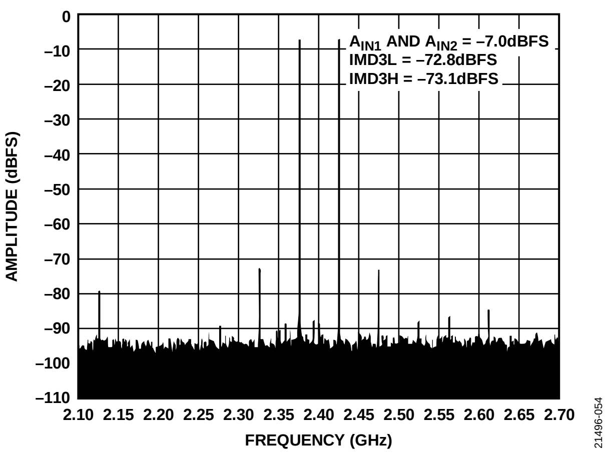



*Figure 54. Two-Tone FFT, $f_{IN1}$ = 3.575 GHz, $f_{IN2}$ = 3.625 GHz, and $A_{IN1}$ and $A_{IN2}$ = −7 dBFS*

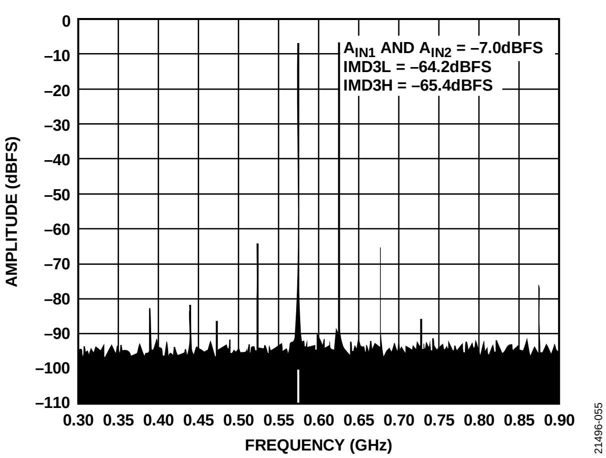



*Figure 55. Two-Tone FFT, $f_{IN1}$ = 5.375 GHz, $f_{IN2}$ = 5.425 GHz, and $A_{IN1}$ and $A_{IN2}$ = −7 dBFS*

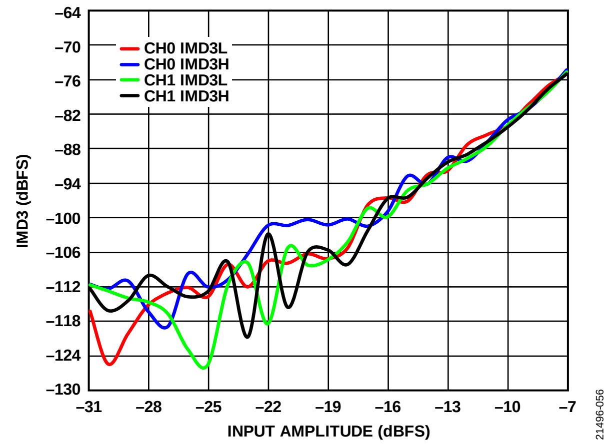



*Figure 56. Two-Tone IMD3 vs. Input Amplitude with $f_{IN1}$ = 2.675 GHz and $f_{IN2}$ = 2.725 GHz*

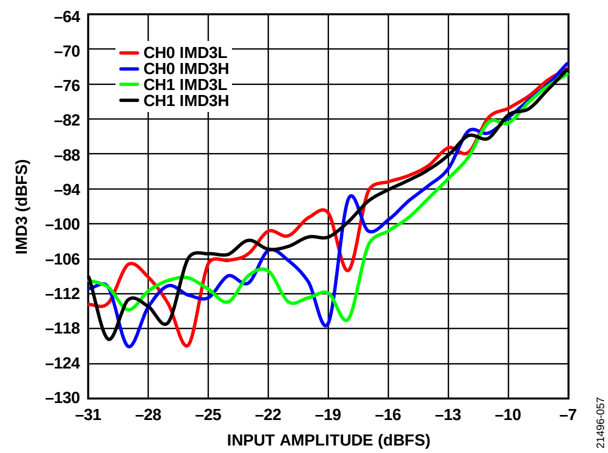



*Figure 57. Two-Tone IMD3 vs. Input Amplitude with $f_{IN1}$ = 3.575 GHz and $f_{IN2}$ = 3.625 GHz*

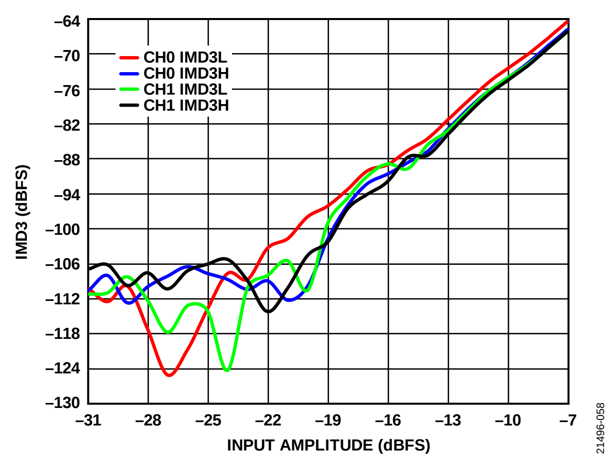



*Figure 58. Two-Tone IMD3 vs. Input Amplitude with $f_{IN1}$ = 5.375 GHz and $f_{IN2}$ = 5.425 GHz*

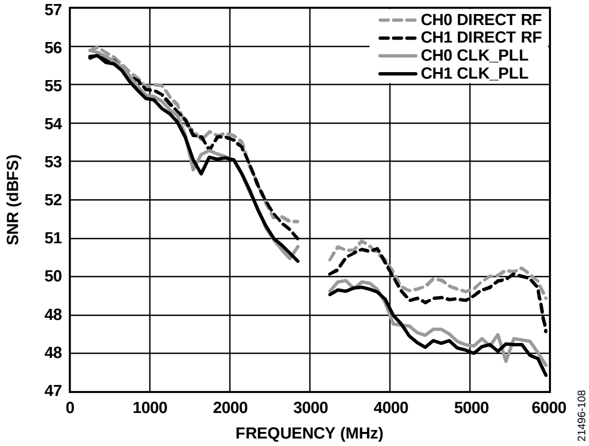



Figure 59. SNR vs. Frequency with $A_{IN}$ =−1 dBFS Between Direct External RF Clock = 6 GHz and PLL Clock Multiplier Enabled with Reference Input of 125 MHz

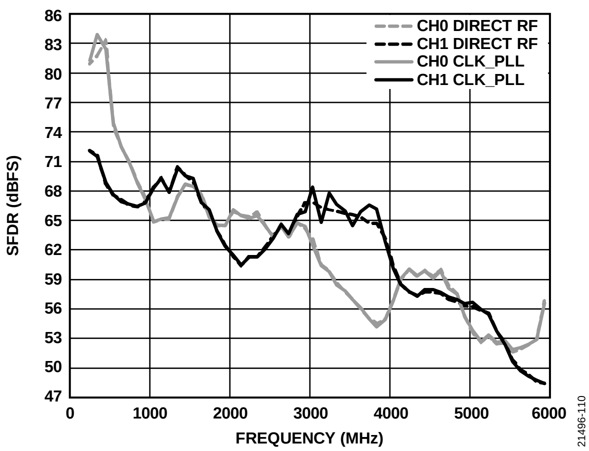



Figure 60. SFDR vs. Frequency with $A_{IN}$ = −1 dBFS Between Direct External RF Clock = 6 GHz and PLL Clock Multiplier Enabled with Reference Input of 125 MHz

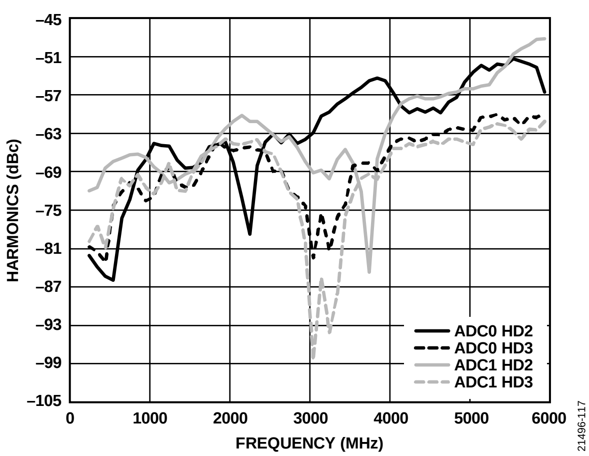



Figure 61. Harmonics (HD2 and HD3) vs. Frequency with $A_{IN}$ = −1 dBFS

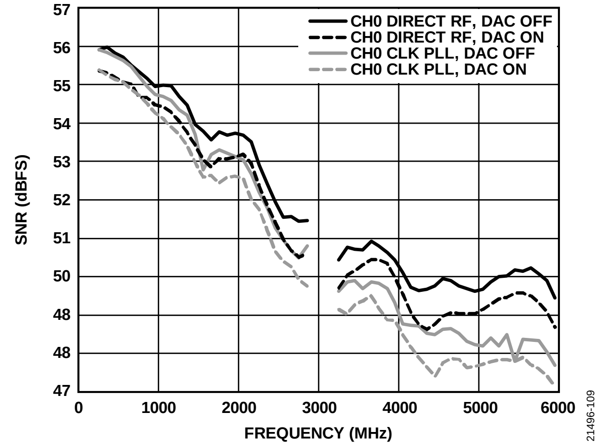



Figure 62. SNR vs. Frequency with $A_{IN}$ = −1 dBFS with DAC On/Off and PLL On/Off Between Direct External RF Clock = 6 GHz and PLL Clock Multiplier Enabled with Reference Input of 125 MHz

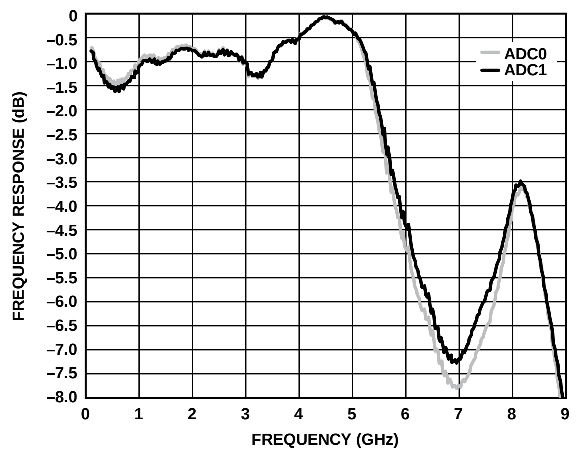



Figure 63. Measured Input Bandwidth of ADC0 and ADC1 Input Using Marki Microwave BALH-0009 on AD9082-FMCA-EBZ (No Matching Network), De-Embedded −3 dB ADC Bandwidth Is Equal to 8 GHz

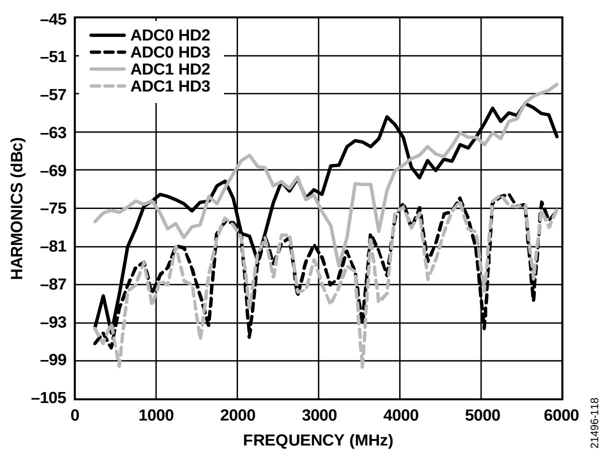



Figure 64. Harmonics (HD2 and HD3) vs. Frequency with $A_{IN}$ = −9 dBFS

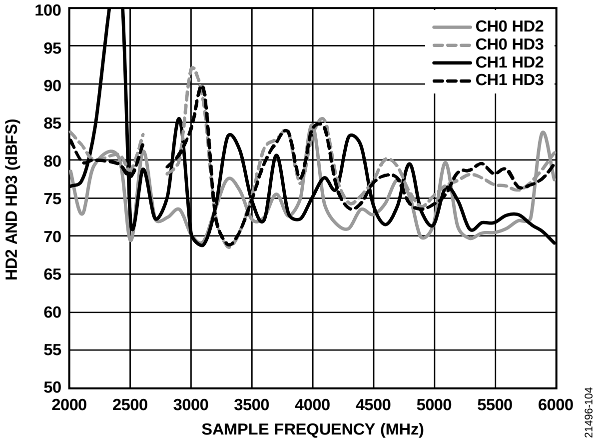



Figure 65. HD2 and HD3 vs. Sample Frequency ($f_S$), $f_{IN}$ = 450 MHz, $A_{IN}$ = −1 dBFS, $f_S$ = 2 GSPS to 6 GSPS

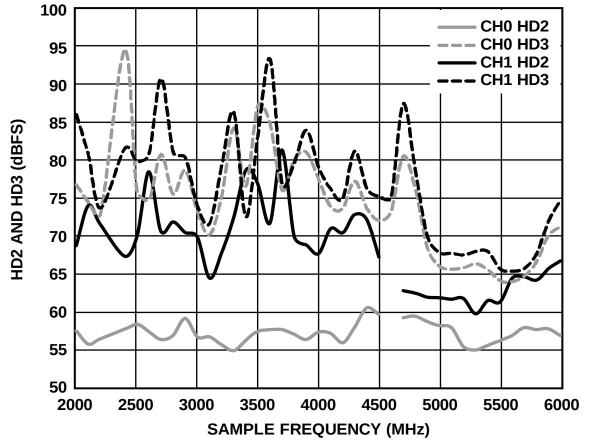



Figure 68. HD2 and HD3 vs. Sample Frequency, $f_{IN}$ = 3450 MHz, $A_{IN}$ = −1 dBFS, $f_S$ = 2 GSPS to 6 GSPS

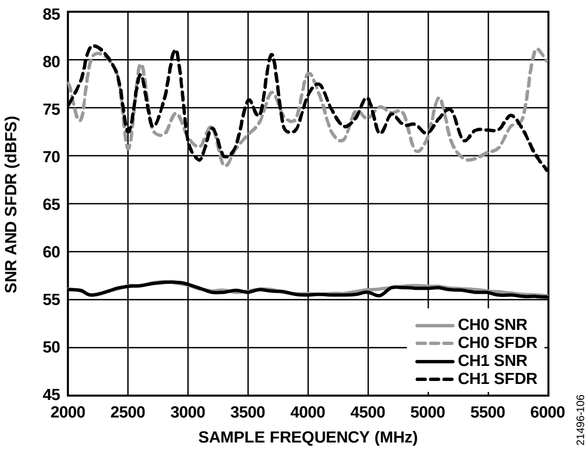



Figure 66. SNR and SFDR vs. Sample Frequency, $f_{IN}$ = 450 MHz, $A_{IN}$ = −1 dBFS, $f_S$ = 2 GSPS to 6 GSPS

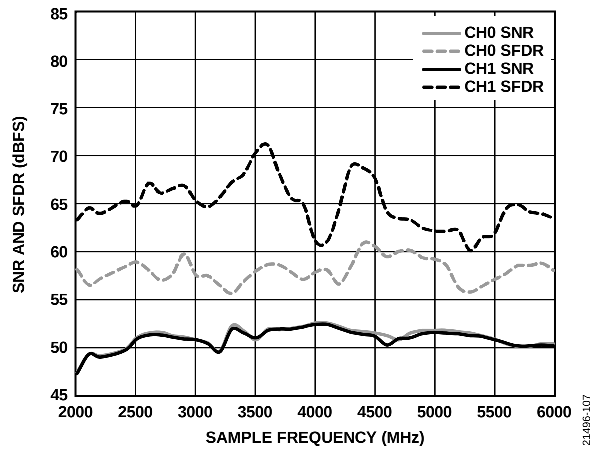



Figure 69. SNR and SFDR vs. Sample Frequency, $f_{IN}$ = 3450 MHz, $A_{IN}$ = −1 dBFS, $f_S$ = 2 GSPS to 6 GSPS

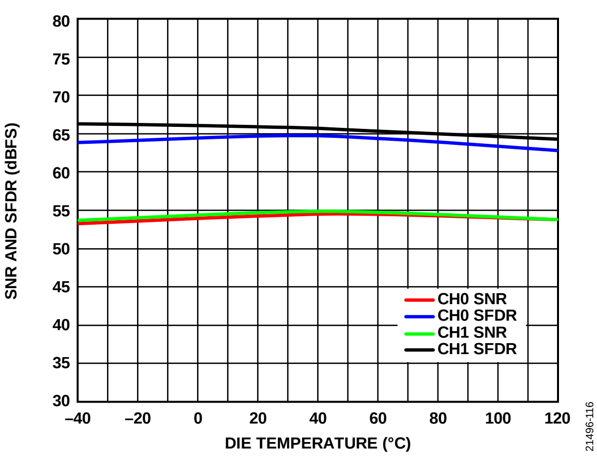



Figure 67. SFDR and SNR vs. Die Temperature, $f_{IN}$= 1.85 GHz, $A_{IN}$ = −1 dBFS

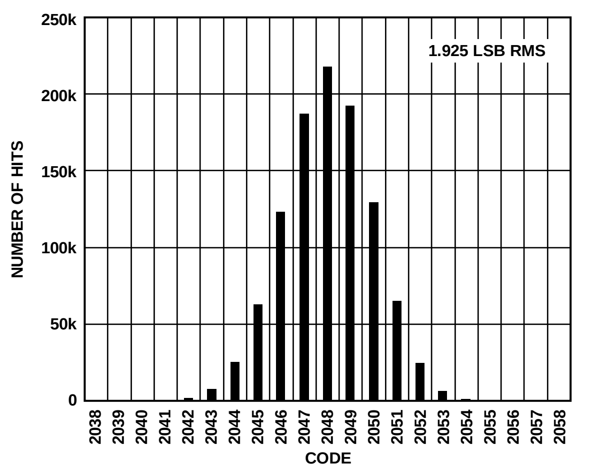



Figure 70. Input Referred Noise Histogram

# THEORY OF OPERATION

The AD9082 is a highly integrated, 28 nm, RF, MxFE featuring four 16-bit, 12 GSPS DAC cores and two 12-bit, 6 GSPS ADC cores (see Figure 1). The DAC core is based on a current segmentation architecture providing a differential complementary current output with an adjustable full-scale output ($I_{OUTFS}$) range of 7 mA to 40 mA. The ADC core is based on a proprietary interleaved architecture that suppresses residual interleaving spurious products into the noise floor. To enable wide bandwidth operation, a high linearity 100 Ω differential buffer with overload protection is used to isolate the ADC core from the RF ADC driver source. An on-chip clock multiplier can be used to synthesize the RF DAC and ADC clocks or, alternatively, an external clock can be applied.

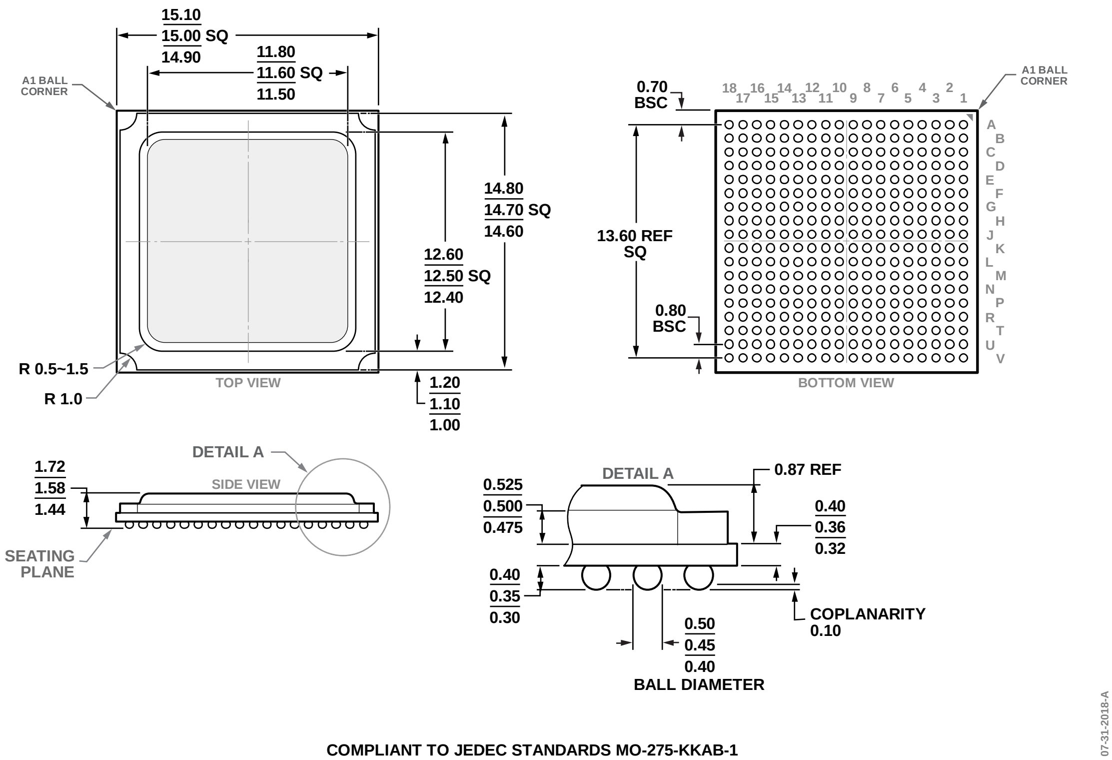
Flexible transmit and receive DSP paths are available to up and down sample the desired intermediate frequency (IF) or RF signal(s) to manageable data interface rates aligned with bandwidth requirements. The transmit and receive DSP paths are symmetric and consist of four coarse digital upconversion (DUC) and digital downconversion (DDC) blocks in the main datapath along with eight fine DUC and DDC blocks in the channelizer datapath. Each block includes a 48-bit NCO configurable for integer or fractional mode of operation. The channelizer datapath enables an efficient implementation to support multiband applications where up to eight RF bands can be supported. Each of the DUC and DDC blocks are bypassable and offer flexible interpolating and decimation factors. The NCO in each block also supports coherent frequency hopping.

Additional features are also included in the receive and transmit datapaths as well as elsewhere to facilitate system integration. Both datapaths include adjustable delay lines to compensate for mismatch in channel delay paths that may occur external to the device. The transmit datapath includes digital gain control, fine delay adjust, and power amplifier protection to simplify DPD integration in a multiband transmitter. The receive path includes a flexible programmable 192-tap finite impulse response (PFIR) filter. The filter can be allocated across one or more ADCs for receive equalization with support for four different profiles. These profiles can be selected using the GPIOx pins. The receive datapath also includes a fast and slow signal detection capability in support of automatic gain control (AGC). Transmit and receive data formatting can be real or complex with resolutions of 8, 12, 16, and 24 bits depending on the JESD204B or the JESD204C mode. The AD9082 also allows complete bypass of the transmit and receive DSP paths enabling Nyquist operation.

The device also supports fast frequency hopping via GPIOx and a low latency digital loopback capability. An on-chip TMU is also included and can be used as part of a thermal management solution. Power savings option in support of time division duplex (TDD) applications are included.

A 16-lane JESD204 transceiver port is available to support the high data throughput rates on the receive and transmit datapaths. Eight SERDES lanes are designated for the transmit datapaths, while the other 8 lanes are designated for the receive datapaths with the option to support two links. The transceiver port supports JESD204C up to 16.22 GSPS or JESD204B up to 15.5 GSPS lane rates. The JESD204 data link layer is highly flexible allowing optimization of the lane count (or rate) required to support a target throughput rate. Internal synchronization for deterministic latency and phase alignment as well as multichip synchronization are possible via an external alignment signal (SYSREF).

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MO-275-KKAB-1

*Figure 71. 324-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]*
*(BP-324-3)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD9082BBPZ-4D2AC | −40°C to +85°C | 324-Ball Ball Grid Array, Thermally Enhanced [BGA_ED], JESD204B and JESD204C | BP-324-3 |
| AD9082BBPZRL-4D2AC | −40°C to +85°C | 324-Ball Ball Grid Array, Thermally Enhanced [BGA_ED], JESD204B and JESD204C | BP-324-3 |
| AD9082-FMCA-EBZ | | AD9082 Evaluation Board with High Performance Analog Network | |

[1] Z = RoHS Compliant Part.


D21496-9/20(A)

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