

Features

- ◆ 64K x 16 advanced high-speed CMOS Static RAM
- ◆ Equal access and cycle times
  - Commercial: 12/15/20ns
  - Industrial: 15/20ns
- ◆ One Chip Select plus one Output Enable pin
- ◆ Bidirectional data inputs and outputs directly TTL-compatible
- ◆ Low power consumption via chip deselect
- ◆ Upper and Lower Byte Enable Pins
- ◆ Commercial and industrial product available in 44-pin Plastic SOJ package and 44-pin TSOP package

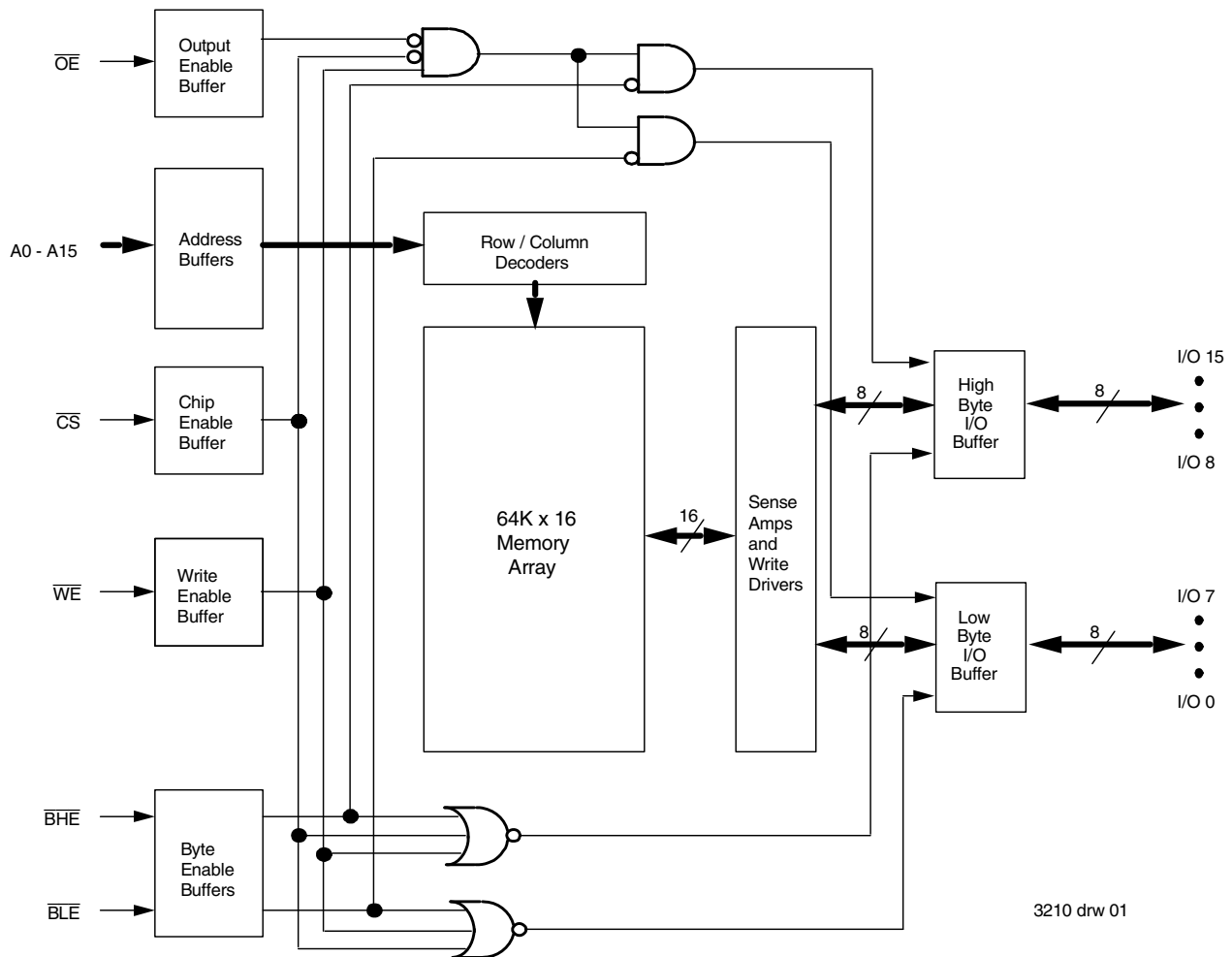
Description

The IDT71016 is a 1,048,576-bit high-speed Static RAM organized as 64K x 16. It is fabricated using high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

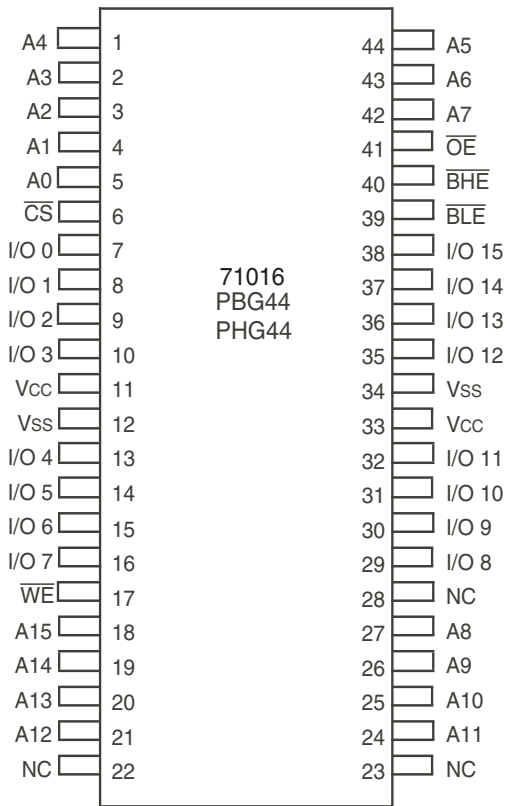
The IDT71016 has an output enable pin which operates as fast as 7ns, with address access times as fast as 12ns. All bidirectional inputs and outputs of the IDT71016 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71016 is packaged in a JEDEC standard 44-pin Plastic SOJ and 44-pin TSOP Type II.

Functional Block Diagram



Pin Configurations<sup>(1)</sup>



SOJ/TSOP  
Top View

3210 drw 02

Pin Descriptions

A0 - A15	Address Inputs	Input
$\overline{CS}$	Chip Select	Input
$\overline{WE}$	Write Enable	Input
$\overline{OE}$	Output Enable	Input
$\overline{BHE}$	High Byte Enable	Input
$\overline{BLE}$	Low Byte Enable	Input
I/O <sub>0</sub> - I/O <sub>15</sub>	Data Input/Output	I/O
Vcc	5.0V Power	Pwr
Vss	Ground	Gnd

3210 tbl 01

NOTE:

1. This text does not indicate orientation of actual part-marking.

Truth Table<sup>(1)</sup>

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>0</sub> - I/O <sub>7</sub>	I/O <sub>8</sub> - I/O <sub>15</sub>	Function
H	X	X	X	X	High-Z	High-Z	Deselected - Standby
L	L	H	L	H	DATAOUT	High-Z	Low Byte Read
L	L	H	H	L	High-Z	DATAOUT	High Byte Read
L	L	H	L	L	DATAOUT	DATAOUT	Word Read
L	X	L	L	L	DATAIN	DATAIN	Word Write
L	X	L	L	H	DATAIN	High-Z	Low Byte Write
L	X	L	H	L	High-Z	DATAIN	High Byte Write
L	H	H	X	X	High-Z	High-Z	Outputs Disabled
L	X	X	H	H	High-Z	High-Z	Outputs Disabled

3210 tbl 02

NOTE:

1. H = V<sub>H</sub>, L = V<sub>IL</sub>, X = Don't care.

### Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Value	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	°C
P <sub>T</sub>	Power Dissipation	1.25	W
I <sub>OUT</sub>	DC Output Current	50	mA

**NOTES:**

3210 tbl 03a

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>TERM</sub> must not exceed V<sub>CC</sub> + 0.5V.

### Recommended Operating Temperature and Supply Voltage

Grade	Temperature	GND	V <sub>CC</sub>
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

3210 tbl 04

### Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	—	V <sub>DD</sub> + 0.5	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

**NOTE:**

3210 tbl 05

- V<sub>IL</sub> (min.) = -1.5V for pulse width less than t<sub>RC</sub>/2, once per cycle.

### Capacitance

(T<sub>A</sub> = +25°C, f = 1.0MHz, SOJ/TSOP Package)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 3dV	6	pF
C <sub>I/O</sub>	I/O Capacitance	V <sub>OUT</sub> = 3dV	7	pF

**NOTE:**

3210 tbl 06

- This parameter is guaranteed by device characterization, but not production tested.

### DC Electrical Characteristics

(V<sub>CC</sub> = 5.0V ± 10%, Commercial and Industrial Temperature Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I <sub>L</sub>	Input Leakage Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND to V <sub>CC</sub>	—	5	μA
I <sub>O</sub>	Output Leakage Current	V <sub>CC</sub> = Max., $\overline{CS}$ = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>	—	5	μA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8mA, V <sub>CC</sub> = Min.	—	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4mA, V <sub>CC</sub> = Min.	2.4	—	V

3210 tbl 07

### DC Electrical Characteristics<sup>(1)</sup>

(V<sub>CC</sub> = 5.0V ± 10%, V<sub>LC</sub> = 0.2V, V<sub>HC</sub> = V<sub>CC</sub> - 0.2V)

Symbol	Parameter	71016S12	71016S15		71016S20		Unit
		Com'l.	Com'l.	Ind.	Com'l.	Ind.	
I <sub>CC</sub>	Dynamic Operating Current $\overline{CS} \leq V_{IL}$ , Outputs Open, V <sub>CC</sub> = Max., f = f <sub>MAX</sub> <sup>(2)</sup>	210	180	180	170	170	mA
I <sub>SB</sub>	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$ , Outputs Open, V <sub>CC</sub> = Max., F = f <sub>MAX</sub> <sup>(2)</sup>	60	50	50	45	45	mA
I <sub>SB1</sub>	Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$ , Outputs Open, V <sub>CC</sub> = Max., f = 0 <sup>(2)</sup> V <sub>IN</sub> ≤ V <sub>LC</sub> or V <sub>IN</sub> ≥ V <sub>HC</sub>	10	10	10	10	10	mA

**NOTES:**

3210 tbl 08

- All values are maximum guaranteed values.
- f<sub>MAX</sub> = 1/t<sub>RC</sub> (all address inputs are cycling at f<sub>MAX</sub>); f = 0 means no address input lines are changing.

## AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1.5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figure 1, 2 and 3

3210 tbl 09

## AC Test Loads

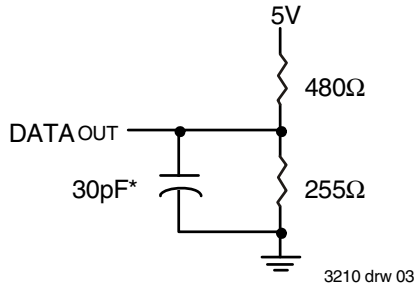


Figure 1. AC Test Load

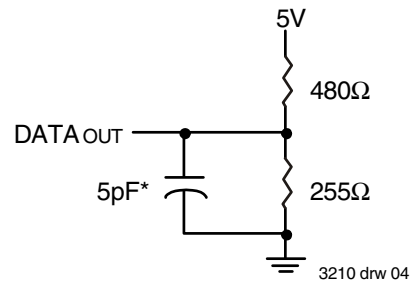


Figure 2. AC Test Load  
(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, and tWHZ)

\*Including jig and scope capacitance.

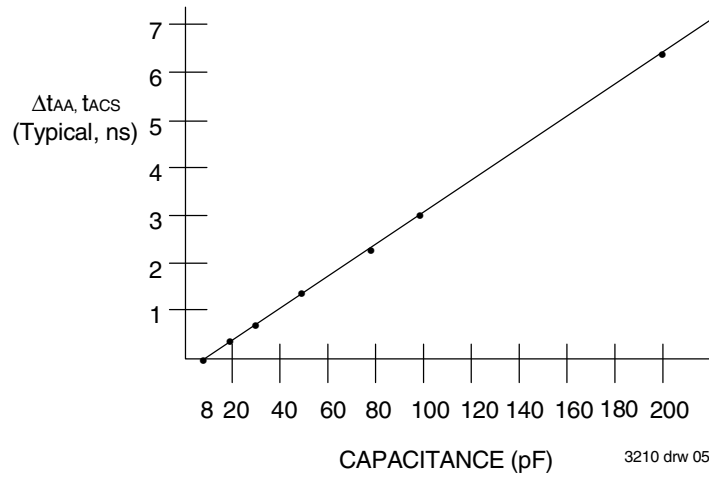


Figure 3. Output Capacitive Derating

AC Electrical Characteristics (V<sub>CC</sub> = 5.0V ± 10%, Commercial and Industrial Range)

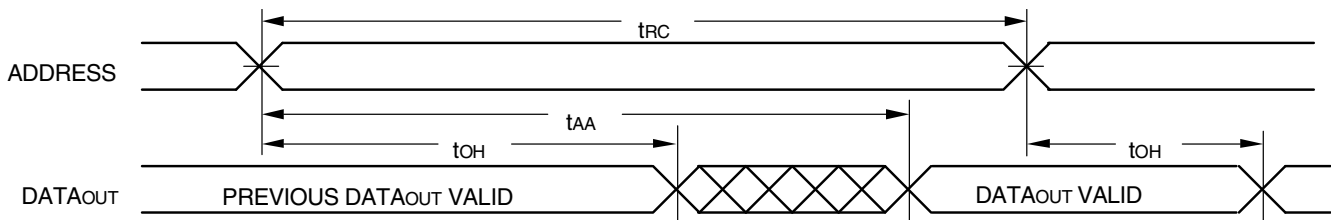
Symbol	Parameter	71016S12 <sup>(2)</sup>		71016S15		71016S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>								
t <sub>RC</sub>	Read Cycle Time	12	—	15	—	20	—	ns
t <sub>AA</sub>	Address Access Time	—	12	—	15	—	20	ns
t <sub>ACS</sub>	Chip Select Access Time	—	12	—	15	—	20	ns
t <sub>CLZ</sub> <sup>(1)</sup>	Chip Select Low to Output in Low-Z	4	—	5	—	5	—	ns
t <sub>CHZ</sub> <sup>(1)</sup>	Chip Select High to Output in High-Z	—	6	—	6	—	8	ns
t <sub>OE</sub>	Output Enable Low to Output Valid	—	7	—	8	—	10	ns
t <sub>OLZ</sub> <sup>(1)</sup>	Output Enable Low to Output in Low-Z	0	—	0	—	0	—	ns
t <sub>OHZ</sub> <sup>(1)</sup>	Output Enable High to Output in High-Z	—	6	—	6	—	8	ns
t <sub>OH</sub>	Output Hold from Address Change	4	—	4	—	5	—	ns
t <sub>BE</sub>	Byte Enable Low to Output Valid	—	7	—	8	—	10	ns
t <sub>BLZ</sub> <sup>(1)</sup>	Byte Enable Low to Output in Low-Z	0	—	0	—	0	—	ns
t <sub>BHZ</sub> <sup>(1)</sup>	Byte Enable High to Output in High-Z	—	6	—	6	—	8	ns
<b>WRITE CYCLE</b>								
t <sub>WC</sub>	Write Cycle Time	12	—	15	—	20	—	ns
t <sub>AW</sub>	Address Valid to End of Write	9	—	10	—	12	—	ns
t <sub>CW</sub>	Chip Select Low to End of Write	9	—	10	—	12	—	ns
t <sub>BW</sub>	Byte Enable Low to End of Write	9	—	10	—	12	—	ns
t <sub>AS</sub>	Address Set-up Time	0	—	0	—	0	—	ns
t <sub>WR</sub>	Address Hold from End of Write	0	—	0	—	0	—	ns
t <sub>WP</sub>	Write Pulse Width	9	—	10	—	12	—	ns
t <sub>DW</sub>	Data Valid to End of Write	7	—	8	—	10	—	ns
t <sub>DH</sub>	Data Hold Time	0	—	0	—	0	—	ns
t <sub>OW</sub> <sup>(1)</sup>	Write Enable High to Output in Low-Z	1	—	1	—	1	—	ns
t <sub>WHZ</sub> <sup>(1)</sup>	Write Enable Low to Output in High-Z	—	6	—	6	—	8	ns

NOTE:

1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.
2. 12ns commercial only.

3210 tbl 10

Timing Waveform of Read Cycle No. 1<sup>(1,2,3)</sup>

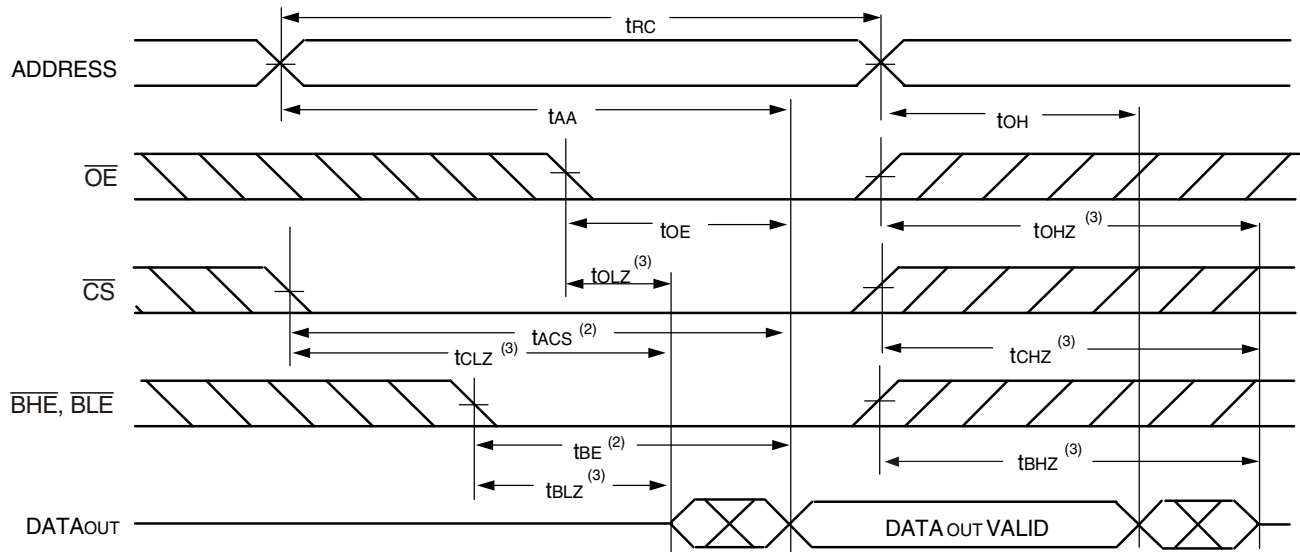


NOTES:

1.  $\overline{WE}$  is HIGH for Read Cycle.
2. Device is continuously selected,  $\overline{CS}$  is LOW.
3.  $\overline{OE}$ ,  $\overline{BHE}$ , and  $\overline{BLE}$  are LOW.

3210 drw 06

### Timing Waveform of Read Cycle No. 2<sup>(1)</sup>

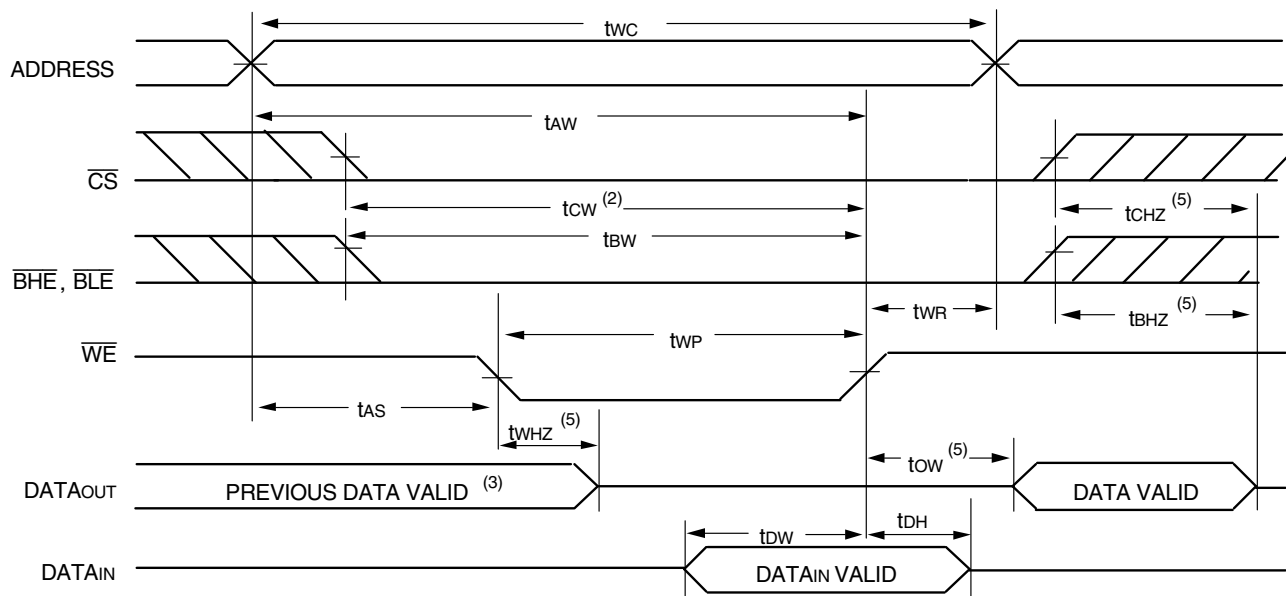


3210 drw 07

**NOTES:**

1.  $\overline{WE}$  is HIGH for Read Cycle.
2. Address must be valid prior to or coincident with the later of  $\overline{CS}$ ,  $\overline{BHE}$ , or  $\overline{BLE}$  transition LOW; otherwise tAA is the limiting parameter.
3. Transition is measured  $\pm 200\text{mV}$  from steady state.

### Timing Waveform of Write Cycle No. 1 ( $\overline{WE}$ Controlled Timing)<sup>(1,2,4)</sup>

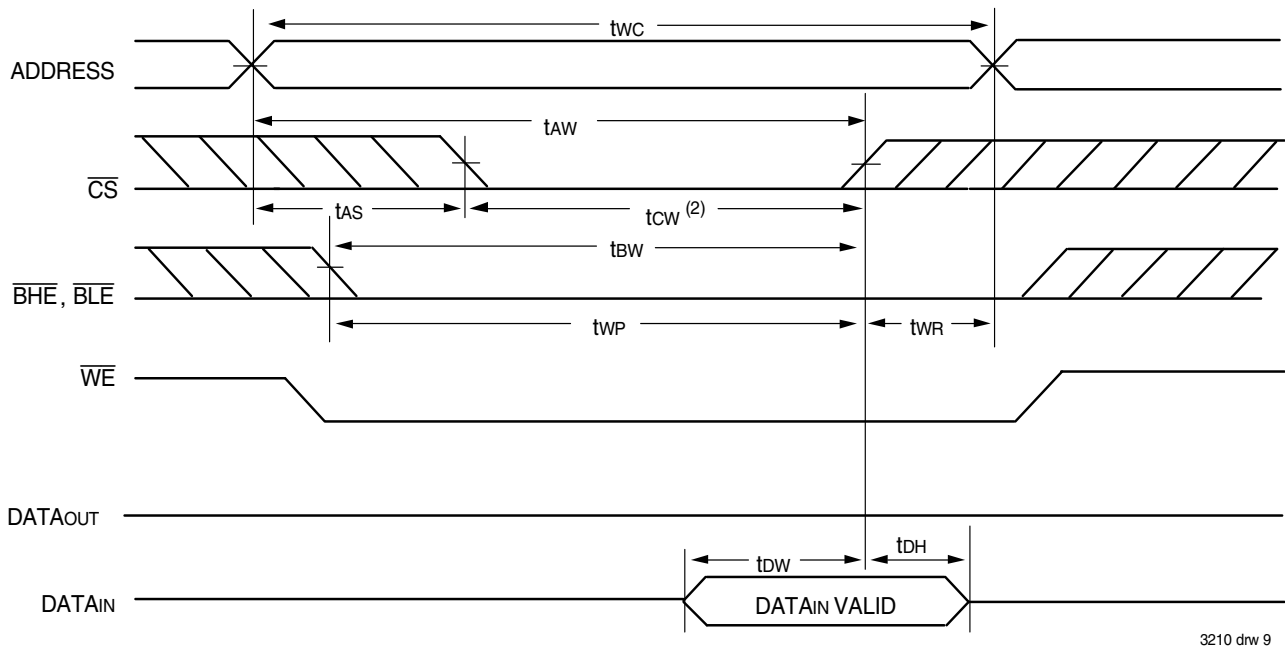


3210 drw 08

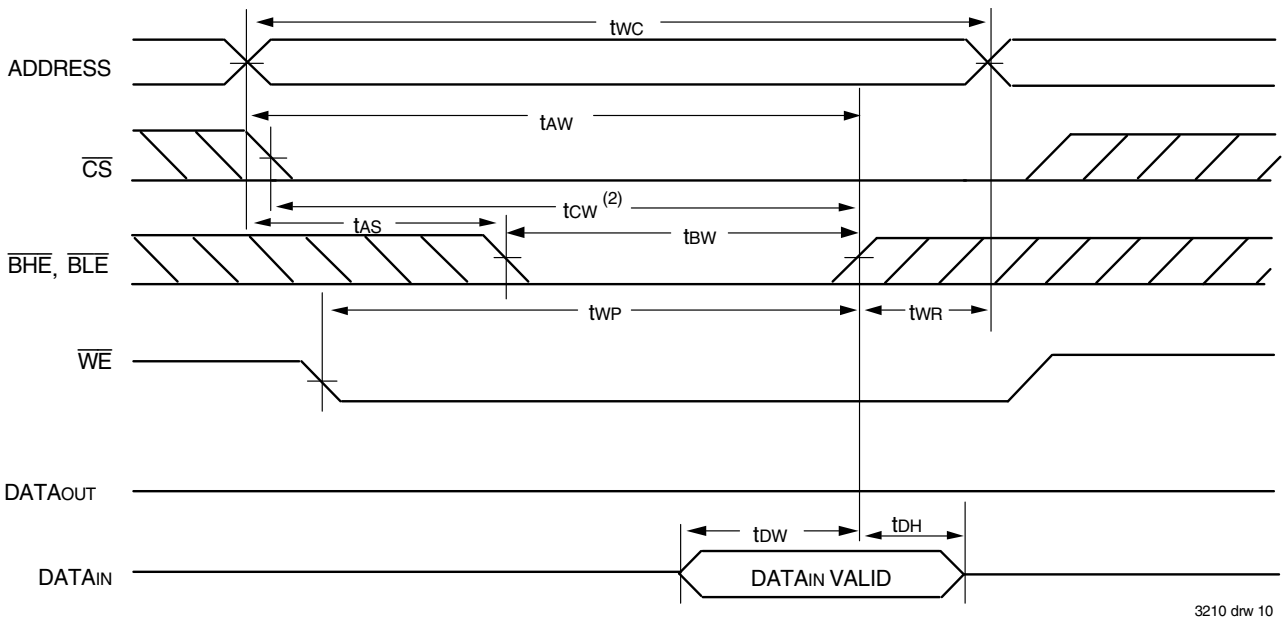
**NOTES:**

1. A write occurs during the overlap of a LOW  $\overline{CS}$ , LOW  $\overline{BHE}$  or  $\overline{BLE}$ , and a LOW  $\overline{WE}$ .
2.  $\overline{OE}$  is continuously HIGH. If during a  $\overline{WE}$  controlled write cycle  $\overline{OE}$  is LOW, twp must be greater than or equal to twhz + tbw to allow the I/O drivers to turn off and data to be placed on the bus for the required tow. If  $\overline{OE}$  is HIGH during a  $\overline{WE}$  controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified twp.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the  $\overline{CS}$  LOW or  $\overline{BHE}$  and  $\overline{BLE}$  LOW transition occurs simultaneously with or after the  $\overline{WE}$  LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured  $\pm 200\text{mV}$  from steady state.

Timing Waveform of Write Cycle No. 2 ( $\overline{\text{CS}}$  Controlled Timing)<sup>(1,4)</sup>



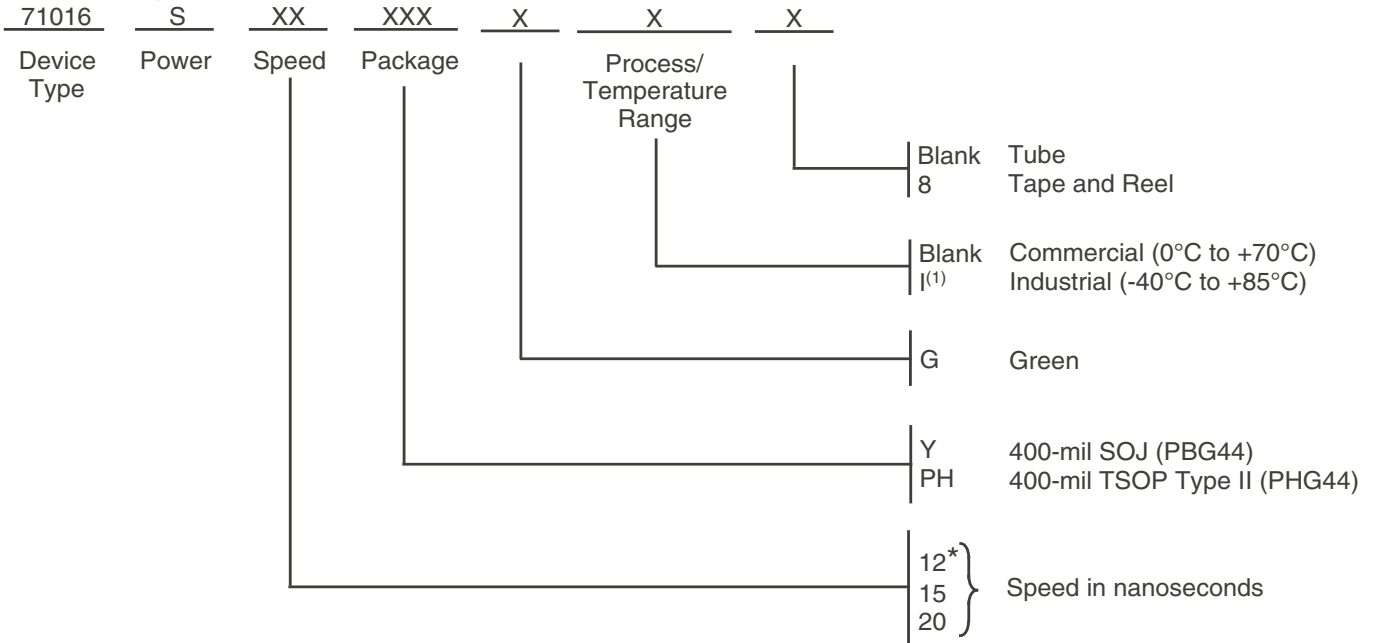
Timing Waveform of Write Cycle No. 3 ( $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$  Controlled Timing)<sup>(1,4)</sup>



NOTES:

1. A write occurs during the overlap of a LOW  $\overline{\text{CS}}$ , LOW  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}}$ , and a LOW  $\overline{\text{WE}}$ .
2.  $\overline{\text{OE}}$  is continuously HIGH. If during a  $\overline{\text{WE}}$  controlled write cycle  $\overline{\text{OE}}$  is LOW,  $t_{\text{WP}}$  must be greater than or equal to  $t_{\text{WHZ}} + t_{\text{OW}}$  to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{\text{OW}}$ . If  $\overline{\text{OE}}$  is HIGH during a  $\overline{\text{WE}}$  controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified  $t_{\text{WP}}$ .
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the  $\overline{\text{CS}}$  LOW or  $\overline{\text{BHE}}$  and  $\overline{\text{BLE}}$  LOW transition occurs simultaneously with or after the  $\overline{\text{WE}}$  LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured  $\pm 200\text{mV}$  from steady state.

### Ordering Information



3210 drw 11

**NOTE:**

1. Contact your local sales office for industrial temp range for other speeds, packages and powers.

\*Commercial temperature range only

### Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
12	71016S12PHG	PHG44	TSOP	C
	71016S12PHG8	PHG44	TSOP	C
	71016S12YG	PBG44	SOJ	C
	71016S12YG8	PBG44	SOJ	C
15	71016S15PHG	PHG44	TSOP	C
	71016S15PHG8	PHG44	TSOP	C
	71016S15PHGI	PHG44	TSOP	I
	71016S15PHG8I	PHG44	TSOP	I
	71016S15YG	PBG44	SOJ	C
	71016S15YG8	PBG44	SOJ	C
	71016S15YGI	PBG44	SOJ	I
	71016S15YG8I	PBG44	SOJ	I
20	71016S20PHG	PHG44	TSOP	C
	71016S20PHG8	PHG44	TSOP	C
	71016S20PHGI	PHG44	TSOP	I
	71016S20PHG8I	PHG44	TSOP	I
	71016S20YG	PBG44	SOJ	C
	71016S20YG8	PBG44	SOJ	C
	71016S20YGI	PBG44	SOJ	I
	71016S20YG8I	PBG44	SOJ	I



## Datasheet Document History

07/30/99:		Updated to new format
08/05/99:	Pg. 3	Expressed commercial and industrial ranges on DC Electrical table
	Pg. 5	Removed I <sub>CC</sub> , I <sub>SB</sub> , and I <sub>SB1</sub> values for S12 industrial speed
	Pg. 6	Expressed commercial and industrial ranges on AC Electrical table
	Pg. 7	Changed footnote #2 to commercial temperature only
	Pg. 8	Revised footnotes on Write Cycle No.1 diagram
		Revised footnotes on Write Cycle No.2 and No.3 diagrams
		Removed SCD 2752 footnote
		Added commercial only for 12ns speed
08/13/99:	Pg. 9	Added Datasheet Document History
09/30/99:	Pg. 3, 5, 8	Added 12ns industrial temperature speed grade offering
08/09/00:		Not recommended for new designs
02/01/01:		Removed "Not recommended for new designs"
01/30/04:	Pg. 8	Added "Restricted hazardous substance device" to order information
01/30/06:	Pg. 3	Updated Capacitance table to include TSOP
02/13/07:	Pg. 8	Added N generation die step to data sheet ordering information
10/13/08:	Pg. 8	Removed "IDT" from orderable part number
09/25/13:	Pg. 1	Updated Commercial and Industrial speed grade offerings
		Removed IDT reference to fabrication
	Pg. 3	Removed Commercial T <sub>A</sub> information from the Absolute Maximum Ratings table
		Removed Ind. temp values for the 12ns speed grade from the DC Elec Chars table
	Pg. 5	Added the footnote annotation to the AC Elec Chars table and the footnote for 12ns commercial only
	Pg. 8	Added T & R to, updated Restricted Hazardous Substance Device wording to "Green", added annotation indicating "Commercial temperature range only" and removed Die Stepping indicator from the ordering information
06/02/20:	Pg. 1 - 10	Rebranded as Renesas datasheet
	Pg. 2 & 8	Updated package codes
	Pg. 8	Added Industrial temp footnote to Ordering Information
	Pg. 8	Added Orderable Part Information table

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