

RL78/I1A

R01DS0171EJ0320

RENESAS MCU

Rev.3.20

Sep 29, 2017

True Low Power Platform, High Resolution PWM and Rich Analog, 2.7 V to 5.5 V operation, 32 to 64 Kbyte Flash, for Inverter Control, Digital Power Control and Lighting Control Applications

1. OUTLINE

1.1 Features

Ultra-Low Power Technology

- 2.7 V to 5.5 V operation from a single supply
- Stop (RAM retained): 0.23 μ A, (LVD enabled): 0.31 μ A
- Halt (RTC + LVD): 0.60 μ A
- Operating: 156.25 μ A/MHz

16-bit RL78 CPU Core

- Delivers 41 DMIPS at maximum operating frequency of 32 MHz
- <R> • Instruction execution: 86% of instructions can be executed in 1 to 2 clock cycles
- CISC architecture (Harvard) with 3-stage pipeline
- <R> • Multiply signed & unsigned: 16 x 16 to 32-bit result in 1 clock cycle
- MAC: 16 x 16 to 32-bit result in 2 clock cycles
- 16-bit barrel shifter for shift & rotate in 1 clock cycle
- 1-wire on-chip debug function

Main Flash Memory

- Density: 32 KB to 64 KB
- Block size: 1 KB
- On-chip single voltage flash memory with protection from block erase/writing
- Self-programming with secure boot swap function and flash shield window function

Data Flash Memory

- Data flash with background operation
- Data flash size: 4 KB
- Erase cycles: 1 million (typ.)
- Erase/programming voltage: 2.7 V to 5.5 V

RAM

- 2 KB to 4 KB size options
- Supports operands or instructions
- Back-up retention in all modes

High-speed On-chip Oscillator

- 32 MHz with +/- 1% accuracy over voltage (2.7 V to 5.5 V) and temperature (-20°C to 85°C)
- Pre-configured settings: 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz & 1 MHz

Reset and Supply Management

- Power-on reset (POR) monitor/generator
- Low voltage detection (LVD) with 6 setting options (Interrupt and/or reset function)

Data Memory Access (DMA) Controller

- Up to 2 fully programmable channels
- Transfer unit: 8- or 16-bit

16-bit timers KB0 to KB2, and KC0 for PWM output

16-bit timers KB0 to KB2: maximum 6 outputs (3 channels x 2)

- Smooth start function, dithering function, forced output stop function (unsynchronized with comparator or external interrupt) enables over-voltage protection, over-current protection and peak current control, and single/interleave PFC function
- Average resolution < 0.98 nsec output, 64 MHz (when using PLL) + dithering option

16-bit timer KC0 (1 channel x 6 (output))

- PWM output gating function by interlocking with 16-bit timers KB0, KB1, and KB2

Extended-Function Timers

- Multi-function 16-bit timers: Up to 8 channels
- Real-time clock (RTC): 1 channel (full calendar and alarm function with watch correction function)
- Interval timer: 12-bit, 1 channel
- 15 kHz watchdog timer: 1 channel (window function)

Multiple Communication Interfaces

- Up to 1 channel x I²C multi-master (SMBus/PMBus support)
- Up to 1 channel x CSI/SPI (7-, 8-bit)
- Up to 3 channels x UART (7-, 8-, 9-bit), DALI support 1 channel (8-, 16-, 17-, 24-bit, master and slave)
- Up to 1 channel x LIN

Rich Analog

- ADC: Up to 11 channels, 8/10-bit resolution, 2.125 μ s conversion time
- Supports 2.7 V
- Internal voltage reference (1.45 V)
- Comparator: High response time 70 ns (typ.), up to 6 channels, internal DAC 3 channels 8-bit resolution, window comparator mode
- PGA (x4 to x32): 6 input channels
- On-chip temperature sensor

Safety Features (IEC or UL 60730 compliance)

- Flash memory CRC calculation
- RAM parity error check
- RAM/SFR write protection
- Illegal memory access detection
- Clock stop/frequency detection
- ADC self-test

General Purpose I/O

- 5-V tolerant, high-current (up to 8.5 mA per pin)
- Open-drain, internal pull-up support

Operating Ambient Temperature

- Standard: -40°C to +105°C
- Extend: -40°C to +125°C

Package Type and Pin Count

SSOP: 20, 30, 38

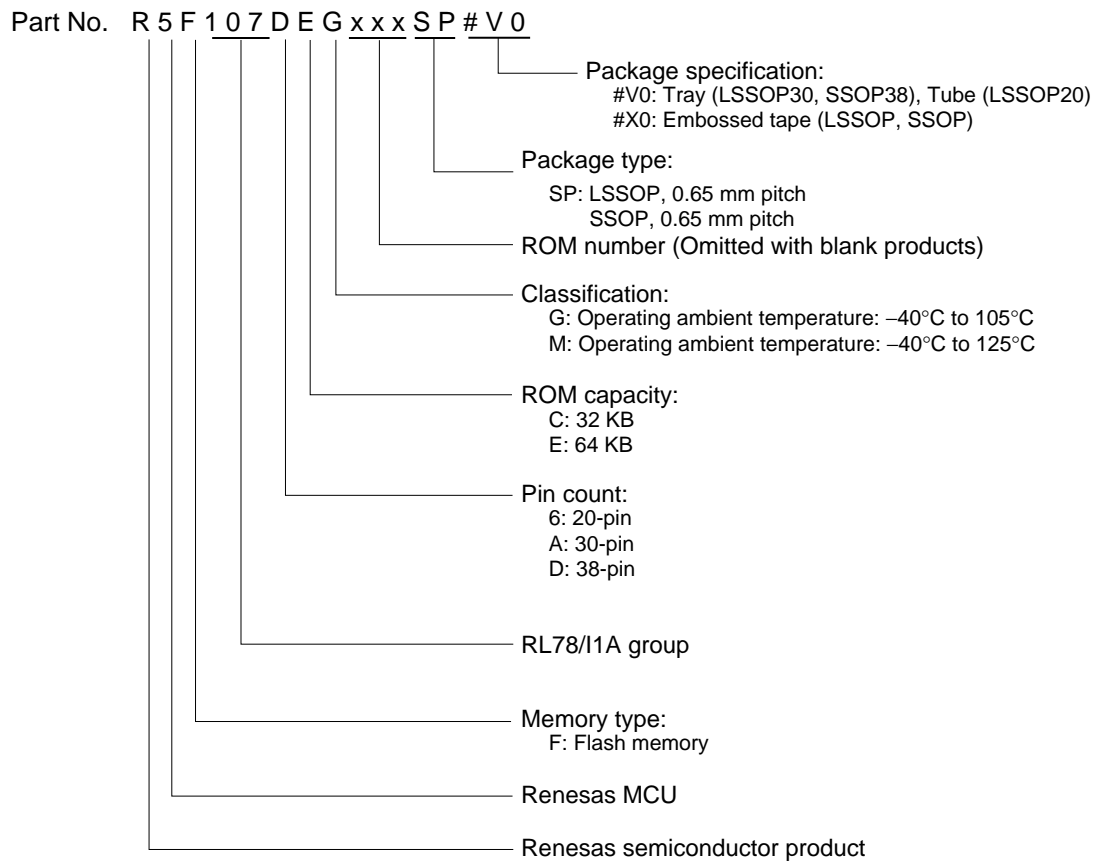
- ROM, RAM capacities

| Flash ROM | Data flash | RAM | RL78/I1A | | |
|-----------|------------|------------------|----------|----------|----------|
| | | | 20 pins | 30 pins | 38 pins |
| 64 KB | 4 KB | 4 KB Note | – | R5F107AE | R5F107DE |
| 32 KB | 4 KB | 2 KB | R5F1076C | R5F107AC | – |

Note This is about 3 KB when the self-programming function and data flash function are used.

1.2 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package of RL78/I1A



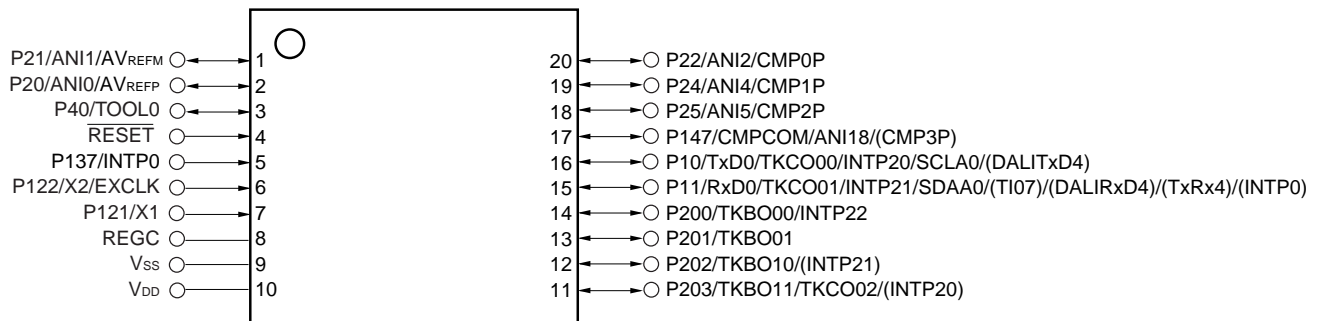
| Pin count | Package | Operating Ambient Temperature | Part Number |
|-----------|---|-------------------------------|---|
| 20 pins | 20-pin plastic LSSOP (4.4 × 6.5) | TA = -40 to +105°C | R5F1076CGSP#V0, R5F1076CGSP#X0 |
| | | TA = -40 to +125°C | R5F1076CMSP#V0, R5F1076CMSP#X0 |
| 30 pins | 30-pin plastic LSSOP (7.62 mm (300)) | TA = -40 to +105°C | R5F107ACGSP#V0, R5F107AEGSP#V0, R5F107ACGSP#X0, R5F107AEGSP#X0 |
| | | TA = -40 to +125°C | R5F107ACMSP#V0, R5F107AEMSP#V0, R5F107ACMSP#X0, R5F107AEMSP#X0 |
| 38 pins | 38-pin plastic SSOP (7.62 mm (300)) | TA = -40 to +105°C | R5F107DEGSP#V0, R5F107DEGSP#X0 |
| | | TA = -40 to +125°C | R5F107DEMSP#V0, R5F107DEMSP#X0 |

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Pin Configuration (Top View)

1.3.1 20-pin products

- 20-pin plastic LSSOP (4.4 x 6.5)

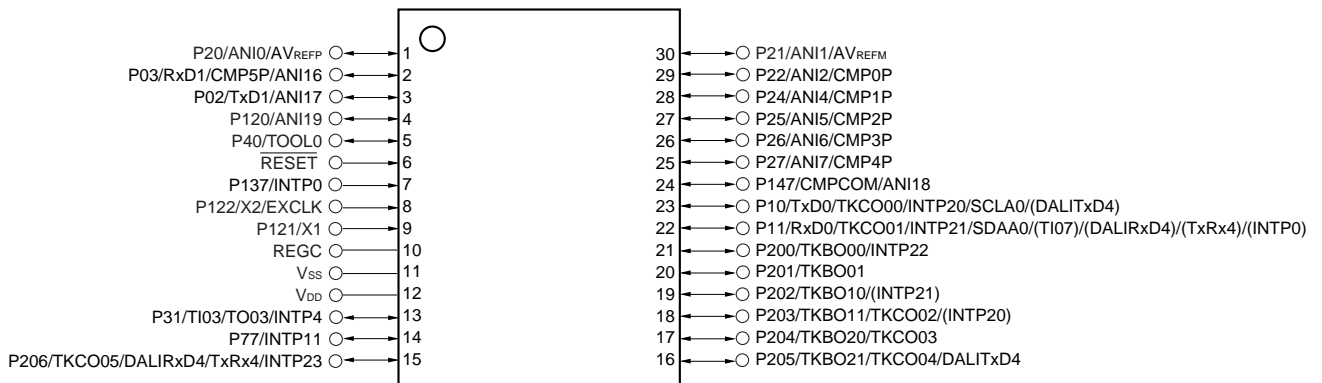


Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

- Remarks**
1. For pin identification, see **1.4 Pin Identification**.
 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR1) or the input switch control register (ISC). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR1)** and **Figure 15-20 Format of Input Switch Control Register (ISC) in the RL78/I1A User's Manual**.
 3. The shared function CMP3P can be assigned to P147 by setting the CMPSEL0 bit in the comparator input switch control register (CMPSEL).

1.3.2 30-pin products

- 30-pin plastic LSSOP (7.62 mm (300))

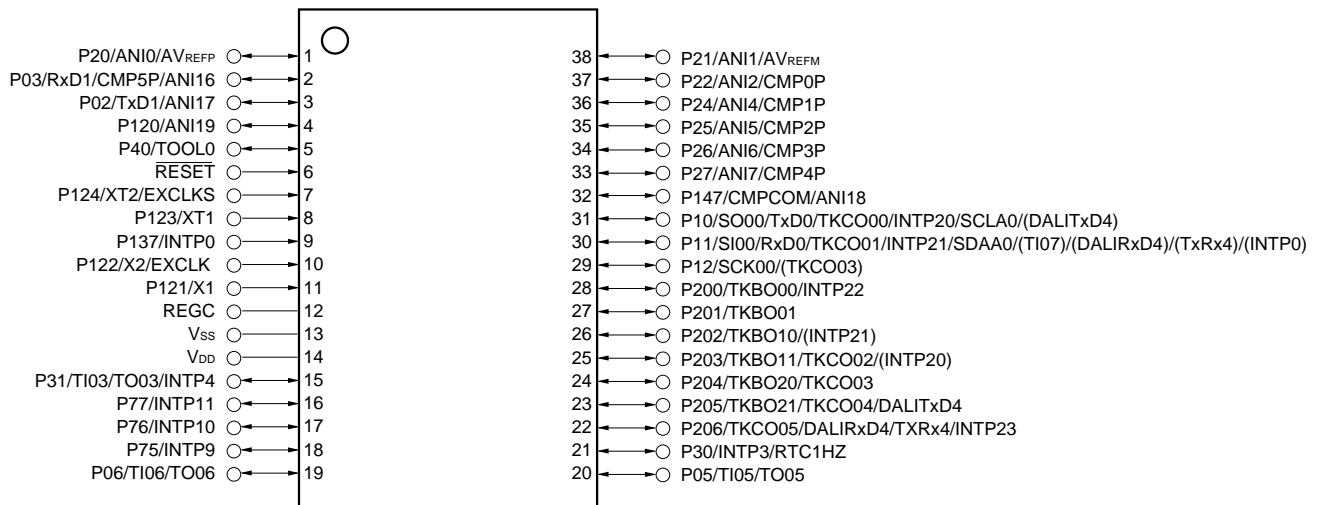


Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

- Remarks**
- For pin identification, see 1.4 Pin Identification.
 - Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR1) or the input switch control register (ISC). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR1)** and **Figure 15-20 Format of Input Switch Control Register (ISC)** in the RL78/I1A User's Manual.

1.3.3 38-pin products

- 38-pin plastic SSOP (7.62 mm (300))



Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

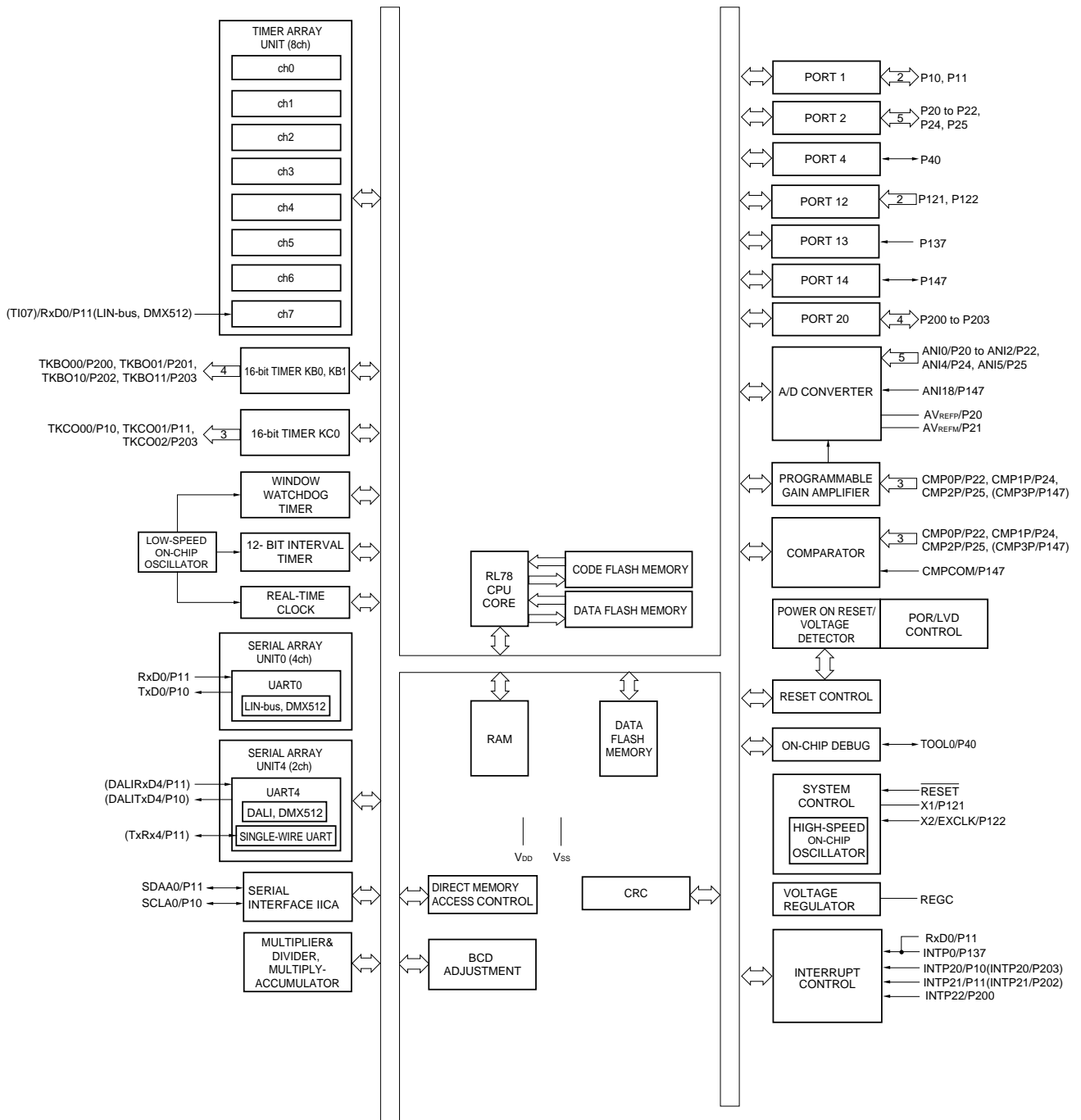
2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR1) or the input switch control register (ISC). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR1)** and **Figure 15-20 Format of Input Switch Control Register (ISC)** in the RL78/I1A User's Manual.

1.4 Pin Identification

| | | | |
|--|---|---|---|
| ANI0 to ANI2, ANI4 to ANI7, ANI16 to ANI19: | Analog Input | REGC: | Regulator Capacitance |
| AVREFM: | Analog Reference Voltage Minus | RESET: | Reset |
| AVREFP: | Analog Reference Voltage Plus | RTC1HZ: | Real-time Clock Correction Clock (1 Hz) Output |
| CMP0P to CMP5P: | Comparator Analog Input | RxD0, RxD1, DALIRxD4: | Receive Data |
| CMPCOM: | Comparator External Reference Voltage | SCK00: | Serial Clock Input/Output |
| EXCLK: | External Clock Input (Main System Clock) | SCLA0: | Serial Clock Input/Output |
| EXCLKS: | External Clock Input (Subsystem Clock) | SDAA0: | Serial Data Input/Output |
| INTP0, INTP3, INTP4, INTP9, INTP10, INTP11, INTP20 to INTP23: | Interrupt Request from Peripheral | SI00: | Serial Data Input |
| P02, P03, P05, P06: | Port 0 | SO00: | Serial Data Output |
| P10 to P12: | Port 1 | TI03, TI05, TI06, TI07: | Timer Input |
| P20 to P22, P24 to P27: | Port 2 | TO03, TO05, TO06, TKBO00, TKBO01 to TKBO20, TKBO21, | Timer Output |
| P30, P31: | Port 3 | TKCO00 to TKCO05: | Timer Output |
| P40: | Port 4 | TOOL0: | Data Input/Output for Tool |
| P75 to P77: | Port 7 | TxRx4: | Serial Data Input/Output for Single Wired UART |
| P120 to P124: | Port 12 | TxD0, TxD1 | |
| P137: | Port 13 | DALITxD4: | Transmit Data |
| P147: | Port 14 | V _{DD} : | Power Supply |
| P200 to P206: | Port 20 | V _{SS} : | Ground |
| | | X1, X2: | Crystal Oscillator (Main System Clock) |
| | | XT1, XT2: | Crystal Oscillator (Subsystem Clock) |

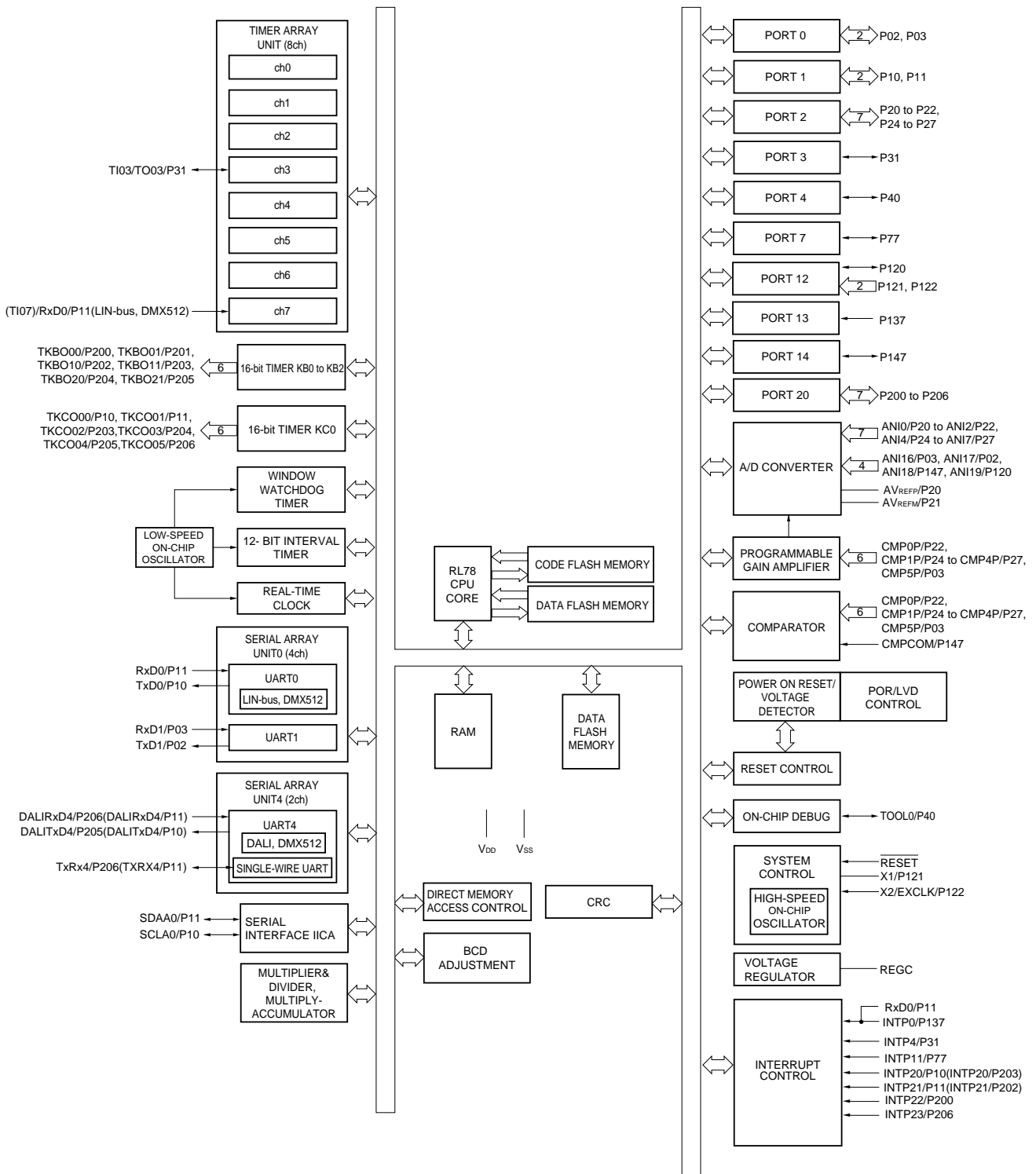
1.5 Block Diagram

1.5.1 20-pin products



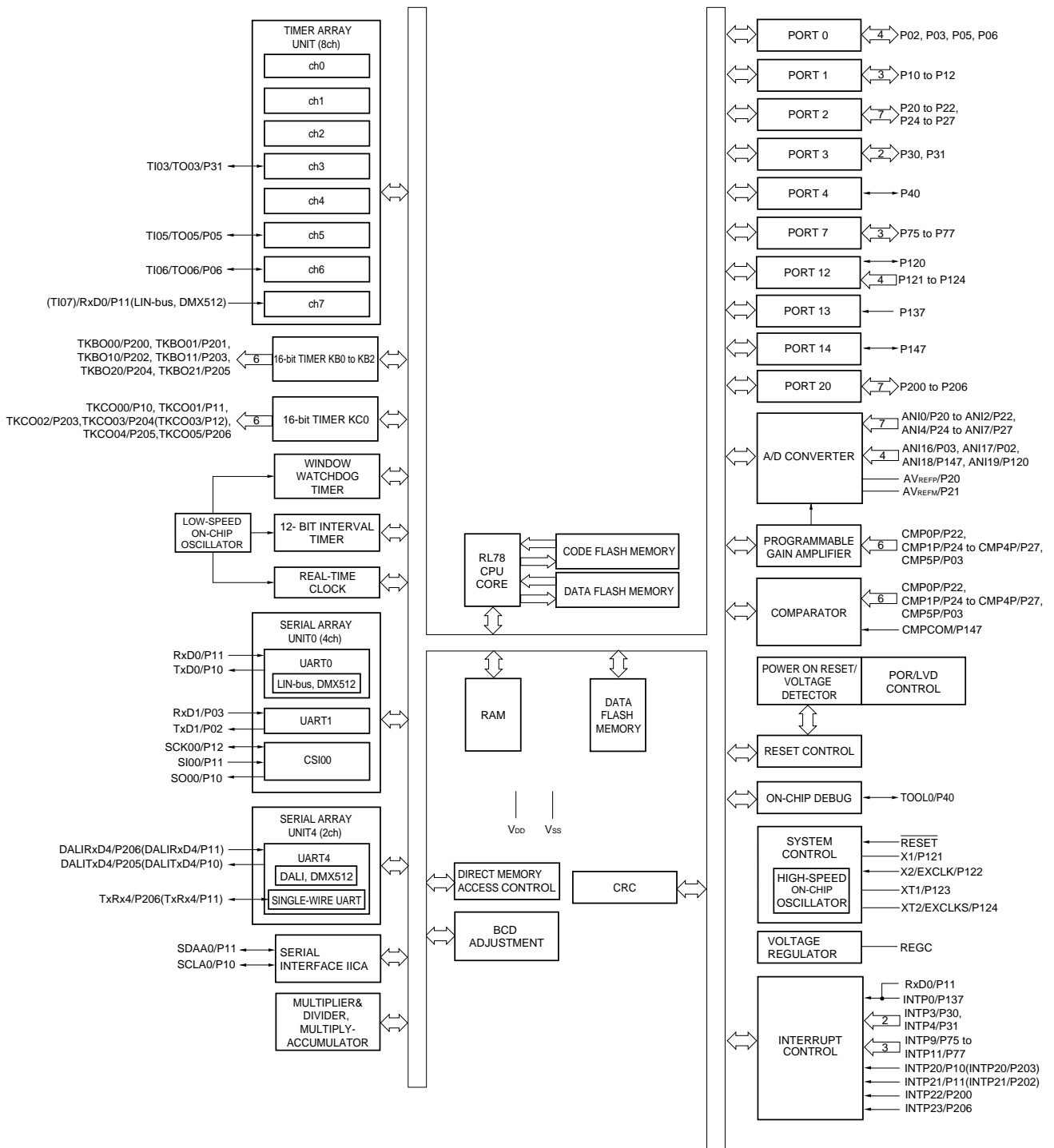
- Remarks 1.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR1) or the input switch control register (ISC). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR1)** and **Figure 15-20 Format of Input Switch Control Register (ISC)** in the RL78/I1A User's Manual.
- 2.** The shared function CMP3P can be assigned to P147 by setting the CMPSEL0 bit in the comparator input switch control register (CMPSEL).

1.5.2 30-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR1) or the input switch control register (ISC). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR1)** and **Figure 15-20 Format of Input Switch Control Register (ISC)** in the RL78/I1A User's Manual.

1.5.3 38-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR1) or the input switch control register (ISC). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR1)** and **Figure 15-20 Format of Input Switch Control Register (ISC)** in the RL78/I1A User's Manual.

1.6 Outline of Functions

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR1) is set to 00H.

(1/3)

| Item | | 20-pin | 30-pin | | 38-pin |
|---|-------------------------------|---|--|--|---------------------|
| | | R5F1076C | R5F107AC | R5F107AE | R5F107DE |
| Code flash memory (KB) | | 32 | 32 | 64 | 64 |
| Data flash memory (KB) | | 4 | 4 | 4 | 4 |
| RAM (KB) | | 2 | 2 | 4 ^{Note 1} | 4 ^{Note 1} |
| Address space | | 1 MB | | | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz ($V_{DD} = 2.7$ to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD} = 2.7$ to 5.5 V) | | | |
| | High-speed on-chip oscillator | HS (High-speed main) mode: 1 to 32 MHz ($V_{DD} = 2.7$ to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD} = 2.7$ to 5.5 V) | | | |
| Clock for 16-bit timers KB0 to KB2, and KC0 | | 64 MHz (TYP.) | | | |
| Subsystem clock (38-pin products only) | | XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz | | | |
| Low-speed on-chip oscillator | | 15 kHz (TYP.) | | | |
| General-purpose register | | (8-bit register × 8) × 4 banks | | | |
| Minimum instruction execution time | | 0.03125 μ s (High-speed on-chip oscillator: $f_{IH} = 32$ MHz operation) | | | |
| | | 0.05 μ s (High-speed system clock: $f_{MX} = 20$ MHz operation) | | | |
| | | 30.5 μ s (Subsystem clock: $f_{SUB} = 32.768$ kHz operation) (38-pin products only) | | | |
| Instruction set | | <ul style="list-style-type: none"> • 8-bit operation, 16-bit operation • Multiplication (8 bits × 8 bits) • Bit manipulation (Set, reset, test, and Boolean operation), etc. | | | |
| I/O port | Total | 16 | 26 | 34 | |
| | CMOS I/O | 13 | 23 | 29 | |
| | CMOS input | 3 | 3 | 5 | |
| | CMOS output | – | – | – | |
| Timer | 16-bit timer TAU | 8 channels (no timer output) | 8 channels (timer output: 1, PWM output: 1 ^{Note 2}) | 8 channels (timer outputs: 3, PWM outputs: 3 ^{Note 2}) | |
| | 16-bit timer KB | 2 channels (PWM outputs: 4) | 3 channels (PWM outputs: 6) | | |
| | 16-bit timer KC | 1 channel (PWM outputs: 3) | 1 channel (PWM outputs: 6) | | |

Notes 1. This is about 3 KB when the self-programming function and data flash function are used. (For details, see **CHAPTER 3 in the RL78/I1A User's Manual.**)

2. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function in the RL78/I1A User's Manual.**)

(2/3)

| Item | | 20-pin | 30-pin | 38-pin |
|---|----------------------------|---|--------------------|---|
| | | R5F1076C | R5F107AC, R5F107AE | R5F107DE |
| Timer | Watchdog timer | 1 channel | | |
| | Real-time clock (RTC) | 1 channel ^{Notes 1, 2} | | |
| | 12-bit interval timer (IT) | 1 channel | | |
| | RTC output | - | | 1 1 Hz (subsystem clock: f _{SUB} = 32.768 kHz) |
| 8/10-bit resolution A/D converter | | 6 channels | 11 channels | 11 channels |
| Comparator | | 4 channels | 6 channels | 6 channels |
| Programmable gain amplifier | | 1 channel | | |
| | Input ^{Note 3} | 4 channels | 6 channels | 6 channels |
| Serial interface | | <p>[20-pin] ^{Note 5}</p> <ul style="list-style-type: none"> • UART (Supporting LIN-bus and DMX512): 1 channel • UART (Supporting DALI communication): 1 channel <p>[30-pin products]</p> <ul style="list-style-type: none"> • UART (Supporting LIN-bus and DMX512): 1 channel • UART: 1 channel • UART (Supporting DALI communication): 1 channel <p>[38-pin products]</p> <ul style="list-style-type: none"> • CSI: 1 channel/UART (Supporting LIN-bus and DMX512): 1 channel • UART: 1 channel • UART (Supporting DALI communication): 1 channel | | |
| | I ² C bus | 1 channel | 1 channel | 1 channel |
| Multiplier and divider/multiply-accumulator | | <ul style="list-style-type: none"> • 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed) | | |
| DMA controller | | 2 channels | | |
| Vectored interrupt sources | Internal | 27 | 30 | 30 |
| | External | 7 | 10 | 11 |
| Reset | | <ul style="list-style-type: none"> • Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution^{Note 4} • Internal reset by RAM parity error • Internal reset by illegal-memory access | | |

- Notes**
1. The subsystem clock (f_{SUB}) can be selected as the operating clock only for 38-pin products.
 2. The 20- and 30-pin products can only be used as the constant-period interrupt function.
 3. The comparator input is alternatively used with analog input pin (ANI pin).
 4. The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.
 5. The 20 pin products can only be used 1 UART simultaneously due to sharing of the same I/O pins.

(3/3)

| Item | 20-pin | 30-pin | 38-pin |
|-------------------------------|---|--------------------|----------|
| | R5F1076C | R5F107AC, R5F107AE | R5F107DE |
| Power-on-reset circuit | <ul style="list-style-type: none"> • Power-on-reset: 1.51 V (TYP.) • Power-down-reset: 1.50 V (TYP.) | | |
| Voltage detector | <ul style="list-style-type: none"> • Rising edge: 2.81 V to 4.06 V (6 stages) • Falling edge: 2.75 V to 3.98 V (6 stages) | | |
| On-chip debug function | Provided | | |
| Power supply voltage | $V_{DD} = 2.7$ to 5.5 V | | |
| Operating ambient temperature | $T_A = -40$ to $+105^\circ\text{C}$ (G: Industrial applications), $T_A = -40$ to $+125^\circ\text{C}$ (M: Industrial applications) | | |

2. ELECTRICAL SPECIFICATIONS

(G: Industrial applications, $T_A = -40$ to $+105^\circ\text{C}$)

In this chapter, shows the electrical specifications of the target products.

Target products (G: Industrial applications): $T_A = -40$ to $+105^\circ\text{C}$
R5F107xxGxx

Cautions 1. The RL78/I1A has an on-chip debug function, which is provided for development and evaluation.

Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted depend on the product. See 2.1 Port Function to 2.2.1 Functions for each product in the RL78/I1A User's Manual.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$) (1/2)

| Parameter | Symbols | Conditions | Ratings | Unit |
|------------------------|-------------|--|--|------|
| Supply voltage | V_{DD} | | -0.5 to +6.5 | V |
| REGC pin input voltage | V_{IREGC} | REGC | -0.3 to +2.8 and -0.3 to $V_{DD} + 0.3$ ^{Note 1} | V |
| Input voltage | V_{I1} | P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120 to P124, P137, P147, P200 to P206, EXCLK, EXCLKS, RESET | -0.3 to $V_{DD} + 0.3$ ^{Note 2} | V |
| Output voltage | V_{O1} | P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120, P147, P200 to P206 | -0.3 to $V_{DD} + 0.3$ ^{Note 2} | V |
| Analog input voltage | V_{AI1} | ANI0 to ANI2, ANI4 to ANI7, ANI16 to ANI19 | -0.3 to $V_{DD} + 0.3$ and -0.3 to $AV_{REF(+)}$ $+ 0.3$ ^{Notes 2, 3} | V |

- Notes**
1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.
 2. Must be 6.5 V or lower.
 3. Do not exceed $AV_{REF(+)} + 0.3$ V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

- Remarks**
1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
 2. $AV_{REF(+)}$: + side reference voltage of the A/D converter.
 3. V_{SS} : Reference voltage

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$) (2/2)

| Parameter | Symbols | Conditions | | Ratings | Unit |
|-------------------------------|----------------------------------|------------------------------|---|---|-------------|
| Output current, high | I _{OH1} | Per pin | P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206 | -40 | mA |
| | | Total of all pins -170 mA | P02, P03, P40, P120 | -70 | mA |
| | | | P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206 | -100 | mA |
| | I _{OH2} | Per pin | P20 to P22, P24 to P27 | -0.5 | mA |
| | | Total of all pins | | -2 | mA |
| | Output current, low | I _{OL1} | Per pin | P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206 | 40 |
| Total of all pins 170 mA | | | P02, P03, P40, P120 | 70 | mA |
| | | | P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206 | 100 | mA |
| I _{OL2} | | Per pin | P20 to P22, P24 to P27 | 1 | mA |
| | | Total of all pins | | 5 | mA |
| Operating ambient temperature | | T _A | In normal operation mode | | -40 to +105 |
| | In flash memory programming mode | | | | |
| Storage temperature | T _{stg} | | | -65 to +150 | °C |

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.2 Oscillator Characteristics

2.2.1 X1, XT1 oscillator characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Parameter | Resonator | Conditions | MIN. | TYP. | MAX. | Unit |
|--|-------------------------------------|------------|------|--------|------|------|
| X1 clock oscillation frequency (f_X) ^{Note} | Ceramic resonator/crystal resonator | | 1.0 | | 20.0 | MHz |
| XT1 clock oscillation frequency (f_{XT}) ^{Note} | Crystal resonator | | 32 | 32.768 | 35 | kHz |

Note Indicates only permissible oscillator frequency ranges. See **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, see **5.4 System Clock Oscillator** in the **RL78/I1A User's Manual**.

2.2.2 On-chip oscillator characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Oscillators | Parameters | Conditions | MIN. | TYP. | MAX. | Unit |
|--|------------|------------------------------------|------|------|------|------|
| High-speed on-chip oscillator clock frequency ^{Note 1} | f_{IH} | | 1 | | 32 | MHz |
| High-speed on-chip oscillator clock frequency accuracy ^{Note 2} | | $T_A = -20$ to 85°C | -1 | | +1 | % |
| | | $T_A = -40$ to 105°C | -1.5 | | +1.5 | % |
| Low-speed on-chip oscillator clock frequency | f_{IL} | | | 15 | | kHz |
| Low-speed on-chip oscillator clock frequency accuracy | | | -15 | | +15 | % |

Notes 1. Frequency can be selected in a high-speed on-chip oscillator. Selected by bits 0 to 3 of option byte (000C2H/010C2H).

2. This indicates the oscillator characteristics only. See **AC Characteristics** for instruction execution time.

2.2.3 PLL characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|-------------|---|-----------------------|------|------|------|
| PLL input clock frequency ^{Note} | f_{PLLIN} | High-speed system clock is selected ($f_{MX} = 4\text{ MHz}$) | 3.94 | 4.00 | 4.06 | MHz |
| | | High-speed on-chip oscillator clock is selected ($f_{IH} = 4\text{ MHz}$) | 3.94 | 4.00 | 4.06 | MHz |
| PLL output clock frequency ^{Note} | f_{PLL} | | $f_{PLLIN} \times 16$ | | | MHz |

Note This only indicates the oscillator characteristics. See **AC Characteristics** for instruction execution time.

2.3 DC Characteristics

2.3.1 Pin characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|--|--|--|---|------|-------|------------------------|----|
| Output current, high ^{Note 1} | I _{OH1} | Per pin for P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206 | 4.0 V \leq V _{DD} \leq 5.5 V | | | -3.0 ^{Note 2} | mA |
| | | | 2.7 V \leq V _{DD} < 4.0 V | | | -1.0 | mA |
| | | Total of P02, P03, P40, P120 (When duty \leq 70% ^{Note 3}) | 4.0 V \leq V _{DD} \leq 5.5 V | | | -12.0 | mA |
| | | | 2.7 V \leq V _{DD} < 4.0 V | | | -4.0 | mA |
| | | Total of P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206 (When duty \leq 70% ^{Note 3}) | 4.0 V \leq V _{DD} \leq 5.5 V | | | -30.0 | mA |
| | | | 2.7 V \leq V _{DD} < 4.0 V | | | -10.0 | mA |
| | Total of all pins (When duty \leq 70% ^{Note 3}) | 4.0 V \leq V _{DD} \leq 5.5 V | | | -30.0 | mA | |
| | | 2.7 V \leq V _{DD} < 4.0 V | | | -14.0 | mA | |
| | I _{OH2} | Per pin for P20 to P22, P24 to P27 | 2.7 V \leq V _{DD} \leq 5.5 V | | | -0.1 ^{Note 2} | mA |
| | | | 2.7 V \leq V _{DD} \leq 5.5 V | | | -0.7 | mA |

- Notes**
- Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.
 - However, do not exceed the total current value.
 - Specification under conditions where the duty factor \leq 70%.
The output current value that has changed to the duty factor $>$ 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
 - Total output current of pins = $(I_{OH} \times 0.7)/(n \times 0.01)$
<Example> Where $n = 80\%$ and $I_{OH} = -10.0\text{ mA}$
Total output current of pins = $(-10.0 \times 0.7)/(80 \times 0.01) \cong -8.7\text{ mA}$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P02, P10 to P12 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|--|--|------|-----------------------|------|
| Output current, I_{OL} ^{Note 1} | I _{OL1} | Per pin for P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206 | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | 8.5 ^{Note 2} | mA |
| | | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ | | 1.5 ^{Note 2} | mA |
| | | Total of P02, P03, P40, P120 (When duty $\leq 70\%$ ^{Note 3}) | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | 40.0 | mA |
| | | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ | | 7.5 | mA |
| | | Total of P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206 (When duty $\leq 70\%$ ^{Note 3}) | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | 40.0 | mA |
| | | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ | | 17.5 | mA |
| | Total of all pins (When duty $\leq 70\%$ ^{Note 3}) | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | 80.0 | mA | |
| | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ | | 25.0 | mA | |
| | I _{OL2} | Per pin for P20 to P22, P24 to P27 | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | 0.4 ^{Note 2} | mA |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | 2.8 | mA |
| | | Total of all pins (When duty $\leq 70\%$ ^{Note 3}) | | | | |

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor $\leq 70\%$.

The output current value that has changed to the duty factor $> 70\%$ the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = $(I_{OL} \times 0.7)/(n \times 0.01)$

<Example> Where $n = 80\%$ and $I_{OL} = -10.0\text{ mA}$

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(80 \times 0.01) \cong -8.7\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|---------------------|-----------|---|--|-------------|------|-------------|---|
| Input voltage, high | V_{IH1} | P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120 to P124, P137, P147, P200 to P206, EXCLK, EXCLKS, RESET | Normal input buffer | $0.8V_{DD}$ | | V_{DD} | V |
| | V_{IH2} | P03, P10, P11 | TTL input buffer $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.1 | | V_{DD} | V |
| | | | TTL input buffer $3.3\text{ V} \leq V_{DD} < 4.0\text{ V}$ | 2.0 | | V_{DD} | V |
| | | | TTL input buffer $2.7\text{ V} \leq V_{DD} < 3.3\text{ V}$ | 1.5 | | V_{DD} | V |
| Input voltage, low | V_{IL1} | P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120 to P124, P137, P147, P200 to P206, EXCLK, EXCLKS, RESET | Normal input buffer | 0 | | $0.2V_{DD}$ | V |
| | V_{IL2} | P03, P10, P11 | TTL input buffer $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 0 | | 0.8 | V |
| | | | TTL input buffer $3.3\text{ V} \leq V_{DD} < 4.0\text{ V}$ | 0 | | 0.5 | V |
| | | | TTL input buffer $2.7\text{ V} \leq V_{DD} < 3.3\text{ V}$ | 0 | | 0.32 | V |

Caution The maximum value of V_{IH} of pins P02, P10 to P12 is V_{DD} , even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|----------------------|------------------|---|---|----------------|------|------|
| Output voltage, high | V _{OH1} | P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206 | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -3.0\text{ mA}$ | | | V |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -1.0\text{ mA}$ | $V_{DD} - 0.7$ | | V |
| | V _{OH2} | P20 to P22, P24 to P27 | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH2} = -100\ \mu\text{A}$ | $V_{DD} - 0.5$ | | V |
| Output voltage, low | V _{OL1} | P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206 | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 8.5\text{ mA}$ | | 0.7 | V |
| | | | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 4.0\text{ mA}$ | | 0.4 | V |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 1.5\text{ mA}$ | | 0.4 | V |
| | V _{OL2} | P20 to P22, P24 to P27 | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL2} = 400\ \mu\text{A}$ | | 0.4 | V |

Caution P02, P10 to P12 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | | |
|-----------------------------|------------|--|--------------------------------|---------------------------------------|------|------|------------------|---------------|
| Input leakage current, high | I_{LIH1} | P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120, P137, P147, P200 to P206, RESET | $V_i = V_{DD}$ | | | 1 | μA | |
| | I_{LIH2} | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS) | $V_i = V_{DD}$ | In input port or external clock input | | | 1 | μA |
| | | | | In resonator connection | | | 10 | μA |
| Input leakage current, low | I_{LIL1} | P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120, P137, P147, P200 to P206, RESET | $V_i = V_{SS}$ | | | -1 | μA | |
| | I_{LIL2} | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS) | $V_i = V_{SS}$ | In input port or external clock input | | | -1 | μA |
| | | | | In resonator connection | | | -10 | μA |
| On-chip pull-up resistance | R_U | P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206 | $V_i = V_{SS}$, In input port | 10 | 20 | 100 | $\text{k}\Omega$ | |

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

 $(T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$) (1/2)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit | | | |
|---|----------------------|---|--|---|---|----------------------|---------------|---------------|---------------|----|
| Supply current Note 1 | I _{DD1} | Operating mode | HS (high-speed main) mode ^{Note 5} | $f_{IH} = 32\text{ MHz}$ ^{Note 3} | $V_{DD} = 5.0\text{ V}$ | | 5.0 | 7.5 | mA | |
| | | | | | $V_{DD} = 3.0\text{ V}$ | | 5.0 | 7.5 | mA | |
| | | | | $f_{IH} = 24\text{ MHz}$ ^{Note 3} | $V_{DD} = 5.0\text{ V}$ | | 3.9 | 5.8 | mA | |
| | | | | | $V_{DD} = 3.0\text{ V}$ | | 3.9 | 5.8 | mA | |
| | | | | $f_{IH} = 16\text{ MHz}$ ^{Note 3} | $V_{DD} = 5.0\text{ V}$ | | 2.9 | 4.2 | mA | |
| | | | | | $V_{DD} = 3.0\text{ V}$ | | 2.9 | 4.2 | mA | |
| | | | LS (low-speed main) mode ^{Note 5} | $f_{IH} = 8\text{ MHz}$ ^{Note 3} , $T_A = -40$ to $+85^\circ\text{C}$ | $V_{DD} = 3.0\text{ V}$ | | 1.3 | 2.0 | mA | |
| | | | HS (high-speed main) mode ^{Note 5} | $f_{MX} = 20\text{ MHz}$ ^{Note 2} , $V_{DD} = 5.0\text{ V}$ | Square wave input | | 3.2 | 4.9 | mA | |
| | | | | | Resonator connection | | 3.3 | 5.0 | mA | |
| | | | | | $f_{MX} = 20\text{ MHz}$ ^{Note 2} , $V_{DD} = 3.0\text{ V}$ | Square wave input | | 3.2 | 4.9 | mA |
| | | | | | | Resonator connection | | 3.3 | 5.0 | mA |
| | | | | $f_{MX} = 10\text{ MHz}$ ^{Note 2} , $V_{DD} = 5.0\text{ V}$ | Square wave input | | 2.0 | 2.9 | mA | |
| | | Resonator connection | | | | 2.0 | 2.9 | mA | | |
| | | $f_{MX} = 10\text{ MHz}$ ^{Note 2} , $V_{DD} = 3.0\text{ V}$ | | | Square wave input | | 2.0 | 2.9 | mA | |
| | | | | | Resonator connection | | 2.0 | 2.9 | mA | |
| | | LS (low-speed main) mode ^{Note 5} | $f_{MX} = 8\text{ MHz}$ ^{Note 2} , $V_{DD} = 3.0\text{ V}$, $T_A = -40$ to $+85^\circ\text{C}$ | Square wave input | | 1.2 | 1.8 | mA | | |
| | | | | Resonator connection | | 1.2 | 1.8 | mA | | |
| | | HS (high-speed main) mode ^{Note 5} | $f_{IH} = 4\text{ MHz}$ ^{Note 3} $f_{PLL} = 64\text{ MHz}$, $f_{CLK} = 32\text{ MHz}$ | $V_{DD} = 5.0\text{ V}$ | | 5.4 | 8.5 | mA | | |
| | | | | $V_{DD} = 3.0\text{ V}$ | | 5.4 | 8.5 | mA | | |
| | | | $f_{IH} = 4\text{ MHz}$ ^{Note 3} $f_{PLL} = 64\text{ MHz}$, $f_{CLK} = 16\text{ MHz}$ | $V_{DD} = 5.0\text{ V}$ | | 3.3 | 5.7 | mA | | |
| | | | | $V_{DD} = 3.0\text{ V}$ | | 3.3 | 5.7 | mA | | |
| | | Subsystem clock operation | $f_{SUB} = 32.768\text{ kHz}$ ^{Note 4} $T_A = -40^\circ\text{C}$ | Square wave input | | 4.2 | 6.0 | μA | | |
| | | | | Resonator connection | | 4.4 | 6.2 | μA | | |
| | | | | $f_{SUB} = 32.768\text{ kHz}$ ^{Note 4} $T_A = +25^\circ\text{C}$ | Square wave input | | 4.2 | 6.0 | μA | |
| Resonator connection | | | | | 4.4 | 6.2 | μA | | | |
| $f_{SUB} = 32.768\text{ kHz}$ ^{Note 4} $T_A = +50^\circ\text{C}$ | Square wave input | | | | 4.3 | 7.2 | μA | | | |
| | Resonator connection | | | | 4.5 | 7.4 | μA | | | |
| $f_{SUB} = 32.768\text{ kHz}$ ^{Note 4} $T_A = +70^\circ\text{C}$ | Square wave input | | | 4.4 | 8.1 | μA | | | | |
| | Resonator connection | | | 4.6 | 8.3 | μA | | | | |
| $f_{SUB} = 32.768\text{ kHz}$ ^{Note 4} $T_A = +85^\circ\text{C}$ | Square wave input | | | 5.2 | 11.4 | μA | | | | |
| | Resonator connection | | | 5.4 | 11.6 | μA | | | | |
| $f_{SUB} = 32.768\text{ kHz}$ ^{Note 4} $T_A = +105^\circ\text{C}$ | Square wave input | | | 6.9 | 20.8 | μA | | | | |
| | Resonator connection | | | 7.1 | 21.0 | μA | | | | |

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, comparator, programmable gain amplifier, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
LS (low-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }8\text{ MHz}$

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$) (2/2)

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|--|----------------------|----------------------------------|--|---|-------------------------|---------------|------|---------------|---------------|
| Supply current Note 1 | I_{DD2} Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{IH} = 32\text{ MHz}$ Note 4 | $V_{DD} = 5.0\text{ V}$ | | 0.72 | 2.9 | mA |
| | | | | | $V_{DD} = 3.0\text{ V}$ | | 0.72 | 2.9 | mA |
| | | | | $f_{IH} = 24\text{ MHz}$ Note 4 | $V_{DD} = 5.0\text{ V}$ | | 0.57 | 2.3 | mA |
| | | | | | $V_{DD} = 3.0\text{ V}$ | | 0.57 | 2.3 | mA |
| | | | | $f_{IH} = 16\text{ MHz}$ Note 4 | $V_{DD} = 5.0\text{ V}$ | | 0.50 | 1.7 | mA |
| | | | | | $V_{DD} = 3.0\text{ V}$ | | 0.50 | 1.7 | mA |
| | | | LS (low-speed main) mode Note 7 | $f_{IH} = 8\text{ MHz}$ Note 4, $T_A = -40$ to $+85^\circ\text{C}$ | $V_{DD} = 3.0\text{ V}$ | | 320 | 910 | μA |
| | | | HS (high-speed main) mode Note 7 | $f_{MX} = 20\text{ MHz}$ Note 3, $V_{DD} = 5.0\text{ V}$ | Square wave input | | 0.40 | 1.9 | mA |
| | | | | | Resonator connection | | 0.50 | 2.0 | mA |
| | | | | $f_{MX} = 20\text{ MHz}$ Note 3, $V_{DD} = 3.0\text{ V}$ | Square wave input | | 0.40 | 1.9 | mA |
| | | | | | Resonator connection | | 0.50 | 2.0 | mA |
| | | | | $f_{MX} = 10\text{ MHz}$ Note 3, $V_{DD} = 5.0\text{ V}$ | Square wave input | | 0.24 | 1.02 | mA |
| | | | | | Resonator connection | | 0.30 | 1.08 | mA |
| | | | | $f_{MX} = 10\text{ MHz}$ Note 3, $V_{DD} = 3.0\text{ V}$ | Square wave input | | 0.24 | 1.02 | mA |
| | | Resonator connection | | | | 0.30 | 1.08 | mA | |
| | | LS (low-speed main) mode Note 7 | $f_{MX} = 8\text{ MHz}$ Note 3, $V_{DD} = 3.0\text{ V}$, $T_A = -40$ to $+85^\circ\text{C}$ | Square wave input | | 130 | 720 | μA | |
| | | | | Resonator connection | | 170 | 760 | μA | |
| | | HS (high-speed main) mode Note 7 | $f_{IH} = 4\text{ MHz}$ Note 4 $f_{PLL} = 64\text{ MHz}$, $f_{CLK} = 32\text{ MHz}$ | $V_{DD} = 5.0\text{ V}$ | | 1.15 | 4.0 | mA | |
| | | | | $V_{DD} = 3.0\text{ V}$ | | 1.15 | 4.0 | mA | |
| | | | $f_{IH} = 4\text{ MHz}$ Note 4 $f_{PLL} = 64\text{ MHz}$, $f_{CLK} = 16\text{ MHz}$ | $V_{DD} = 5.0\text{ V}$ | | 0.95 | 3.2 | mA | |
| | | | | $V_{DD} = 3.0\text{ V}$ | | 0.95 | 3.2 | mA | |
| | | Subsystem clock operation | $f_{SUB} = 32.768\text{ kHz}$ Note 5 $T_A = -40^\circ\text{C}$ | Square wave input | | 0.28 | 0.70 | μA | |
| | | | | Resonator connection | | 0.47 | 0.89 | μA | |
| | | | $f_{SUB} = 32.768\text{ kHz}$ Note 5 $T_A = +25^\circ\text{C}$ | Square wave input | | 0.33 | 0.70 | μA | |
| | | | | Resonator connection | | 0.52 | 0.89 | μA | |
| | | | $f_{SUB} = 32.768\text{ kHz}$ Note 5 $T_A = +50^\circ\text{C}$ | Square wave input | | 0.41 | 1.90 | μA | |
| | | | | Resonator connection | | 0.60 | 2.09 | μA | |
| | | | $f_{SUB} = 32.768\text{ kHz}$ Note 5 $T_A = +70^\circ\text{C}$ | Square wave input | | 0.54 | 2.80 | μA | |
| Resonator connection | | | | 0.73 | 2.99 | μA | | | |
| $f_{SUB} = 32.768\text{ kHz}$ Note 5 $T_A = +85^\circ\text{C}$ | Square wave input | | | 1.27 | 6.10 | μA | | | |
| | Resonator connection | | | 1.46 | 6.29 | μA | | | |
| $f_{SUB} = 32.768\text{ kHz}$ Note 5 $T_A = +105^\circ\text{C}$ | Square wave input | | 3.04 | 15.5 | μA | | | | |
| | Resonator connection | | 3.23 | 15.7 | μA | | | | |
| I_{DD3} Note 6 | STOP mode Note 8 | $T_A = -40^\circ\text{C}$ | | | | | 0.18 | 0.50 | μA |
| | | $T_A = +25^\circ\text{C}$ | | | | | 0.23 | 0.50 | μA |
| | | $T_A = +50^\circ\text{C}$ | | | | | 0.27 | 1.70 | μA |
| | | $T_A = +70^\circ\text{C}$ | | | | | 0.44 | 2.60 | μA |
| | | $T_A = +85^\circ\text{C}$ | | | | | 1.17 | 5.90 | μA |
| | | $T_A = +105^\circ\text{C}$ | | | | | 2.94 | 15.3 | μA |

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, comparator, programmable gain amplifier, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When $RTCLPC = 1$ and setting ultra-low current consumption ($AMPHS1 = 1$). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
LS (low-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }8\text{ MHz}$
 8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---------------------------------|--|---|------|------|------|---------------|
| Low-speed on-chip oscillator operating current | I_{FIL} ^{Note 1} | | | | 0.20 | | μA |
| RTC operating current | I_{RTC} Notes 1, 2, 3 | | | | 0.02 | | μA |
| 12-bit interval timer operating current | I_{IT} Notes 1, 2, 4 | | | | 0.02 | | μA |
| Watchdog timer operating current | I_{WDT} Notes 1, 2, 5 | $f_{IL} = 15\text{ kHz}$ | | | 0.22 | | μA |
| A/D converter operating current | I_{ADC} Notes 1, 6 | When conversion at maximum speed | Normal mode, $AV_{REFP} = V_{DD} = 5.0\text{ V}$ | | 1.3 | 1.7 | mA |
| | | | Low voltage mode, $AV_{REFP} = V_{DD} = 3.0\text{ V}$ | | 0.5 | 0.7 | mA |
| A/D converter reference voltage current | I_{ADREF} ^{Note 1} | | | | 75.0 | | μA |
| Temperature sensor operating current | I_{TMPS} ^{Note 1} | | | | 75.0 | | μA |
| LVD operating current | I_{LVD} ^{Notes 1, 7} | | | | 0.08 | | μA |
| Self-programming operating current | I_{FSP} ^{Notes 1, 8} | | | | 2.50 | 12.2 | mA |
| Programmable gain amplifier operating current | I_{PGA} ^{Note 9} | | | | 0.21 | 0.31 | mA |
| | | | | | 0.18 | 0.29 | mA |
| Comparator operating current | I_{CMP} ^{Note 10} | When one comparator channel is operating | $AV_{REFP} = V_{DD} = 5.0\text{ V}$ | | 41.4 | 62 | μA |
| | | | $AV_{REFP} = V_{DD} = 3.0\text{ V}$ | | 37.2 | 59 | μA |
| | I_{VREF} | When one internal reference voltage circuit is operating | $AV_{REFP} = V_{DD} = 5.0\text{ V}$ | | 14.8 | 26 | μA |
| | | | $AV_{REFP} = V_{DD} = 3.0\text{ V}$ | | 8.9 | 20 | μA |
| Programmable gain amplifier/comparator reference current source | I_{IREF} ^{Note 11} | | | | 3.2 | 5.1 | μA |
| | | | | | 2.9 | 4.9 | μA |
| BGO operating current | I_{BGO} ^{Note 12} | | | | 2.50 | 12.2 | mA |
| SNOOZE operating current | I_{SNOZ} ^{Note 1} | ADC operation | The mode is performed ^{Note 13} | | 0.50 | 1.1 | mA |
| | | | The A/D conversion operations are performed, Standard mode, $AV_{REFP} = V_{DD} = 5.0\text{ V}$ | | 2.0 | 3.04 | mA |
| | | CSI/UART operation | | | 0.70 | 1.54 | mA |

(Notes and Remarks are listed on the next page.)

- Notes**
1. Current flowing to the V_{DD} .
 2. When the high-speed on-chip oscillator and high-speed system clock are stopped.
 3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2} , and I_{RTC} , when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.
 4. Current flowing only to the 12-bit interval timer (excluding the operating current of the XT1 oscillator and f_{IL} operating current). The current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2} , and I_{IT} , when the 12-bit interval timer operates in operation mode or HALT mode.
 5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer is in operation.
 6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.
 7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.
 8. Current flowing during self-programming operation.
 9. Current flowing only to the programmable gain amplifier. The supply current value of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} , and I_{PGA} , when the programmable gain amplifier is operating in operating mode or in HALT mode.
 10. Current flowing only to the comparator. The supply current value of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} , and I_{CMP} , when the comparator is operating.
 11. This is the current required to flow to V_{DD} pin of the current circuit that is used as the programmable gain amplifier and the comparator.
 12. Current flowing only during data flash rewrite.
 13. See **21.3.3 SNOOZE mode in the RL78/I1A User's Manual** for shift time to the SNOOZE mode .

- Remarks**
1. f_{IL} : Low-speed on-chip oscillator clock frequency
 2. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 3. f_{CLK} : CPU/peripheral hardware clock frequency
 4. Temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$
 5. Example of calculating current value when using programmable gain amplifier and comparator.
Examples 1) TYP. operating current value when three comparator channels, one internal reference voltage generator, and PGA are operating (when $AV_{REFP} = V_{DD} = 5.0\text{ V}$)

$$\begin{aligned}
 & I_{CMP} \times 3 + I_{VREF} + I_{PGA} + I_{IREF} \\
 &= 41.4 [\mu\text{A}] \times 3 + 14.8 [\mu\text{A}] \times 1 + 210 [\mu\text{A}] + 3.2 [\mu\text{A}] \\
 &= 352.2 [\mu\text{A}]
 \end{aligned}$$

- Examples 2) TYP. operating current value when using two comparator channels, without using internal reference voltage generator (when $AV_{REFP} = V_{DD} = 5.0\text{ V}$)

$$\begin{aligned}
 & I_{CMP} \times 2 + I_{IREF} \\
 &= 41.4 [\mu\text{A}] \times 2 + 3.2 [\mu\text{A}] \\
 &= 86.0 [\mu\text{A}]
 \end{aligned}$$

2.4 AC Characteristics

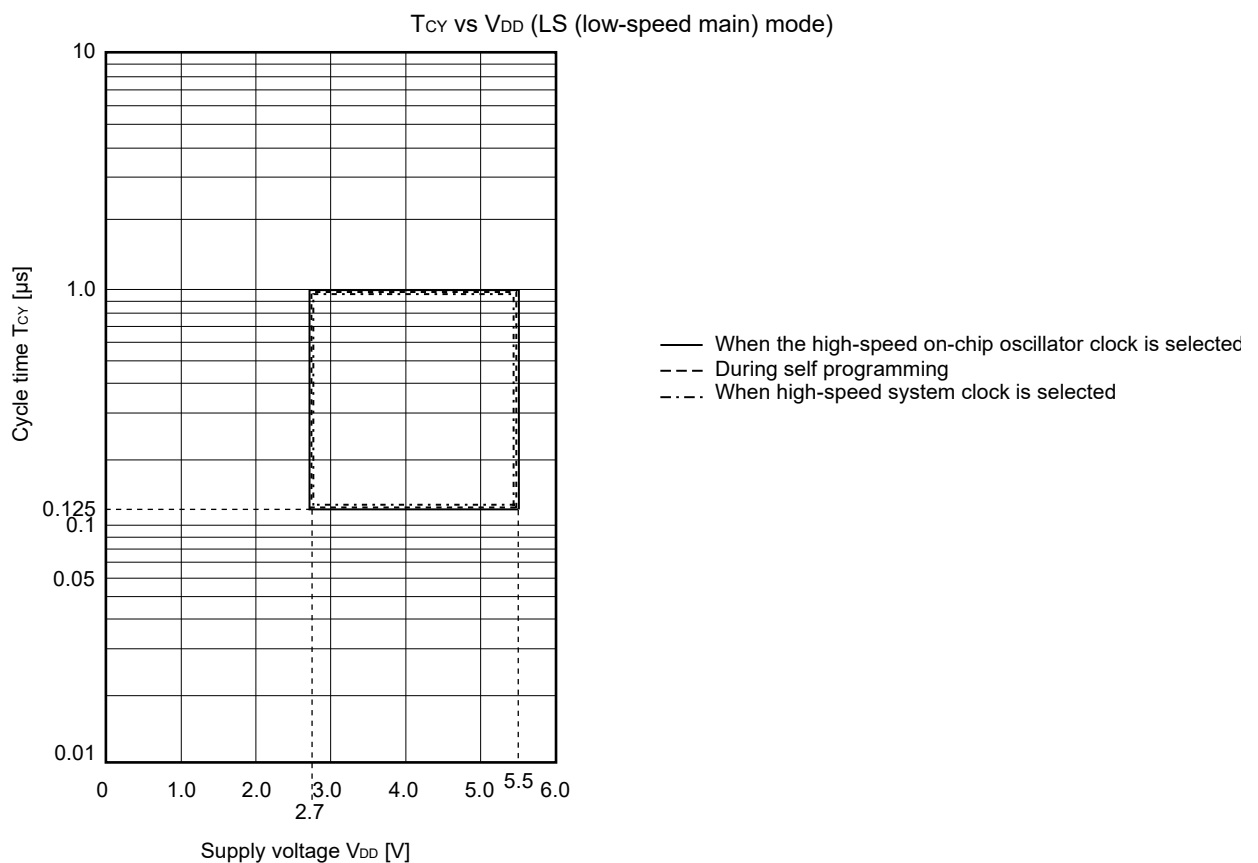
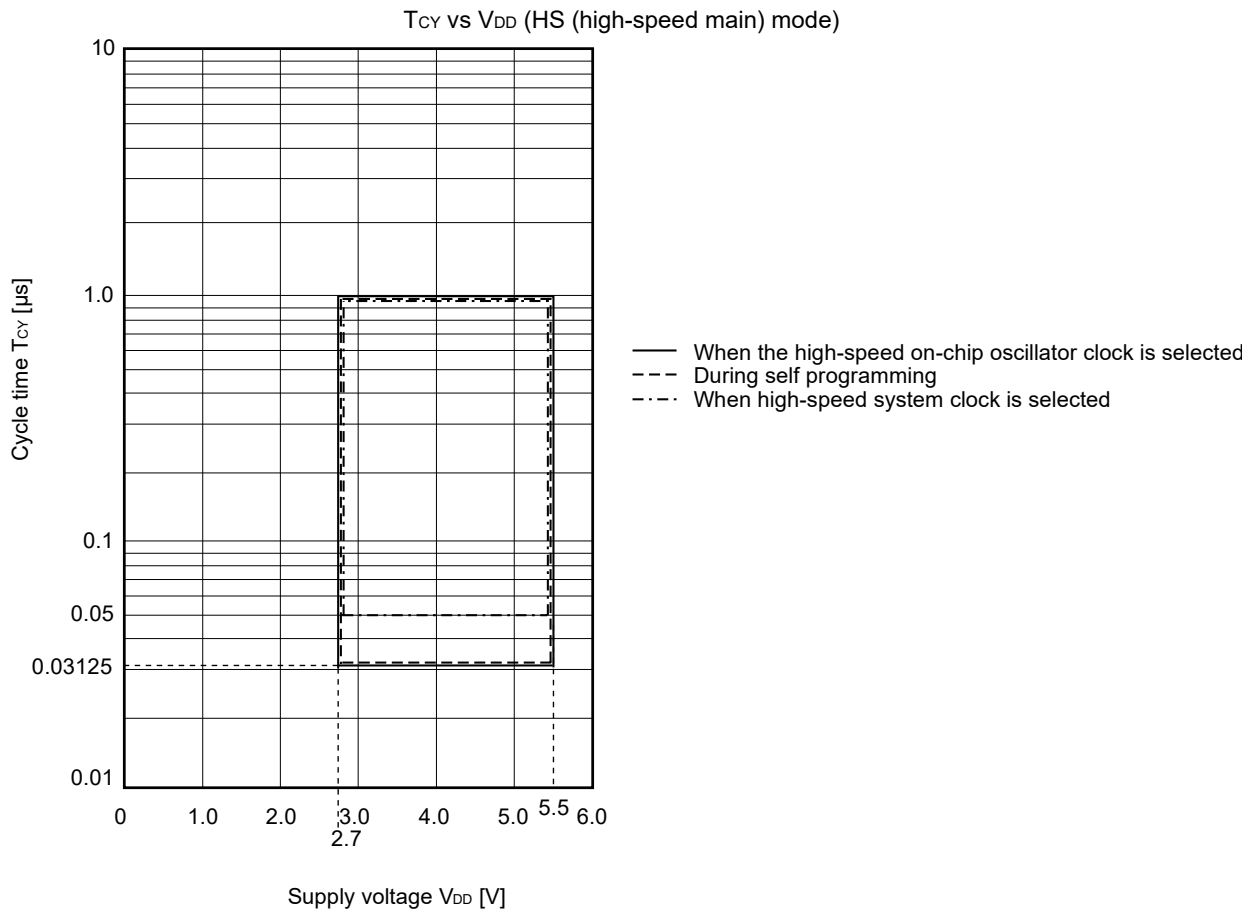
($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|------------------------------------|--|--|------------------------------------|-------|---------------|---------------|
| Instruction cycle (minimum instruction execution time) | T_{CY} | Main system clock (f_{MAIN}) operation | HS (high-speed main) mode | 0.03125 | | 1 | μs |
| | | | LS (low-speed main) mode | $T_A = -40$ to $+85^\circ\text{C}$ | 0.125 | | 1 |
| | | Subsystem clock (f_{SUB}) operation | | 28.5 | 30.5 | 31.3 | μs |
| | | In the self programming mode | HS (high-speed main) mode | 0.03125 | | 1 | μs |
| LS (low-speed main) mode | $T_A = -40$ to $+85^\circ\text{C}$ | | 0.125 | | 1 | μs | |
| External system clock frequency | f_{EX} | | | 1.0 | | 20.0 | MHz |
| | f_{EXS} | | | 32 | | 35 | kHz |
| External system clock input high-level width, low-level width | t_{EXH} , t_{EXL} | | | 24 | | | ns |
| | t_{EXHS} , t_{EXLS} | | | 13.7 | | | μs |
| Ti03, Ti05, Ti06, Ti07 input high-level width, low-level width | t_{TIH} , t_{TIL} | | | $2/f_{MCK}+10$ | | | ns |
| TO03, TO05, TO06, TKBO00, TKBO01, TKBO10, TKBO11, TKBO20, TKBO21, TKCO00 to TKCO05 output frequency (When duty = 50%) | f_{TO} | HS (high-speed main) mode | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | 8 | MHz |
| | | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ | | | 4 | MHz |
| | | LS (low-speed main) mode, $T_A = -40$ to $+85^\circ\text{C}$ | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | 4 | MHz |
| | | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ | | | 2 | MHz |
| Interrupt input high-level width, low-level width | t_{INTH} , t_{INTL} | INTP0, INTP3, INTP4, INTP9 to INTP11, INTP20 to INTP23 | | 1 | | | μs |
| $\overline{\text{RESET}}$ low-level width | t_{RSL} | | | 10 | | | μs |

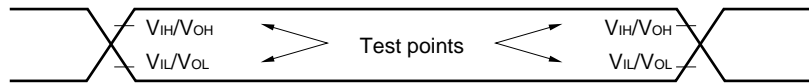
Remark f_{MCK} : Timer array unit operation clock frequency

(Operation clock to be set by the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

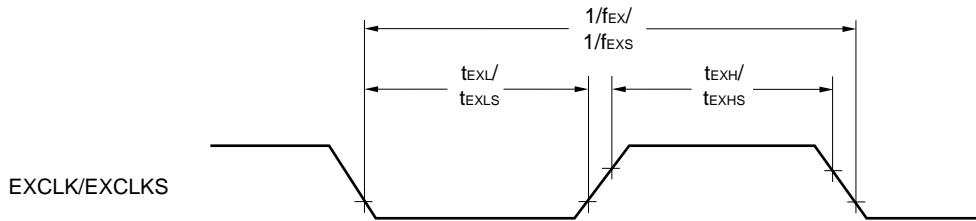
Minimum Instruction Execution Time during Main System Clock Operation



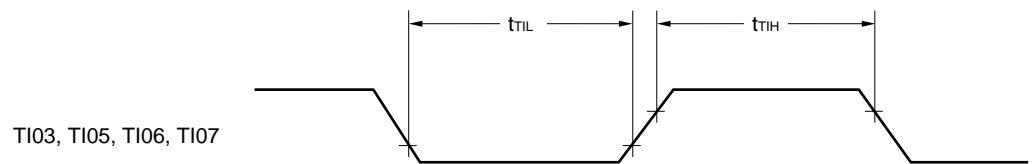
AC Timing Test Points



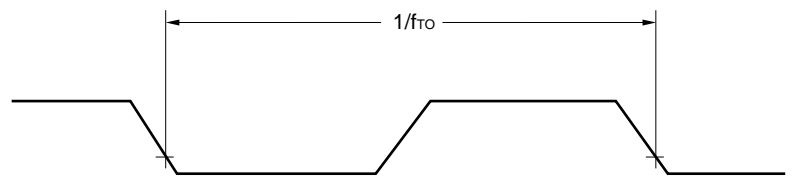
External System Clock Timing



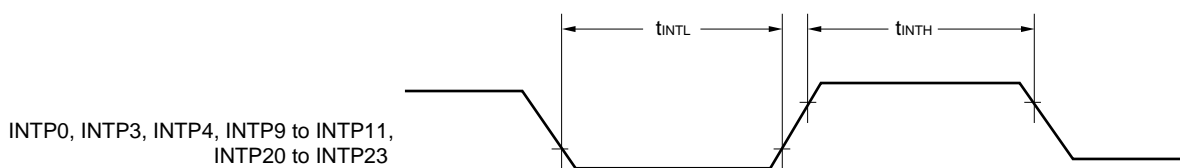
TI/TO Timing



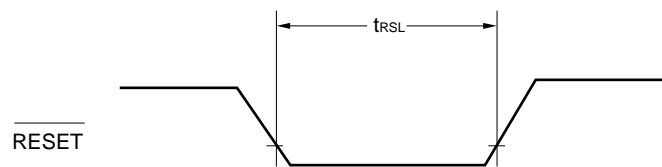
TO03, TO05, TO06, TKBO00, TKBO01, TKBO10, TKBO11, TKBO20, TKBO21, TKCO00 to TKCO05



Interrupt Request Input Timing

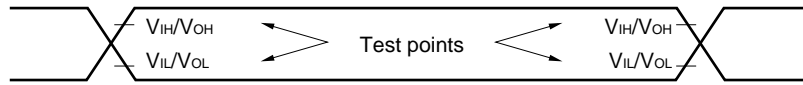


RESET Input Timing



2.5 Peripheral Functions Characteristics

AC Timing Test Points



2.5.1 Serial array unit 0, 4 (UART0, UART1, CSI00, DALI/UART4)

(1) During communication at same potential (UART mode)

($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---------------------------------|--------|--|---|-------------|--------------------------|-------------|------|
| | | | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate ^{Note 1} | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | $f_{MCK}/6$ | | $f_{MCK}/6$ | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ ^{Note 2} | 5.3 | 1.3 | Mbps | |

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

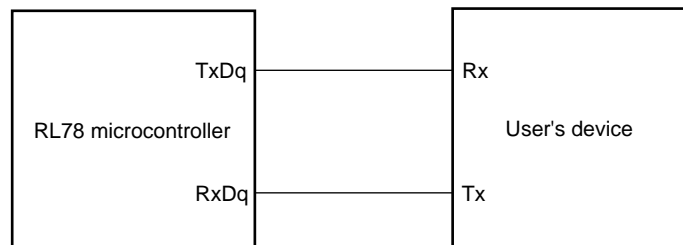
2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

HS (high-speed main) mode: 32 MHz ($2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)

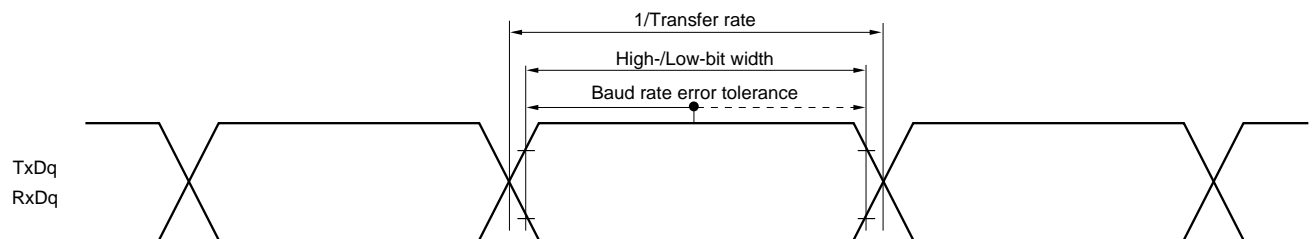
LS (low-speed main) mode: 8 MHz ($2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$), $T_A = -40$ to $+85^\circ\text{C}$

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)

2. f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00 to 03))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**($T_A = -40$ to $+105^\circ\text{C}$ ^{Note 5}, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|-------------|--|---------------------------|------|--------------------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | t_{KCY1} | $t_{KCY1} \geq 4/f_{CLK}$ | 125 | | 500 | | ns |
| SCKp high-/low-level width | t_{KH1} , | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | $t_{KCY1}/2 - 12$ | | $t_{KCY1}/2 - 50$ | | ns |
| | t_{KL1} | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | $t_{KCY1}/2 - 18$ | | $t_{KCY1}/2 - 50$ | | ns |
| Slp setup time (to SCKp \uparrow) <small>Note 1</small> | t_{SIK1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 44 | | 110 | | ns |
| | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 44 | | 110 | | ns |
| Slp hold time (from SCKp \uparrow) <small>Note 2</small> | t_{KSI1} | | 19 | | 19 | | ns |
| Delay time from SCKp \downarrow to SOp output ^{Note 3} | t_{KSO1} | $C = 30\text{ pF}$ ^{Note 4} | | 25 | | 25 | ns |

- Notes**
1. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The Slp setup time becomes “to SCKp \downarrow ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
 2. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The Slp hold time becomes “from SCKp \downarrow ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
 3. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The delay time to SOp output becomes “from SCKp \uparrow ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
 4. C is the load capacitance of the SCKp and SOp output lines.
 5. Operating conditions of LS (low-speed main) mode is $T_A = -40$ to $+85^\circ\text{C}$.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM number (g = 1)
 2. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

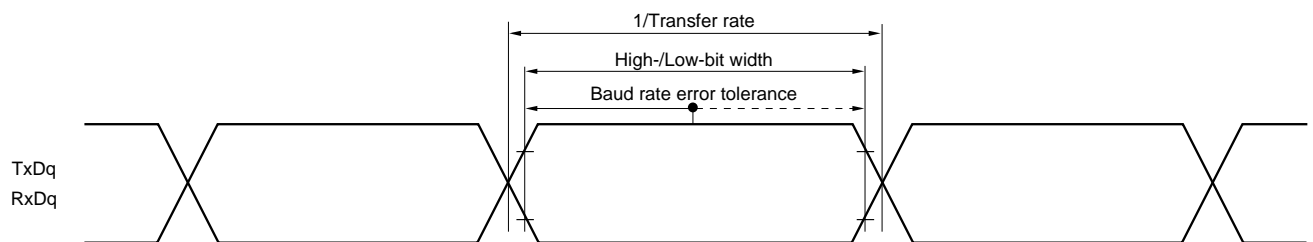
(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)
 (T_A = -40 to +105°C^{Note 6}, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|--|---------------------------------|---------------------------|---------------------------|------------------------|--------------------------|-------------------------|------|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time ^{Note 5} | t _{KCY2} | 4.0 V ≤ V _{DD} ≤ 5.5 V | 20 MHz < f _{MCK} | 8/f _{MCK} | | - | | ns |
| | | | f _{MCK} ≤ 20 MHz | 6/f _{MCK} | | 6/f _{MCK} | | ns |
| | | 2.7 V ≤ V _{DD} ≤ 5.5 V | 16 MHz < f _{MCK} | 8/f _{MCK} | | - | | ns |
| | | | f _{MCK} ≤ 16 MHz | 6/f _{MCK} | | 6/f _{MCK} | | ns |
| SCKp high-/low-level width | t _{KH2} , t _{KL2} | | | t _{KCY2} /2 | | t _{KCY2} /2 | | ns |
| Slp setup time (to SCKp↑) ^{Note 1} | t _{SIK2} | | | 1/f _{MCK} +20 | | 1/f _{MCK} +30 | | ns |
| Slp hold time (from SCKp↑) ^{Note 2} | t _{SIK2} | | | 1/f _{MCK} +31 | | 1/f _{MCK} +31 | | ns |
| Delay time from SCKp↓ to SOp output ^{Note 3} | t _{KSO2} | C = 30 pF ^{Note 4} | | | 2/f _{MCK} +44 | | 2/f _{MCK} +110 | ns |

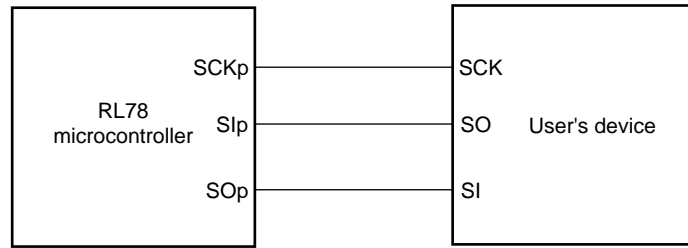
- Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 4. C is the load capacitance of the SOp output lines.
 5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps
 6. Operating conditions of LS (low-speed main) mode is T_A = -40 to +85°C.

Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

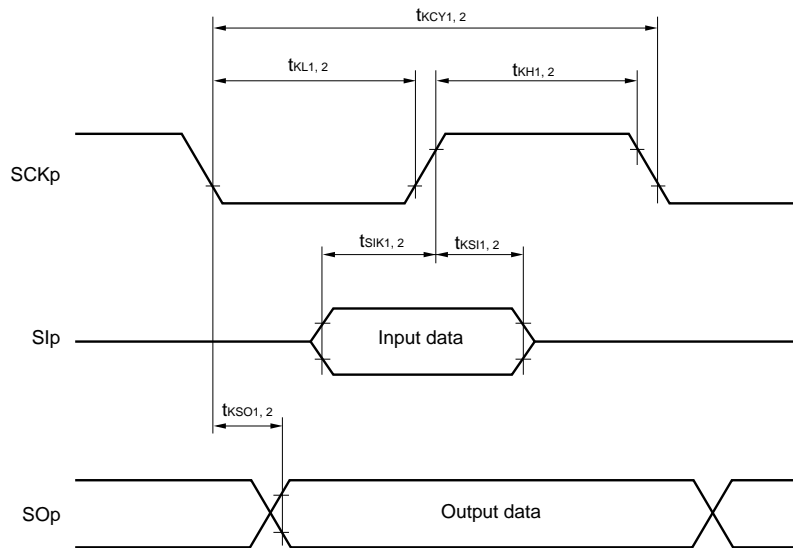
- Remarks**
1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM number (g = 1)
 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))



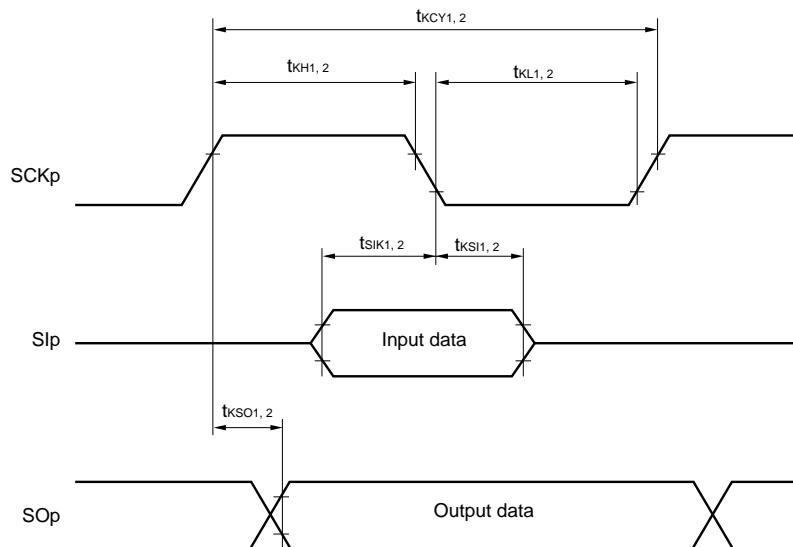
CSI mode connection diagram (during communication at same potential)



**CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



- Remarks 1. p: CSI number (p = 00)
- 2. m: Unit number, n: Channel number (mn = 00)

(4) Communication at different potential (2.5 V, 3 V) (UART mode) (1/2)**($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit | |
|---------------|--------|---|--|------|-----------------------------|-----------------------------|-----------------------------|------|
| | | | MIN. | MAX. | MIN. | MAX. | | |
| Transfer rate | | Reception | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ | | | $f_{MCK}/6^{\text{Note 1}}$ | $f_{MCK}/6^{\text{Note 1}}$ | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}^{\text{Note 2}}$ | | | 5.3 | 1.3 | Mbps |
| | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ | | | $f_{MCK}/6^{\text{Note 1}}$ | $f_{MCK}/6^{\text{Note 1}}$ | bps | |
| | | Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}^{\text{Note 2}}$ | | | 5.3 | 1.3 | Mbps | |

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.**2.** The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:HS (high-speed main) mode: 32 MHz ($2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)LS (low-speed main) mode: 8 MHz ($2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$), $T_A = -40$ to $+85^\circ\text{C}$.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

Remarks 1. $V_b[V]$: Communication line voltage**2.** q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)**3.** f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

(4) Communication at different potential (2.5 V, 3 V) (UART mode) (2/2)(T_A = -40 to +105°C ^{Note 5}, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit | | |
|---------------|--------|---|---|------|--------------------------|-----------------------|-----------------------|-----------------------|------|
| | | | MIN. | MAX. | MIN. | MAX. | | | |
| Transfer rate | | Transmission | 4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V | | | Note 1 | | Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 1.4 kΩ, V _b = 2.7 V | | | 2.8 ^{Note 2} | | 2.8 ^{Note 2} | Mbps |
| | | 2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V | | | Note 3 | | Note 3 | bps | |
| | | Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V | | | 1.2 ^{Note 4} | | 1.2 ^{Note 4} | Mbps | |

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the "Conditions" column are met. See **Note 1** above to calculate the maximum transfer rate under conditions of the customer.
- The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

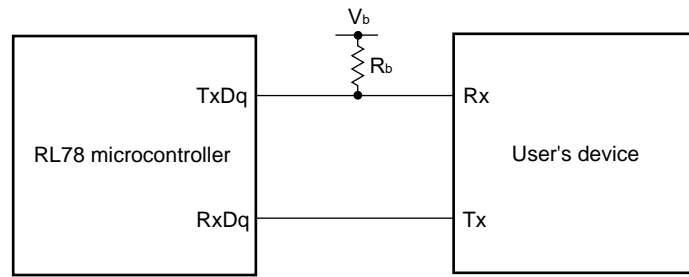
* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the "Conditions" column are met. See **Note 3** above to calculate the maximum transfer rate under conditions of the customer.
- Operating conditions of LS (low-speed main) mode is T_A = -40 to +85°C.

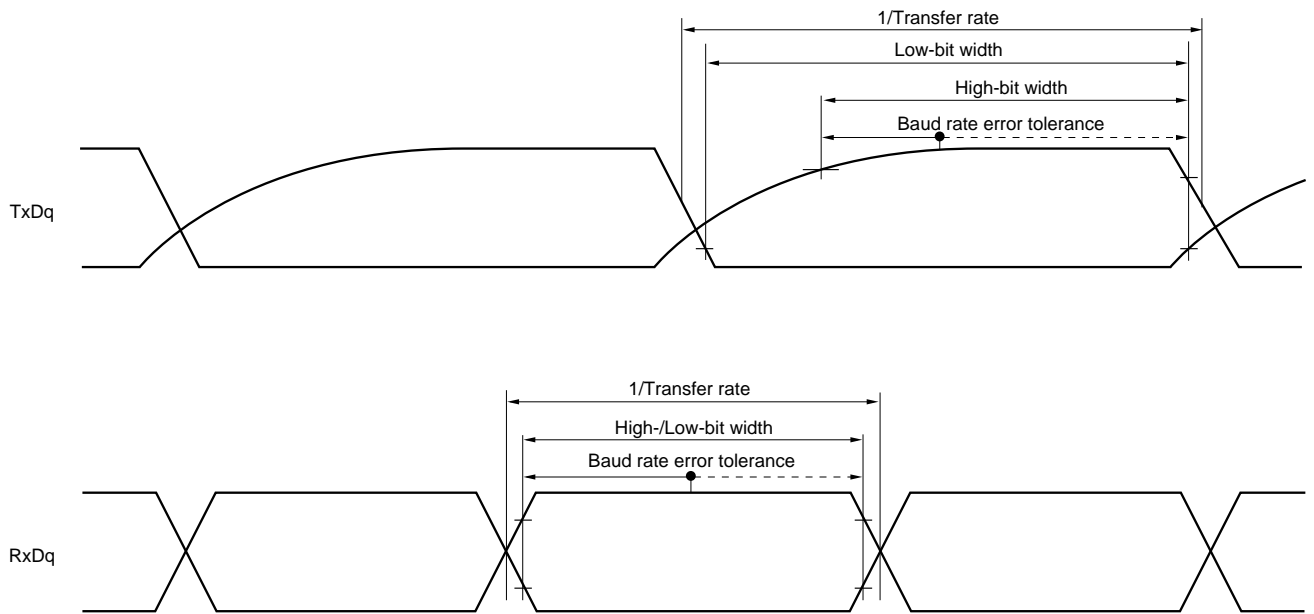
Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

- Remarks 1.** R_b[Ω]: Communication line (TxDq) pull-up resistance,
C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage
- q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)
 - f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03))

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance, $V_b[V]$: Communication line voltage
 2. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)

(5) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)
($T_A = -40$ to $+105^\circ\text{C}$ ^{Note 3}, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|------------|---|---|---------------------------|--------------------|--------------------------|--------------------|------|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | t_{KCY1} | $t_{KCY1} \geq 2/f_{CLK}$ | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | 200 | | 1150 | | ns |
| | | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | 300 | | 1150 | | ns |
| SCKp high-level width | t_{KH1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | | $t_{KCY1}/2 - 50$ | | $t_{KCY1}/2 - 75$ | | ns |
| | | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | | $t_{KCY1}/2 - 120$ | | $t_{KCY1}/2 - 170$ | |
| SCKp low-level width | t_{KL1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | | $t_{KCY1}/2 - 7$ | | $t_{KCY1}/2 - 50$ | | ns |
| | | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | | $t_{KCY1}/2 - 10$ | | $t_{KCY1}/2 - 50$ | |
| Slp setup time (to SCKp \uparrow) ^{Note 1} | t_{SIK1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | | 81 | | 479 | | ns |
| | | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | | 177 | | 479 | |
| Slp hold time (from SCKp \uparrow) ^{Note 1} | t_{KSI1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | | 10 | | 19 | | ns |
| | | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | | 10 | | 19 | |
| Delay time from SCKp \downarrow to SOp output ^{Note 1} | t_{KSO1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | | | 60 | | 100 | ns |
| | | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | | | 130 | | 195 |
| Slp setup time (to SCKp \downarrow) ^{Note 2} | t_{SIK1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | | 44 | | 110 | | ns |
| | | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | | 44 | | 110 | |
| Slp hold time (from SCKp \downarrow) ^{Note 2} | t_{KSI1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | | 10 | | 19 | | ns |
| | | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | | 10 | | 19 | |
| Delay time from SCKp \uparrow to SOp output ^{Note 2} | t_{KSO1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | | | 10 | | 25 | ns |
| | | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | | | 10 | | 25 |

- Notes**
1. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$.
 2. When $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
 3. Operating conditions of LS (low-speed main) mode is $T_A = -40$ to $+85^\circ\text{C}$.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

- Remarks**
1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[\text{F}]$: Communication line (SCKp, SOp) load capacitance, $V_b[\text{V}]$: Communication line voltage
 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

(6) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**($T_A = -40$ to $+105^\circ\text{C}$ ^{Note 3}, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

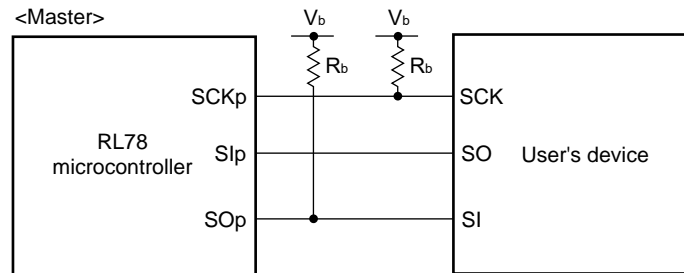
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|------------|---|---------------------------|------|--------------------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | t_{KCY1} | $t_{KCY1} \geq 4/f_{CLK}$ $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | 300 | | 1150 | | ns |
| | | | 500 | | 1150 | | ns |
| SCKp high-level width | t_{KH1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | $t_{KCY1}/2 - 75$ | | $t_{KCY1}/2 - 75$ | | ns |
| | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | $t_{KCY1}/2 - 170$ | | $t_{KCY1}/2 - 170$ | | ns |
| SCKp low-level width | t_{KL1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | $t_{KCY1}/2 - 12$ | | $t_{KCY1}/2 - 50$ | | ns |
| | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | $t_{KCY1}/2 - 18$ | | $t_{KCY1}/2 - 50$ | | ns |
| Slp setup time (to SCKp \uparrow) ^{Note 1} | t_{SIK1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | 81 | | 479 | | ns |
| | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | 177 | | 479 | | ns |
| Slp hold time (from SCKp \uparrow) ^{Note 1} | t_{KSH1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | 19 | | 19 | | ns |
| | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | 19 | | 19 | | ns |
| Delay time from SCKp \downarrow to SOP output ^{Note 1} | t_{KSO1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | | 100 | | 100 | ns |
| | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | | 195 | | 195 | ns |
| Slp setup time (to SCKp \downarrow) ^{Note 2} | t_{SIK1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | 44 | | 110 | | ns |
| | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | 44 | | 110 | | ns |
| Slp hold time (from SCKp \downarrow) ^{Note 2} | t_{KSH1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | 19 | | 19 | | ns |
| | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | 19 | | 19 | | ns |
| Delay time from SCKp \uparrow to SOP output ^{Note 2} | t_{KSO1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | | 25 | | 25 | ns |
| | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | | 25 | | 25 | ns |

- Notes**
1. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$.
 2. When $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
 3. Operating conditions of LS (low-speed main) mode is $T_A = -40$ to $+85^\circ\text{C}$.

(Caution and Remarks are listed on the next page.)

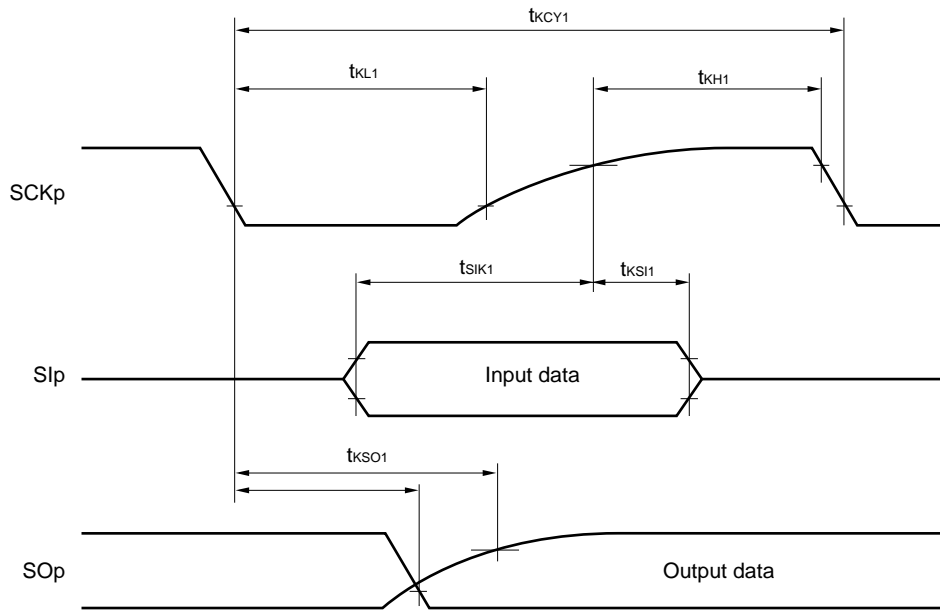
Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)

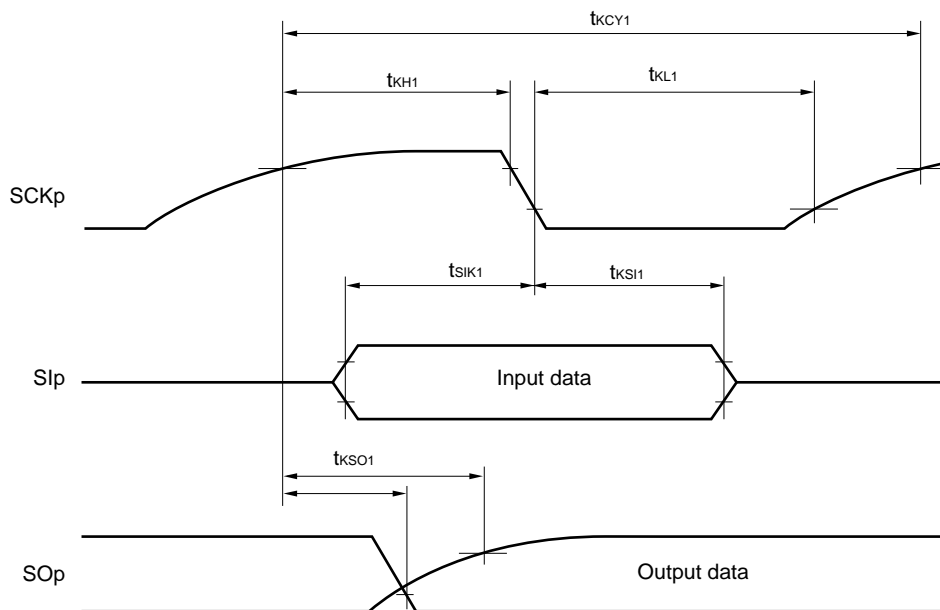


- Remarks**
1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[F]$: Communication line (SCKp, SOp) load capacitance, $V_b[V]$: Communication line voltage
 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

(7) DALI/UART4 mode

 $(T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V})$

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---------------|--------|--|---------------------------|--------------|--------------------------|--------------|------|
| | | | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate | | | | $f_{MCK}/12$ | | $f_{MCK}/12$ | bps |
| | | Maximum transfer rate theoretical value HS: $f_{CLK} = 32\text{ MHz}$, $f_{MCK} = f_{CLK}$ LS: $f_{CLK} = 8\text{ MHz}$, $f_{MCK} = f_{CLK}$ | | 2.6 | | 0.6 | Mbps |

Remark f_{MCK} : Operation clock frequency of DALI/UART.

(Operation clock to be set by the serial clock select register mn (SPS4).)

Caution Operating conditions of LS (low-speed main) mode is $T_A = -40$ to $+85^\circ\text{C}$.

2.5.2 Serial interface IICA

(1) I²C standard mode(TA = -40 to +105°C^{Note 3}, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---------------------|---|---------------------------|------|--------------------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | f _{SCL} | Standard mode: f _{CLK} ≥ 1 MHz | 0 | 100 | 0 | 100 | kHz |
| Setup time of restart condition | t _{SU:STA} | | 4.7 | | 4.7 | | μs |
| Hold time ^{Note 1} | t _{HD:STA} | | 4.0 | | 4.0 | | μs |
| Hold time when SCLA0 = "L" | t _{LOW} | | 4.7 | | 4.7 | | μs |
| Hold time when SCLA0 = "H" | t _{HIGH} | | 4.0 | | 4.0 | | μs |
| Data setup time (reception) | t _{SU:DAT} | | 250 | | 250 | | ns |
| Data hold time (transmission) ^{Note 2} | t _{HD:DAT} | | 0 | 3.45 | 0 | 3.45 | μs |
| Setup time of stop condition | t _{SU:STO} | | 4.0 | | 4.0 | | μs |
| Bus-free time | t _{BUF} | | 4.7 | | 4.7 | | μs |

- Notes**
1. The first clock pulse is generated after this period when the start/restart condition is detected.
 2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.
 3. Operating conditions of LS (low-speed main) mode is T_A = -40 to +85°C.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(2) I²C fast mode

(T_A = -40 to +105°C^{Note 3}, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

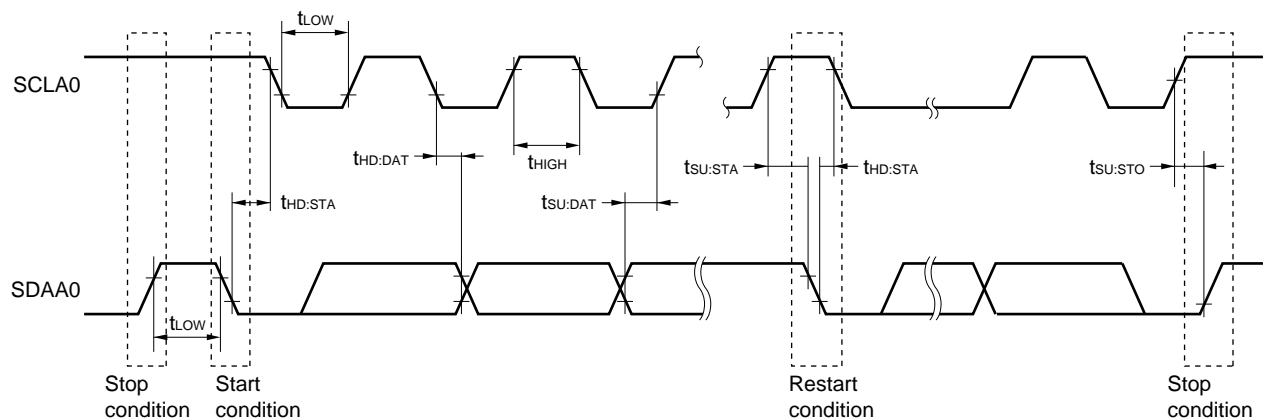
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---------------------|---------------------------------------|---------------------------|------|--------------------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | f _{SCL} | fast mode: f _{CLK} ≥ 3.5 MHz | 0 | 400 | 0 | 400 | kHz |
| Setup time of restart condition | t _{SU:STA} | | 0.6 | | 0.6 | | μs |
| Hold time ^{Note 1} | t _{HD:STA} | | 0.6 | | 0.6 | | μs |
| Hold time when SCLA0 = "L" | t _{LOW} | | 1.3 | | 1.3 | | μs |
| Hold time when SCLA0 = "H" | t _{HIGH} | | 0.6 | | 0.6 | | μs |
| Data setup time (reception) | t _{SU:DAT} | | 100 | | 100 | | ns |
| Data hold time (transmission) ^{Note 2} | t _{HD:DAT} | | 0 | 0.9 | 0 | 0.9 | μs |
| Setup time of stop condition | t _{SU:STO} | | 0.6 | | 0.6 | | μs |
| Bus-free time | t _{BUF} | | 1.3 | | 1.3 | | μs |

- Notes**
1. The first clock pulse is generated after this period when the start/restart condition is detected.
 2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.
 3. Operating conditions of LS (low-speed main) mode is T_A = -40 to +85°C.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

I²C serial transfer timing



2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

| Input channel | Reference Voltage | | |
|--|--|--|--|
| | Reference voltage (+) = AV_{REFP} Reference voltage (-) = AV_{REFM} | Reference voltage (+) = V_{DD} Reference voltage (-) = V_{SS} | Reference voltage (+) = V_{BGR} Reference voltage (-) = AV_{REFM} |
| ANI0 to ANI2, ANI4 to ANI7 | See 2.6.1 (1) . | See 2.6.1 (3) . | See 2.6.1 (4) . |
| ANI16 to ANI19 | See 2.6.1 (2) . | | |
| Internal reference voltage Temperature sensor output voltage | See 2.6.1 (1) . | | – |

(1) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin: ANI2, ANI4 to ANI7, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|--|------------------|--|--|--------|-------------|------|---------------|
| Resolution | RES | | 8 | | 10 | bit | |
| Overall error ^{Note 1} | AINL | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} | | 1.2 | ± 3.5 | LSB | |
| Conversion time | t_{CONV} | 10-bit resolution Target pin: ANI2, ANI4 to ANI7 | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.125 | | 39 | μs |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 3.1875 | | 39 | μs |
| | | 10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.375 | | 39 | μs |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 3.5625 | | 39 | μs |
| Zero-scale error ^{Notes 1, 2} | E _{ZS} | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} | | | ± 0.25 | %FSR | |
| Full-scale error ^{Notes 1, 2} | E _{FS} | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} | | | ± 0.25 | %FSR | |
| Integral linearity error ^{Note 1} | ILE | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} | | | ± 2.5 | LSB | |
| Differential linearity error ^{Note 1} | DLE | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} | | | ± 1.5 | LSB | |
| Analog input voltage | V _{AIN} | ANI2, ANI4 to ANI7 | 0 | | AV_{REFP} | V | |
| | | Internal reference voltage (HS (high-speed main) mode) | V_{BGR} ^{Note 4} | | | V | |
| | | Temperature sensor output voltage (HS (high-speed main) mode) | V_{TMS25} ^{Note 4} | | | V | |

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

4. See 2.6.2 Temperature sensor/internal reference voltage characteristics.

(2) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin: ANI16 to ANI19

($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|------------------|--|--|--------|-----------------------------|---------------|
| Resolution | RES | | 8 | | 10 | bit |
| Overall error ^{Note 1} | AINL | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Notes 3} | | 1.2 | ± 5.0 | LSB |
| Conversion time | t_{CONV} | 10-bit resolution Target ANI pin : ANI16 to ANI19 | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.125 | 39 | μs |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 3.1875 | 39 | μs |
| Zero-scale error ^{Notes 1, 2} | E _{ZS} | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Notes 3} | | | ± 0.35 | %FSR |
| Full-scale error ^{Notes 1, 2} | E _{FS} | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Notes 3} | | | ± 0.35 | %FSR |
| Integral linearity error ^{Note 1} | ILE | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Notes 3} | | | ± 3.5 | LSB |
| Differential linearity error ^{Note 1} | DLE | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Notes 3} | | | ± 2.0 | LSB |
| Analog input voltage | V _{AIN} | ANI16 to ANI19 | 0 | | AV_{REFP} and V_{DD} | V |

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

- (3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin: ANI0 to ANI2, ANI4 to ANI7, ANI16 to ANI19, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = V_{DD} , Reference voltage (-) = V_{SS})

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|-----------------|--|--|--------|------------|---------------|
| Resolution | RES | | 8 | | 10 | bit |
| Overall error ^{Note 1} | AINL | 10-bit resolution | | 1.2 | ± 7.0 | LSB |
| Conversion time | t_{CONV} | 10-bit resolution Target pin: ANI0 to ANI2, ANI4 to ANI7, ANI16 to ANI19 | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.125 | 39 | μs |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 3.1875 | 39 | μs |
| Conversion time | t_{CONV} | 10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.375 | 39 | μs |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 3.5625 | 39 | μs |
| Zero-scale error ^{Notes 1, 2} | E _{ZS} | 10-bit resolution | | | ± 0.60 | %FSR |
| Full-scale error ^{Notes 1, 2} | E _{FS} | 10-bit resolution | | | ± 0.60 | %FSR |
| Integral linearity error ^{Note 1} | ILE | 10-bit resolution | | | ± 4.0 | LSB |
| Differential linearity error ^{Note 1} | DLE | 10-bit resolution | | | ± 2.0 | LSB |
| Analog input voltage | V_{AIN} | ANI0 to ANI2, ANI4 to ANI7 | 0 | | V_{DD} | V |
| | | ANI16 to ANI19 | 0 | | V_{DD} | V |
| | | Internal reference voltage (HS (high-speed main) mode) | V_{BGR} ^{Note 3} | | | V |
| | | Temperature sensor output voltage (HS (high-speed main) mode) | V_{TMPS25} ^{Note 3} | | | V |

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. See 2.6.2 Temperature sensor/internal reference voltage characteristics.

- (4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = $AV_{REFM}/ANI1$ (ADREFM = 1), target pin: ANI0, ANI2, ANI4 to ANI7, ANI16 to ANI19

($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = V_{BGR} ^{Note 3}, Reference voltage (-) = $AV_{REFM} = 0\text{ V}$ ^{Note 4}, HS (high-speed main) mode)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|------------|------------------|------|------|-----------------------------|---------------|
| Resolution | RES | | 8 | | | bit |
| Conversion time | t_{CONV} | 8-bit resolution | 17 | | 39 | μs |
| Zero-scale error ^{Notes 1, 2} | E_{ZS} | 8-bit resolution | | | ± 0.60 | %FSR |
| Integral linearity error ^{Note 1} | ILE | 8-bit resolution | | | ± 2.0 | LSB |
| Differential linearity error ^{Note 1} | DLE | 8-bit resolution | | | ± 1.0 | LSB |
| Analog input voltage | V_{AIN} | | 0 | | V_{BGR} ^{Note 3} | V |

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. See 2.6.2 Temperature sensor/internal reference voltage characteristics.

4. When reference voltage (-) = V_{SS} , the MAX. values are as follows.

Zero-scale error: Add $\pm 0.35\%$ FSR to the MAX. value when reference voltage (-) = AV_{REFM} .

Integral linearity error: Add ± 0.5 LSB to the MAX. value when reference voltage (-) = AV_{REFM} .

Differential linearity error: Add ± 0.2 LSB to the MAX. value when reference voltage (-) = AV_{REFM} .

2.6.2 Temperature sensor/internal reference voltage characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, HS (high-speed main) mode)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------------------------|--------------|---|------|------|------|---------------|
| Temperature sensor output voltage | V_{TMPS25} | Setting ADS register = 80H, $T_A = +25^\circ\text{C}$ | | 1.05 | | V |
| Internal reference voltage | V_{BGRT} | Setting ADS register = 81H | 1.38 | 1.45 | 1.5 | V |
| Temperature coefficient | F_{VTMPS} | Temperature sensor that depends on the temperature | | -3.6 | | mV/C |
| Operation stabilization wait time | t_{AMP} | | 5 | | | μs |

2.6.3 Programmable gain amplifier

($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$, $V_{SS} = AV_{REFM} = 0\text{ V}$)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|-------------|---|--|--------------|---------|-------------------------|------------------|
| Input offset voltage | V_{IOPGA} | | | | ± 5 | ± 10 | mV |
| Input voltage range | V_{IPGA} | | | 0 | | $0.9V_{DD}/\text{gain}$ | V |
| Gain error ^{Note 1} | | 4, 8 times | | | | ± 1 | % |
| | | 16 times | | | | ± 1.5 | % |
| | | 32 times | | | | ± 2 | % |
| Slew rate ^{Note 1} | SR_{RPGA} | Rising edge | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 4, 8 times | 4 | | V/ μs |
| | | | | 16, 32 times | 1.4 | | V/ μs |
| | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ | 4, 8 times | 1.8 | | V/ μs | |
| | | | 16, 32 times | 0.5 | | V/ μs | |
| | SR_{FPGA} | Falling edge | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 4, 8 times | 3.2 | | V/ μs |
| | | | | 16, 32 times | 1.4 | | V/ μs |
| | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ | 4, 8 times | 1.2 | | V/ μs | |
| | | | 16, 32 times | 0.5 | | V/ μs | |
| Operation stabilization wait time ^{Note 2} | t_{PGA} | 4, 8 times | | 5 | | | μs |
| | | 16, 32 times | | 10 | | | μs |

Notes 1. When $V_{IPGA} = 0.1V_{DD}/\text{gain}$ to $0.9V_{DD}/\text{gain}$.

2. Time required until a state is entered where the DC and AC specifications of the PGA are satisfied after the PGA operation has been enabled ($PGAEN = 1$).

Remark These characteristics apply when AV_{REFM} is selected as GND of the PGA by using the CVRVS1 bit.

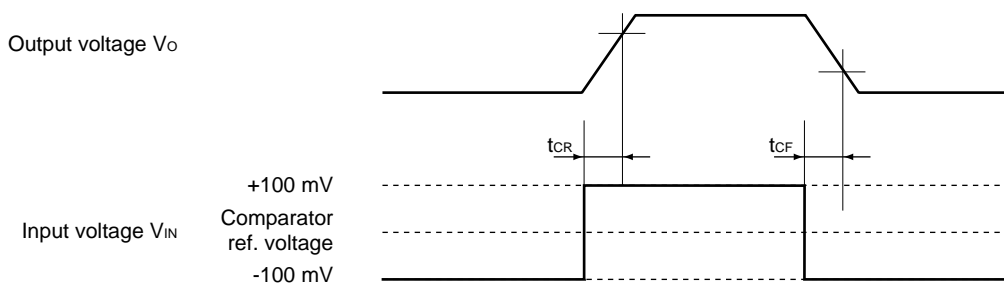
2.6.4 Comparator

($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$, $V_{SS} = AV_{REFM} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---------------------|---|-------|---------|-------------|---------------|
| Input offset voltage | V_{IOCOMP} | | | ± 5 | ± 40 | mV |
| Input voltage range | V_{ICMP} | CMP0P to CMP5P | 0 | | V_{DD} | V |
| | | CMPCOM | 0.045 | | $0.9V_{DD}$ | V |
| Internal reference voltage deviation | ΔV_{IREF} | CmRVM register values: 7FH to 80H ($m = 0$ to 2) | | | ± 2 | LSB |
| | | Other than above | | | ± 1 | LSB |
| Response time | t_{CR} , t_{CF} | Input amplitude = $\pm 100\text{ mV}$ | | 70 | 150 | ns |
| Operation stabilization wait time ^{Note 1} | t_{CMP} | $3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 1 | | | μs |
| | | $2.7\text{ V} \leq V_{DD} < 3.3\text{ V}$ | 3 | | | μs |
| Reference voltage stabilization wait time | t_{VR} | CVRE: 0 to 1 ^{Note 2} | 10 | | | μs |

- Notes**
1. Time required until a state is entered where the DC and AC specifications of the comparator are satisfied after the operation of the comparator has been enabled (CMPnEN bit = 1; $n = 0$ to 5)
 2. Enable comparator output (CnOE bit = 1; $n = 0$ to 5) after enabling operation of the internal reference voltage generator (by setting the CVREm bit to 1; $m = 0$ to 2) and waiting for the operation stabilization time to elapse.

Remark These characteristics apply when AV_{REFP} is selected as the power supply source of the internal reference voltage by using the CVRVS0 bit, and when AV_{REFM} is selected as GND of the internal reference voltage by using the CVRVS1 bit.

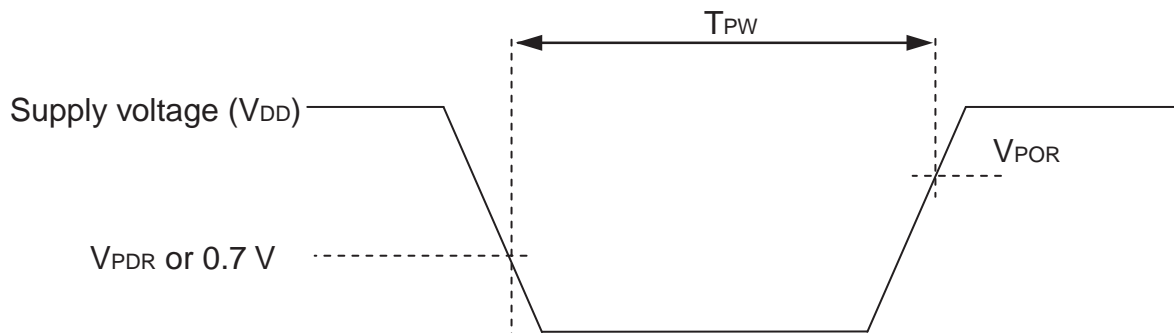


2.6.5 POR circuit characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------------------|-----------|------------------------|------|------|------|---------------|
| Detection voltage | V_{POR} | Power supply rise time | 1.45 | 1.51 | 1.57 | V |
| | V_{PDR} | Power supply fall time | 1.44 | 1.50 | 1.56 | V |
| Minimum pulse width ^{Note} | T_{PW} | | 300 | | | μs |

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR} . This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



2.6.6 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode**($T_A = -40$ to $+105^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5$ V, $V_{SS} = 0$ V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|----------------------|------------|------------------------|------|------|------|---------------|
| Detection voltage | V_{LVD0} | Power supply rise time | 3.97 | 4.06 | 4.14 | V |
| | | Power supply fall time | 3.89 | 3.98 | 4.06 | V |
| | V_{LVD1} | Power supply rise time | 3.67 | 3.75 | 3.82 | V |
| | | Power supply fall time | 3.59 | 3.67 | 3.74 | V |
| | V_{LVD2} | Power supply rise time | 3.06 | 3.13 | 3.19 | V |
| | | Power supply fall time | 2.99 | 3.06 | 3.12 | V |
| | V_{LVD3} | Power supply rise time | 2.95 | 3.02 | 3.08 | V |
| | | Power supply fall time | 2.89 | 2.96 | 3.02 | V |
| | V_{LVD4} | Power supply rise time | 2.85 | 2.92 | 2.97 | V |
| | | Power supply fall time | 2.79 | 2.86 | 2.91 | V |
| | V_{LVD5} | Power supply rise time | 2.75 | 2.81 | 2.87 | V |
| | | Power supply fall time | 2.70 | 2.75 | 2.81 | V |
| Minimum pulse width | t_{LW} | | 300 | | | μs |
| Detection delay time | | | | | 300 | μs |

LVD Detection Voltage of Interrupt & Reset Mode**($T_A = -40$ to $+105^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5$ V, $V_{SS} = 0$ V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|---------------------------|------------|---|------------------------------|------|------|------|---|
| Interrupt and reset mode | V_{LVD0} | $V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1$, falling reset voltage: 2.7 V | 2.70 | 2.75 | 2.81 | V | |
| | V_{LVD1} | LVIS1, LVIS0 = 1, 0 | Rising release reset voltage | 2.85 | 2.92 | 2.97 | V |
| | | | Falling interrupt voltage | 2.79 | 2.86 | 2.91 | V |
| | V_{LVD2} | LVIS1, LVIS0 = 0, 1 | Rising release reset voltage | 2.95 | 3.02 | 3.08 | V |
| | | | Falling interrupt voltage | 2.89 | 2.96 | 3.02 | V |
| | V_{LVD3} | LVIS1, LVIS0 = 0, 0 | Rising release reset voltage | 3.97 | 4.06 | 4.14 | V |
| Falling interrupt voltage | | | 3.89 | 3.98 | 4.06 | V | |

2.6.7 Supply voltage rise inclination characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0$ V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---------------------|-----------|------------|------|------|------|------|
| Supply voltage rise | SV_{DD} | | | | 54 | V/ms |

Caution Keep the internal reset status by using the LVD circuit or an external reset signal until V_{DD} rises to within the operating voltage range shown in 32.4 AC Characteristics.

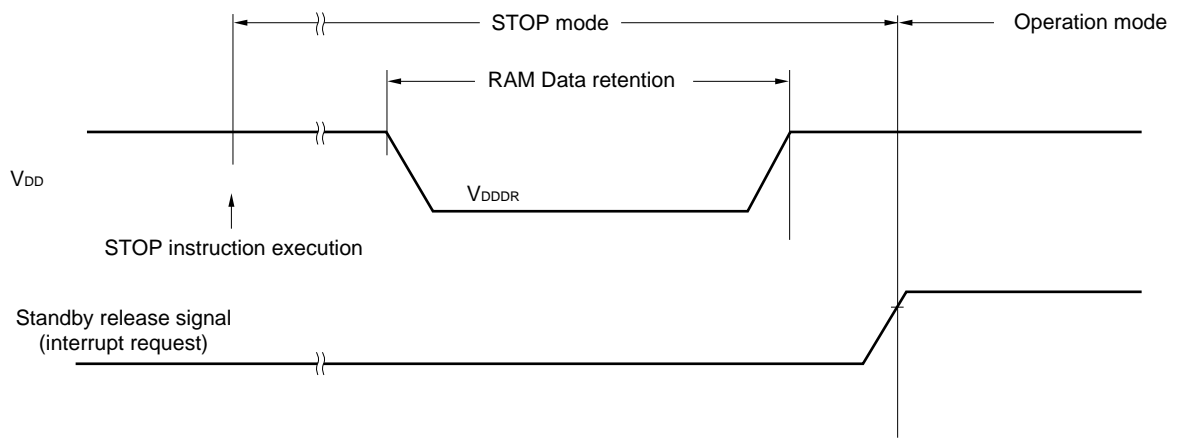
2.7 RAM Data Retention Characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|------------|------------|------------------------|------|------|------|
| Data retention supply voltage ^{Note 2} | V_{DDDR} | | 1.44 ^{Note 1} | | 5.5 | V |

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.

Caution When CPU is operated at the voltage of out of the operation voltage range, RAM data is not retained. Therefore, set STOP mode before the supplied voltage is below the operation voltage range.



2.8 Flash Memory Programming Characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|-------------------|---|---------|-----------|------|-------|
| CPU/peripheral hardware clock frequency | f _{CLK} | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 1 | | 32 | MHz |
| Number of code flash rewrites ^{Notes 1, 2, 3} | C _{enwr} | Retained for 20 years, $T_A = 85^\circ\text{C}$ ^{Note 3} | 1,000 | | | Times |
| Number of data flash rewrites ^{Notes 1, 2, 3} | | Retained for 1 year, $T_A = 25^\circ\text{C}$ ^{Note 3} | | 1,000,000 | | |
| | | Retained for 5 years, $T_A = 85^\circ\text{C}$ ^{Note 3} | 100,000 | | | |
| | | Retained for 20 years, $T_A = 85^\circ\text{C}$ ^{Note 3} | 10,000 | | | |

- Notes 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
- 2.** When using flash memory programmer and Renesas Electronics self programming library
- 3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 Dedicated Flash Memory Programmer Communication (UART)

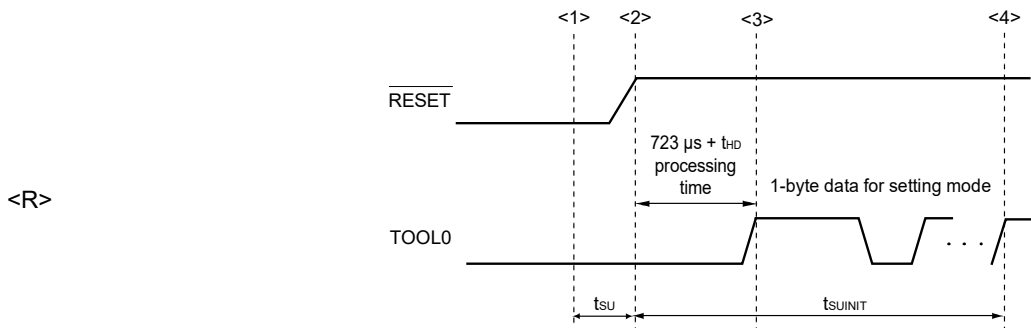
($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---------------|--------|---------------------------|---------|------|------|------|
| Transfer rate | | During serial programming | 115.2 k | | 1 M | bps |

2.10 Timing of Entry to Flash Memory Programming Modes

($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|----------------------|--|------|------|------|---------------|
| How long from when an external reset ends until the initial communication settings are specified | t_{SUIINIT} | POR and LVD reset must end before the external reset ends. | | | 100 | ms |
| How long from when the TOOL0 pin is placed at the low level until an external reset ends | t_{SU} | POR and LVD reset must end before the external reset ends. | 10 | | | μs |
| How long the TOOL0 pin must be kept at the low level after a reset ends (except soft processing time) | t_{HD} | POR and LVD reset must end before the external reset ends. | 1 | | | ms |



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset ends (POR and LVD reset must end before the pin reset ends.).
- <3> The TOOL0 pin is set to the high level.
- <4> Complete the baud rate setting by UART reception.

Remark t_{SUIINIT} : The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

t_{SU} : How long from when the TOOL0 pin is placed at the low level until an external reset ends

t_{HD} : How long to keep the TOOL0 pin at the low level from when the external and internal resets end (except soft processing time)

3. ELECTRICAL SPECIFICATIONS

(M: Industrial applications, $T_A = -40$ to $+125^\circ\text{C}$)

In this chapter, shows the electrical specifications of the target products.

Target products (M: Industrial applications): $T_A = -40$ to $+125^\circ\text{C}$
R5F107xxMxx

- Cautions**
1. The RL78/I1A has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
 2. The pins mounted depend on the product. See 2.1 Port Function to 2.2.1 Functions for each product in the RL78/I1A User's Manual.
 3. When any of these products are used at 105°C or lower, see 2. ELECTRICAL SPECIFICATIONS ($T_A = -40$ to $+105^\circ\text{C}$).

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$) (1/2)

| Parameter | Symbols | Conditions | Ratings | Unit |
|------------------------|------------|--|---|------|
| Supply voltage | V_{DD} | | -0.5 to +6.5 | V |
| REGC pin input voltage | V_{REGC} | REGC | -0.3 to +2.8 and -0.3 to $V_{DD} + 0.3$ ^{Note 1} | V |
| Input voltage | V_{I1} | P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120 to P124, P137, P147, P200 to P206, EXCLK, EXCLKS, RESET | -0.3 to $V_{DD} + 0.3$ ^{Note 2} | V |
| Output voltage | V_{O1} | P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120, P147, P200 to P206 | -0.3 to $V_{DD} + 0.3$ ^{Note 2} | V |
| Analog input voltage | V_{AI1} | ANI0 to ANI2, ANI4 to ANI7, ANI16 to ANI19 | -0.3 to $V_{DD} + 0.3$ and -0.3 to $AV_{REF(+)}$ $+0.3$ ^{Notes 2, 3} | V |

- Notes**
1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.
 2. Must be 6.5 V or lower.
 3. Do not exceed $AV_{REF(+)} + 0.3$ V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

- Remarks**
1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
 2. $AV_{REF(+)}$: + side reference voltage of the A/D converter.
 3. V_{SS} : Reference voltage

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$) (2/2)

| Parameter | Symbols | Conditions | | Ratings | Unit |
|-------------------------------|----------------------------------|------------------------------|---|---|------------------|
| Output current, high | I_{OH1} | Per pin | P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206 | -40 | mA |
| | | Total of all pins -170 mA | P02, P03, P40, P120 | -70 | mA |
| | | | P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206 | -100 | mA |
| | | I_{OH2} | Per pin | P20 to P22, P24 to P27 | -0.5 |
| | Total of all pins | | | -2 | mA |
| | Output current, low | I_{OL1} | Per pin | P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206 | 40 |
| Total of all pins 170 mA | | | P02, P03, P40, P120 | 70 | mA |
| | | | P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206 | 100 | mA |
| I_{OL2} | | | Per pin | P20 to P22, P24 to P27 | 1 |
| | | Total of all pins | | 5 | mA |
| Operating ambient temperature | | T_A | In normal operation mode | | -40 to +125 |
| | In flash memory programming mode | | -40 to +105 | | |
| Storage temperature | T_{stg} | | | -65 to +150 | $^\circ\text{C}$ |

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.2 Oscillator Characteristics

3.2.1 X1, XT1 oscillator characteristics

($T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Parameter | Resonator | Conditions | MIN. | TYP. | MAX. | Unit |
|--|---|------------|------|--------|------|------|
| X1 clock frequency (f_x) ^{Note} | Ceramic resonator/ crystal resonator | | 1.0 | | 20.0 | MHz |
| XT1 clock frequency (f_{XT}) ^{Note} | Crystal resonator | | 32 | 32.768 | 35 | kHz |

Note Indicates only permissible oscillator frequency ranges. See **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, see 5.4 System Clock Oscillator in the RL78/I1A User's Manual.

3.2.2 On-chip oscillator characteristics

($T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Oscillators | Parameters | Conditions | MIN. | TYP. | MAX. | Unit |
|--|------------|--|------|------|------|------|
| High-speed on-chip oscillator clock frequency ^{Note 1} | f_{IH} | | 1 | | 32 | MHz |
| High-speed on-chip oscillator clock frequency accuracy ^{Note 2} | | $T_A = -20$ to 85°C | -1 | | +1 | % |
| | | $T_A = -40$ to 105°C | -1.5 | | +1.5 | % |
| | | $T_A = -40$ to 125°C When 16 MHz selected | -2 | | +2 | % |
| Low-speed on-chip oscillator clock frequency | f_{IL} | | | 15 | | kHz |
| Low-speed on-chip oscillator clock frequency accuracy | | | -15 | | +15 | % |

Notes 1. Frequency can be selected in a high-speed on-chip oscillator. Selected by bits 0 to 3 of option byte (000C2H/010C2H).

2. This indicates the oscillator characteristics only. See **AC Characteristics** for instruction execution time.

Remark When using the device at an ambient temperature that exceeds $T_A = 105^\circ\text{C}$, the selectable oscillation frequency is 16 MHz max.

3.2.3 PLL characteristics

($T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|-------------|---|-----------------------|------|------|------|
| PLL input clock frequency ^{Note} | f_{PLLIN} | High-speed system clock is selected ($f_{MX} = 4\text{ MHz}$) | 3.92 | 4.00 | 4.08 | MHz |
| | | High-speed on-chip oscillator clock is selected ($f_{IH} = 4\text{ MHz}$) | 3.92 | 4.00 | 4.08 | MHz |
| PLL output clock frequency ^{Note} | f_{PLL} | | $f_{PLLIN} \times 16$ | | | MHz |

Note This only indicates the oscillator characteristics. See **AC Characteristics** for instruction execution time.

Remark When using the device at an ambient temperature that exceeds $T_A = 105^\circ\text{C}$, only 16 MHz ($f_{PLL} \times 1/4$) can be selected as the CPU operating frequency.

3.3 DC Characteristics

3.3.1 Pin characteristics

($T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|--|---|---|--|------|------------------------|------------------------|----|
| Output current, high ^{Note 1} | I _{OH1} | Per pin for P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206 | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | -3.0 ^{Note 2} | mA |
| | | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ | | | -1.0 | mA |
| | | Total of P02, P03, P40, P120 (When duty $\leq 70\%$ ^{Note 3}) | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | -9.0 | mA |
| | | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ | | | -3.0 | mA |
| | | Total of P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206 (When duty $\leq 70\%$ ^{Note 3}) | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | -21.0 | mA |
| | | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ | | | -6.0 | mA |
| | Total of all pins (When duty $\leq 70\%$ ^{Note 3}) | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | -21.0 | mA | |
| | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ | | | -9.0 | mA | |
| I _{OH2} | Per pin for P20 to P22, P24 to P27 | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | -0.1 ^{Note 2} | mA | |
| | | Total of all pins (When duty $\leq 70\%$ ^{Note 3}) | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | -0.4 | mA |

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor $\leq 70\%$.

The output current value that has changed to the duty factor $> 70\%$ the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = $(I_{OH} \times 0.7)/(n \times 0.01)$

<Example> Where $n = 80\%$ and $I_{OH} = -10.0\text{ mA}$

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(80 \times 0.01) \cong -8.7\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Caution P02, P10 to P12 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|---|---|--|--|------|-----------------------|-----------------------|----|
| Output current, $I_{OL}^{\text{Note 1}}$ | I _{OL1} | Per pin for P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206 | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | 8.5 ^{Note 2} | mA |
| | | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ | | | 1.5 ^{Note 2} | mA |
| | | Total of P02, P03, P40, P120 (When duty $\leq 70\%$ ^{Note 3}) | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | 20.0 | mA |
| | | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ | | | 5.0 | mA |
| | | Total of P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206 (When duty $\leq 70\%$ ^{Note 3}) | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | 20.0 | mA |
| | | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ | | | 10.0 | mA |
| | Total of all pins (When duty $\leq 70\%$ ^{Note 3}) | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | 40.0 | mA | |
| | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ | | | 15.0 | mA | |
| I _{OL2} | Per pin for P20 to P22, P24 to P27 | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | 0.4 ^{Note 2} | mA | |
| | | Total of all pins (When duty $\leq 70\%$ ^{Note 3}) | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | 1.6 | mA |

- Notes**
- Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.
 - However, do not exceed the total current value.
 - Specification under conditions where the duty factor $\leq 70\%$.
The output current value that has changed to the duty factor $> 70\%$ the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
 - Total output current of pins = $(I_{OL} \times 0.7)/(n \times 0.01)$
<Example> Where $n = 80\%$ and $I_{OL} = -10.0\text{ mA}$
Total output current of pins = $(-10.0 \times 0.7)/(80 \times 0.01) \cong -8.7\text{ mA}$
 However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | | |
|---------------------|-----------|---|--|---|------|-------------|----------|---|
| Input voltage, high | V_{IH1} | P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120 to P124, P137, P147, P200 to P206, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | Normal input buffer | $0.8V_{DD}$ | | V_{DD} | V | |
| | | | TTL input buffer $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.1 | | V_{DD} | V | |
| | | | | TTL input buffer $3.3\text{ V} \leq V_{DD} < 4.0\text{ V}$ | 2.0 | | V_{DD} | V |
| | | | | TTL input buffer $2.7\text{ V} \leq V_{DD} < 3.3\text{ V}$ | 1.5 | | V_{DD} | V |
| Input voltage, low | V_{IL1} | P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120 to P124, P137, P147, P200 to P206, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | Normal input buffer | 0 | | $0.2V_{DD}$ | V | |
| | | | TTL input buffer $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 0 | | 0.8 | V | |
| | | | | TTL input buffer $3.3\text{ V} \leq V_{DD} < 4.0\text{ V}$ | 0 | | 0.5 | V |
| | | | | TTL input buffer $2.7\text{ V} \leq V_{DD} < 3.3\text{ V}$ | 0 | | 0.32 | V |
| | V_{IL2} | P03, P10, P11 | TTL input buffer $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 0 | | 0.8 | V | |
| | | | TTL input buffer $3.3\text{ V} \leq V_{DD} < 4.0\text{ V}$ | 0 | | 0.5 | V | |
| | | | TTL input buffer $2.7\text{ V} \leq V_{DD} < 3.3\text{ V}$ | 0 | | 0.32 | V | |

Caution The maximum value of V_{IH} of pins P02, P10 to P12 is V_{DD} , even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|----------------------|------------------|---|---|----------------|------|------|
| Output voltage, high | V _{OH1} | P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206 | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -3.0\text{ mA}$ | $V_{DD} - 0.7$ | | V |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -1.0\text{ mA}$ | $V_{DD} - 0.5$ | | V |
| | V _{OH2} | P20 to P22, P24 to P27 | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH2} = -100\ \mu\text{A}$ | $V_{DD} - 0.5$ | | V |
| Output voltage, low | V _{OL1} | P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206 | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 8.5\text{ mA}$ | | 0.7 | V |
| | | | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 4.0\text{ mA}$ | | 0.4 | V |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 1.5\text{ mA}$ | | 0.4 | V |
| | V _{OL2} | P20 to P22, P24 to P27 | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL2} = 400\ \mu\text{A}$ | | 0.4 | V |

Caution P02, P10 to P12 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | | |
|-----------------------------|------------|--|--------------------------------|---------------------------------------|------|------|------------------|---------------|
| Input leakage current, high | I_{LIH1} | P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120, P137, P147, P200 to P206, RESET | $V_i = V_{DD}$ | | | 1 | μA | |
| | I_{LIH2} | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS) | $V_i = V_{DD}$ | In input port or external clock input | | | 1 | μA |
| | | | | In resonator connection | | | 10 | μA |
| Input leakage current, low | I_{LIL1} | P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120, P137, P147, P200 to P206, RESET | $V_i = V_{SS}$ | | | -1 | μA | |
| | I_{LIL2} | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS) | $V_i = V_{SS}$ | In input port or external clock input | | | -1 | μA |
| | | | | In resonator connection | | | -10 | μA |
| On-chip pull-up resistance | R_U | P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206 | $V_i = V_{SS}$, In input port | 10 | 20 | 100 | $\text{k}\Omega$ | |

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.3.2 Supply current characteristics

 $(T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$) (1/2)

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|--|----------------------|---|---|--|-------------------------|---------------|------|---------------|------|
| Supply current Note 1 | I _{DD1} | Operating mode | HS (high-speed main) mode ^{Note 5} | f _{IH} = 16 MHz ^{Note 3} | V _{DD} = 5.0 V | | 2.9 | 4.8 | mA |
| | | | | | V _{DD} = 3.0 V | | 2.9 | 4.8 | mA |
| | | HS (high-speed main) mode ^{Note 5} | f _{MX} = 20 MHz ^{Note 2} , V _{DD} = 5.0 V | Square wave input | | 3.2 | 5.6 | mA | |
| | | | | Resonator connection | | 3.3 | 5.7 | mA | |
| | | | f _{MX} = 20 MHz ^{Note 2} , V _{DD} = 3.0 V | Square wave input | | 3.2 | 5.6 | mA | |
| | | | | Resonator connection | | 3.3 | 5.7 | mA | |
| | | | f _{MX} = 10 MHz ^{Note 2} , V _{DD} = 5.0 V | Square wave input | | 2.0 | 3.3 | mA | |
| | | | | Resonator connection | | 2.0 | 3.3 | mA | |
| | | | f _{MX} = 10 MHz ^{Note 2} , V _{DD} = 3.0 V | Square wave input | | 2.0 | 3.3 | mA | |
| | | | | Resonator connection | | 2.0 | 3.3 | mA | |
| | | HS (high-speed main) mode ^{Note 5} | f _{IH} = 4 MHz ^{Note 3} f _{PLL} = 64 MHz, f _{CLK} = 16 MHz | V _{DD} = 5.0 V | | 3.3 | 6.5 | mA | |
| | | | | V _{DD} = 3.0 V | | 3.3 | 6.5 | mA | |
| | | Subsystem clock operation | f _{SUB} = 32.768 kHz ^{Note 4} T _A = -40°C | Square wave input | | 4.2 | 6.0 | μA | |
| | | | | Resonator connection | | 4.4 | 6.2 | μA | |
| | | | f _{SUB} = 32.768 kHz ^{Note 4} T _A = $+25^\circ\text{C}$ | Square wave input | | 4.2 | 6.0 | μA | |
| | | | | Resonator connection | | 4.4 | 6.2 | μA | |
| | | | f _{SUB} = 32.768 kHz ^{Note 4} T _A = $+50^\circ\text{C}$ | Square wave input | | 4.3 | 7.2 | μA | |
| | | | | Resonator connection | | 4.5 | 7.4 | μA | |
| | | | f _{SUB} = 32.768 kHz ^{Note 4} T _A = $+70^\circ\text{C}$ | Square wave input | | 4.4 | 8.1 | μA | |
| | | | | Resonator connection | | 4.6 | 8.3 | μA | |
| f _{SUB} = 32.768 kHz ^{Note 4} T _A = $+85^\circ\text{C}$ | Square wave input | | | 5.2 | 11.4 | μA | | | |
| | Resonator connection | | | 5.4 | 11.6 | μA | | | |
| f _{SUB} = 32.768 kHz ^{Note 4} T _A = $+105^\circ\text{C}$ | Square wave input | | | 6.9 | 20.8 | μA | | | |
| | Resonator connection | | | 7.1 | 21.0 | μA | | | |
| f _{SUB} = 32.768 kHz ^{Note 4} T _A = $+125^\circ\text{C}$ | Square wave input | | 11.1 | 51.2 | μA | | | | |
| | Resonator connection | | 11.3 | 51.4 | μA | | | | |

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, comparator, programmable gain amplifier, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }20\text{ MHz}$

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

($T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$) (2/2)

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit | |
|----------------------------|---------------------------|----------------------------|--|---|---------------------------|----------------------|---------------|---------------|------|---------------|
| Supply current Note 1 | I_{DD2} Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{IH} = 16\text{ MHz}$ Note 4 | $V_{DD} = 5.0\text{ V}$ | | 0.50 | 2.0 | mA | |
| | | | | | $V_{DD} = 3.0\text{ V}$ | | 0.50 | 2.0 | mA | |
| | | | HS (high-speed main) mode Note 7 | $f_{MX} = 20\text{ MHz}$ Note 3, $V_{DD} = 5.0\text{ V}$ | Square wave input | | 0.40 | 2.2 | mA | |
| | | | | | Resonator connection | | 0.50 | 2.3 | mA | |
| | | | | $f_{MX} = 20\text{ MHz}$ Note 3, $V_{DD} = 3.0\text{ V}$ | Square wave input | | 0.40 | 2.2 | mA | |
| | | | | | Resonator connection | | 0.50 | 2.3 | mA | |
| | | | | $f_{MX} = 10\text{ MHz}$ Note 3, $V_{DD} = 5.0\text{ V}$ | Square wave input | | 0.24 | 1.22 | mA | |
| | | | | | Resonator connection | | 0.30 | 1.28 | mA | |
| | | | $f_{MX} = 10\text{ MHz}$ Note 3, $V_{DD} = 3.0\text{ V}$ | Square wave input | | 0.24 | 1.22 | mA | | |
| | | | | Resonator connection | | 0.30 | 1.28 | mA | | |
| | | | HS (high-speed main) mode Note 7 | $f_{IH} = 4\text{ MHz}$ Note 4 $f_{PLL} = 64\text{ MHz}$, $f_{CLK} = 16\text{ MHz}$ | $V_{DD} = 5.0\text{ V}$ | | 0.95 | 3.7 | mA | |
| | | | | | $V_{DD} = 3.0\text{ V}$ | | 0.95 | 3.7 | mA | |
| | | | Subsystem clock operation | $f_{SUB} = 32.768\text{ kHz}$ Note 5 | $T_A = -40^\circ\text{C}$ | Square wave input | | 0.28 | 0.70 | μA |
| | | | | | | Resonator connection | | 0.47 | 0.89 | μA |
| | $T_A = +25^\circ\text{C}$ | Square wave input | | | | 0.33 | 0.70 | μA | | |
| | | Resonator connection | | | | 0.52 | 0.89 | μA | | |
| | $T_A = +50^\circ\text{C}$ | Square wave input | | | | 0.41 | 1.90 | μA | | |
| | | Resonator connection | | | | 0.60 | 2.09 | μA | | |
| | $T_A = +70^\circ\text{C}$ | Square wave input | | | | 0.54 | 2.80 | μA | | |
| | | Resonator connection | | | | 0.73 | 2.99 | μA | | |
| $T_A = +85^\circ\text{C}$ | Square wave input | | | | 1.27 | 6.10 | μA | | | |
| | Resonator connection | | | | 1.46 | 6.29 | μA | | | |
| $T_A = +105^\circ\text{C}$ | Square wave input | | 3.04 | 15.5 | μA | | | | | |
| | Resonator connection | | 3.23 | 15.7 | μA | | | | | |
| $T_A = +125^\circ\text{C}$ | Square wave input | | 7.20 | 45.2 | μA | | | | | |
| | Resonator connection | | 7.53 | 45.5 | μA | | | | | |
| I_{DD3} Note 6 | STOP mode Note 8 | $T_A = -40^\circ\text{C}$ | | | 0.18 | 0.50 | μA | | | |
| | | $T_A = +25^\circ\text{C}$ | | | 0.23 | 0.50 | μA | | | |
| | | $T_A = +50^\circ\text{C}$ | | | 0.27 | 1.70 | μA | | | |
| | | $T_A = +70^\circ\text{C}$ | | | 0.44 | 2.60 | μA | | | |
| | | $T_A = +85^\circ\text{C}$ | | | 1.17 | 5.90 | μA | | | |
| | | $T_A = +105^\circ\text{C}$ | | | 2.94 | 15.3 | μA | | | |
| | | $T_A = +125^\circ\text{C}$ | | | 7.14 | 45.1 | μA | | | |

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, comparator, programmable gain amplifier, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When $RTCLPC = 1$ and setting ultra-low current consumption ($AMPHS1 = 1$). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }20\text{ MHz}$
 8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

($T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|-------------------------------|--|---|-------------------------------------|------|------|---------------|
| Low-speed on-chip oscillator operating current | I_{FIL} ^{Note 1} | | | | 0.20 | | μA |
| RTC operating current | I_{RTC} Notes 1, 2, 3 | | | | 0.02 | | μA |
| 12-bit interval timer operating current | I_{IT} Notes 1, 2, 4 | | | | 0.02 | | μA |
| Watchdog timer operating current | I_{WDT} Notes 1, 2, 5 | $f_{IL} = 15\text{ kHz}$ | | | 0.22 | | μA |
| A/D converter operating current | I_{ADC} Notes 1, 6 | When conversion at maximum speed | Normal mode, $AV_{REFP} = V_{DD} = 5.0\text{ V}$ | | 1.3 | 1.7 | mA |
| A/D converter reference voltage current | I_{ADREF} ^{Note 1} | | | | 75.0 | | μA |
| Temperature sensor operating current | I_{TMPS} ^{Note 1} | | | | 75.0 | | μA |
| LVD operating current | I_{LVD} Notes 1, 7 | | | | 0.08 | | μA |
| Self-programming operating current | I_{FSP} Notes 1, 8 | | | | 2.5 | 12.2 | mA |
| Programmable gain amplifier operating current | I_{PGA} ^{Note 9} | | | $AV_{REFP} = V_{DD} = 5.0\text{ V}$ | 0.21 | 0.37 | mA |
| | | | | $AV_{REFP} = V_{DD} = 3.0\text{ V}$ | 0.18 | 0.35 | mA |
| Comparator operating current | I_{CMP} ^{Note 10} | When one comparator channel is operating | | $AV_{REFP} = V_{DD} = 5.0\text{ V}$ | 41.4 | 74 | μA |
| | | | | $AV_{REFP} = V_{DD} = 3.0\text{ V}$ | 37.2 | 71 | μA |
| | I_{VREF} | When one internal reference voltage circuit is operating | | $AV_{REFP} = V_{DD} = 5.0\text{ V}$ | 14.8 | 31 | μA |
| | | | | $AV_{REFP} = V_{DD} = 3.0\text{ V}$ | 8.9 | 24 | μA |
| Programmable gain amplifier/comparator reference current source | I_{IREF} ^{Note 11} | | | $AV_{REFP} = V_{DD} = 5.0\text{ V}$ | 3.2 | 6.1 | μA |
| | | | | $AV_{REFP} = V_{DD} = 3.0\text{ V}$ | 2.9 | 4.9 | μA |
| BGO operating current | I_{BGO} ^{Note 12} | | | | 2.50 | 12.2 | mA |
| SNOOZE operating current | I_{SNOZ} ^{Note 1} | A/D converter operation | The mode is performed ^{Note 13} | | 0.50 | 1.10 | mA |
| | | | The A/D conversion operations are performed, Normal mode, $AV_{REFP} = V_{DD} = 5.0\text{ V}$ | | 1.20 | 2.17 | mA |
| | | CSI/UART operation | | | 0.70 | 1.27 | mA |

(Notes and Remarks are listed on the next page.)

- Notes**
1. Current flowing to the V_{DD} .
 2. When the high-speed on-chip oscillator and high-speed system clock are stopped.
 3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2} , and I_{RTC} , when the real-time clock is operating in operating mode or in HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.
 4. Current flowing only to the 12-bit interval timer (excluding the operating current of the XT1 oscillator and I_{FIL} operating current). The current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2} , and I_{IT} , when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.
 5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current value of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} , and I_{WDT} , when the watchdog timer is operating.
 6. Current flowing only to the A/D converter. The supply current value of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} , when the A/D converter is operating in operating mode or in HALT mode.
 7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.
 8. Current flowing during self-programming operation.
 9. Current flowing only to the programmable gain amplifier. The supply current value of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} , and I_{PGA} , when the programmable gain amplifier is operating in operating mode or in HALT mode.
 10. Current flowing only to the comparator. The supply current value of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} , and I_{CMP} , when the comparator is operating.
 11. This is the current required to flow to V_{DD} pin of the current circuit that is used as the programmable gain amplifier and the comparator.
 12. Current flowing only during data flash rewrite.
 13. See **21.3.3 SNOOZE mode in the RL78/I1A User's Manual** for shift time to the SNOOZE mode.

- Remarks**
1. f_{IL} : Low-speed on-chip oscillator clock frequency
 2. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 3. f_{CLK} : CPU/peripheral hardware clock frequency
 4. Temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$
 5. Example of calculating current value when using programmable gain amplifier and comparator.
Examples 1) TYP. operating current value when three comparator channels, one internal reference voltage generator, and PGA are operating (when $AV_{REFP} = V_{DD} = 5.0\text{ V}$)

$$\begin{aligned}
 & I_{CMP} \times 3 + I_{VREF} + I_{PGA} + I_{IREF} \\
 &= 41.4 [\mu\text{A}] \times 3 + 14.8 [\mu\text{A}] \times 1 + 210 [\mu\text{A}] + 3.2 [\mu\text{A}] \\
 &= 352.2 [\mu\text{A}]
 \end{aligned}$$

- Examples 2) TYP. operating current value when using two comparator channels, without using internal reference voltage generator (when $AV_{REFP} = V_{DD} = 5.0\text{ V}$)

$$\begin{aligned}
 & I_{CMP} \times 2 + I_{IREF} \\
 &= 41.4 [\mu\text{A}] \times 2 + 3.2 [\mu\text{A}] \\
 &= 86.0 [\mu\text{A}]
 \end{aligned}$$

3.4 AC Characteristics

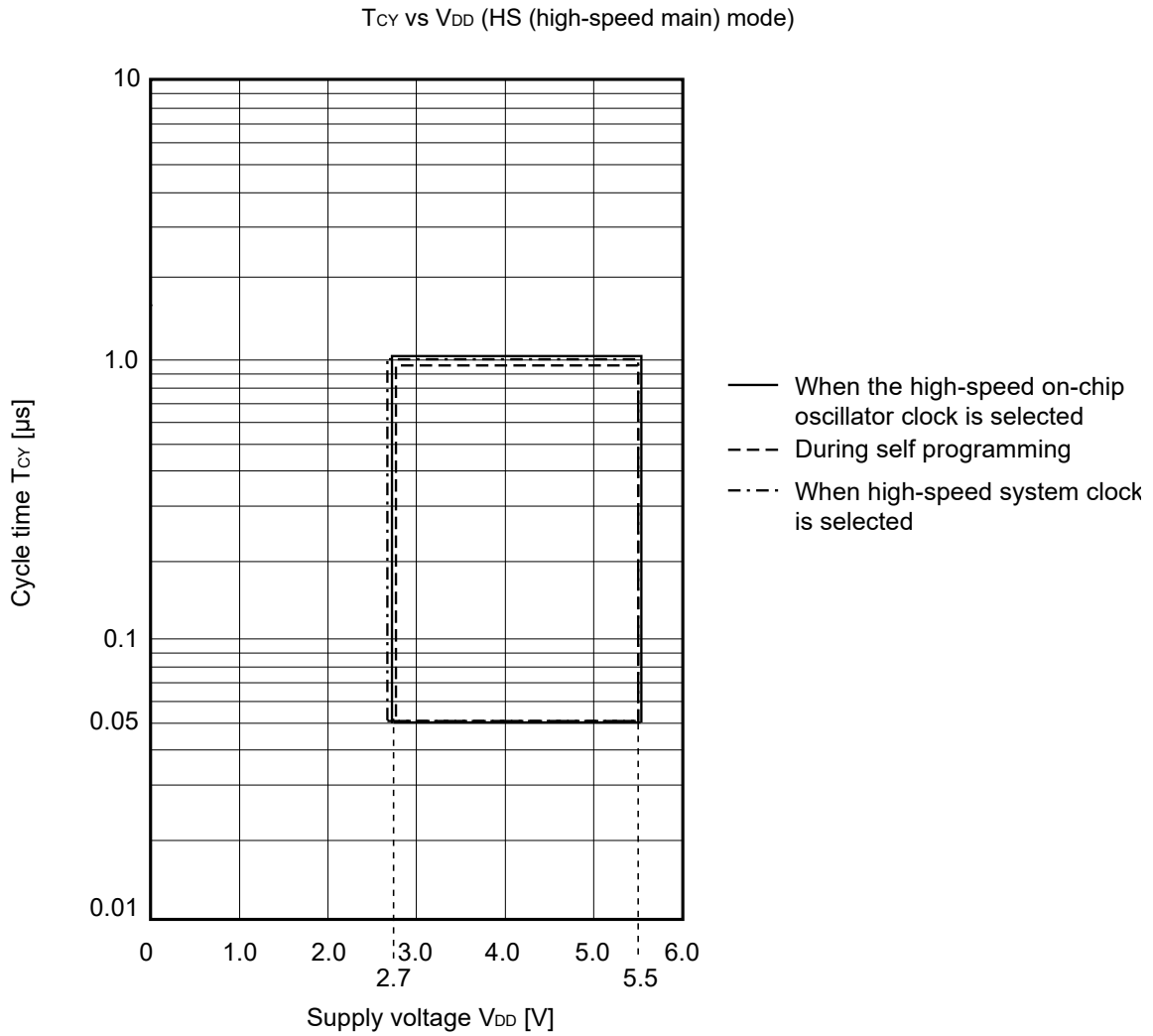
 $(T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|-------------------------|--|--|-------------------------------------|------|------|---------------|
| Instruction cycle (minimum instruction execution time) | T_{CY} | Main system clock (f_{MAIN}) operation | HS (high-speed main) mode | 0.05 | | 1 | μs |
| | | Subsystem clock (f_{SUB}) operation | | 28.5 | 30.5 | 31.3 | μs |
| | | In the self programming mode | HS (high-speed main) mode | $T_A = -40$ to $+105^\circ\text{C}$ | 0.05 | | 1 |
| External system clock frequency | f_{EX} | | | 1.0 | | 20.0 | MHz |
| | f_{EXS} | | | 32 | | 35 | kHz |
| External system clock input high-level width, low-level width | t_{EXH} , t_{EXL} | | | 24 | | | ns |
| | t_{EXHS} , t_{EXLS} | | | 13.7 | | | μs |
| TI03, TI05, TI06, TI07 input high-level width, low-level width | t_{TIH} , t_{TIL} | | | $2/f_{MCK}+10$ | | | ns |
| TO03, TO05, TO06, TKBO00, TKBO01, TKBO10, TKBO11, TKBO20, TKBO21, TKCO00 to TKCO05 output frequency (When duty = 50%) | f_{TO} | HS (high-speed main) mode | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | 5 | MHz |
| | | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ | | | 4 | MHz |
| Interrupt input high-level width, low-level width | t_{INTH} , t_{INTL} | INTP0, INTP3, INTP4, INTP9 to INTP11, INTP20 to INTP23 | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 1 | | | μs |
| RESET low-level width | t_{RSL} | | | 10 | | | μs |

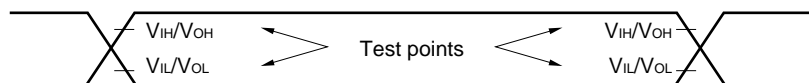
Remark f_{MCK} : Timer array unit operation clock frequency

(Operation clock to be set by the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

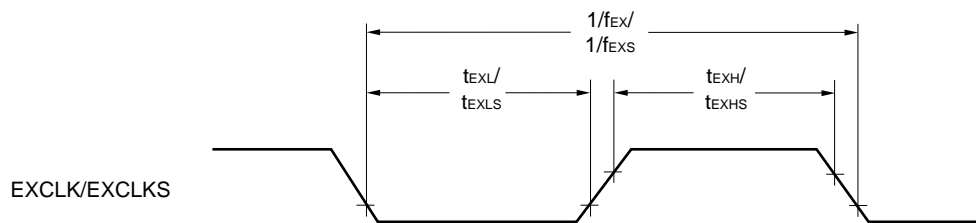
Minimum Instruction Execution Time during Main System Clock Operation



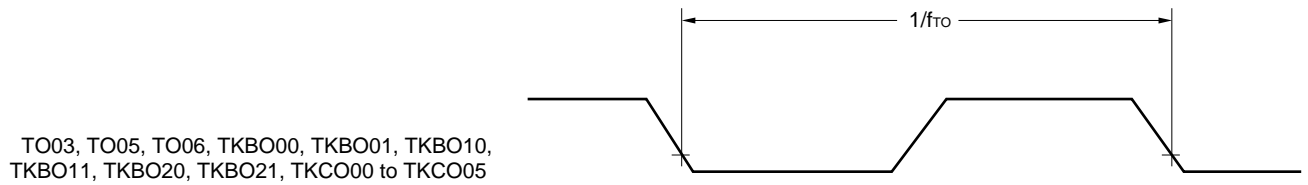
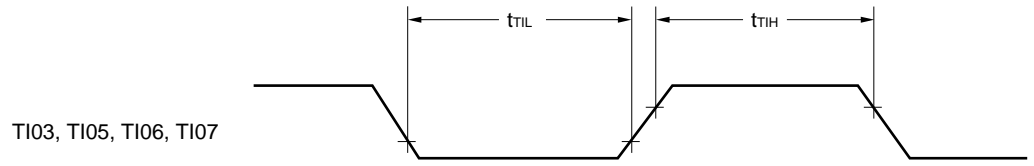
AC Timing Test Points



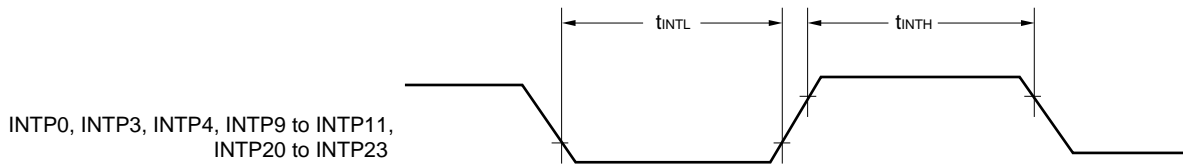
External System Clock Timing



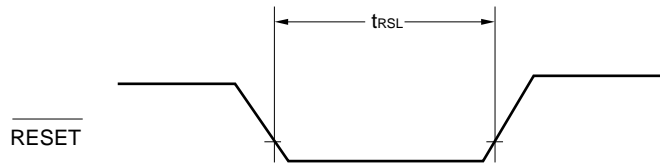
TI/TO Timing



Interrupt Request Input Timing

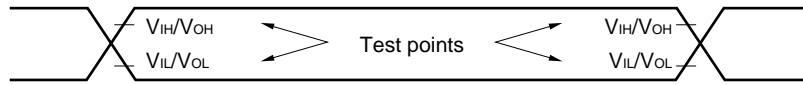


RESET Input Timing



3.5 Peripheral Functions Characteristics

AC Timing Test Points



3.5.1 Serial array unit 0, 4 (UART0, UART1, CSI00, DALI/UART4)

(1) During communication at same potential (UART mode)

(T_A = -40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

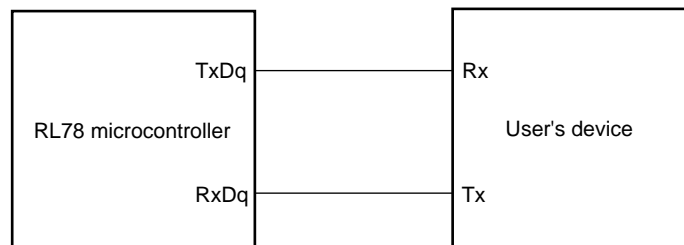
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---------------------------------|--------|---|---------------------------|-------------|------|
| | | | MIN. | MAX. | |
| Transfer rate ^{Note 1} | | Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ ^{Note 2} | | $f_{MCK}/6$ | bps |
| | | | | 3.3 | Mbps |

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

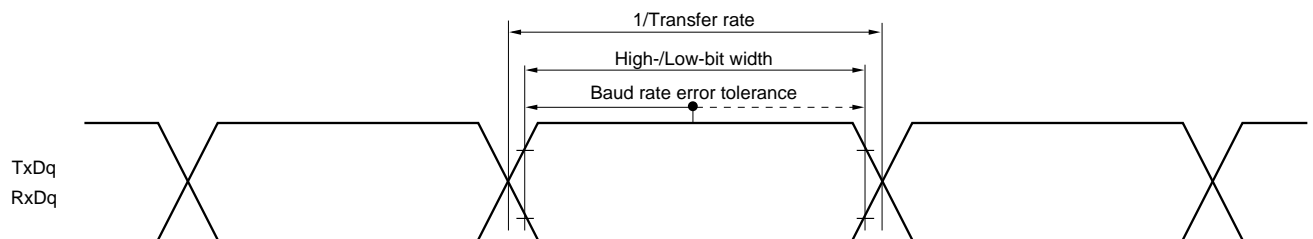
2. The operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

HS (high-speed main) mode: 20 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00 to 03))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**($T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit | |
|---|--------------------------|--|--|------|------|----|
| | | | MIN. | MAX. | | |
| SCKp cycle time | t_{KCY1} | $t_{KCY1} \geq 4/f_{CLK}$ | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 250 | | ns |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 500 | | ns |
| SCKp high-/low-level width | t_{KH1} , t_{KL1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | $t_{KCY1}/2 - 20$ | | | ns |
| | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | $t_{KCY1}/2 - 40$ | | | ns |
| Slp setup time (to SCKp \uparrow) ^{Note 1} | t_{SIK1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 80 | | | ns |
| | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 80 | | | ns |
| Slp hold time (from SCKp \uparrow) ^{Note 2} | t_{KSI1} | | 40 | | | ns |
| Delay time from SCKp \downarrow to SOp output ^{Note 3} | t_{KSO1} | $C = 30\text{ pF}$ ^{Note 4} | | 80 | | ns |

- Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp \downarrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp \downarrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp \uparrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM number (g = 1)
 2. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

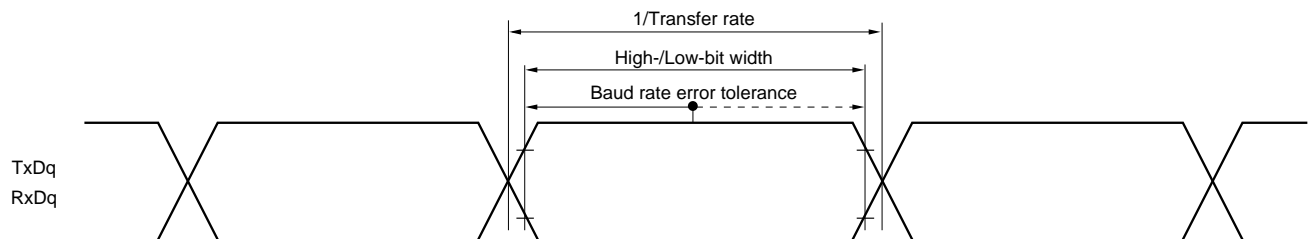
($T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|--------------------------|--|------------------------------|---------------------------|----------------|------|
| | | | | MIN. | MAX. | |
| SCKp cycle time ^{Note 5} | t_{KCY2} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | $f_{MCK} \leq 20\text{ MHz}$ | $6/f_{MCK}$ | | ns |
| | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | $16\text{ MHz} < f_{MCK}$ | $8/f_{MCK}$ | | ns |
| | | | $f_{MCK} \leq 16\text{ MHz}$ | $6/f_{MCK}$ | | ns |
| SCKp high-/low-level width | t_{KH2} , t_{KL2} | | | $t_{KCY2}/2$ | | ns |
| Slp setup time (to SCKp \uparrow) ^{Note 1} | t_{SIK2} | | | $1/f_{MCK}+40$ | | ns |
| Slp hold time (from SCKp \uparrow) ^{Note 2} | t_{KSI2} | | | $1/f_{MCK}+60$ | | ns |
| Delay time from SCKp \downarrow to SOP output ^{Note 3} | t_{KSO2} | $C = 30\text{ pF}$ ^{Note 4} | | | $2/f_{MCK}+80$ | ns |

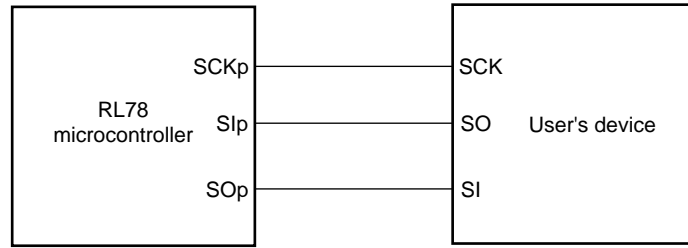
- Notes**
1. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The Slp setup time becomes “to SCKp \downarrow ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
 2. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The Slp hold time becomes “from SCKp \downarrow ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
 3. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The delay time to SOP output becomes “from SCKp \uparrow ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
 4. C is the load capacitance of the SOP output lines.
 5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOP pin by using port input mode register g (PIMg) and port output mode register g (POMg).

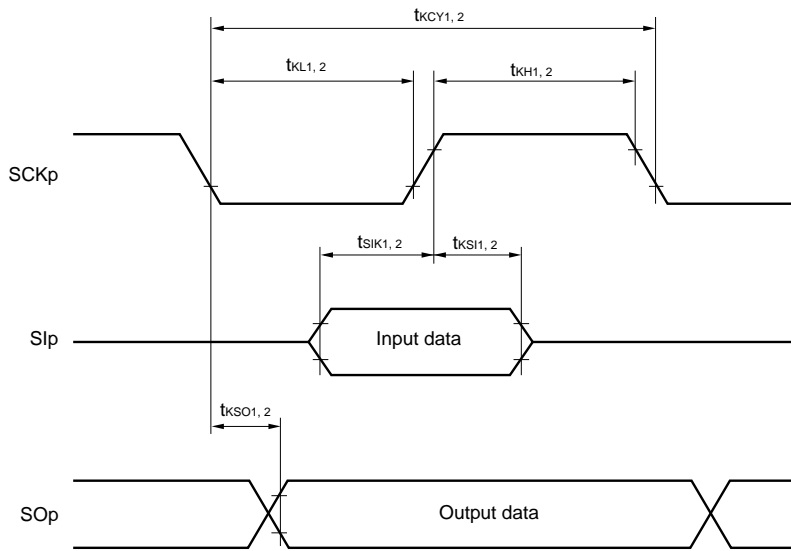
- Remarks**
1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM number (g = 1)
 2. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))



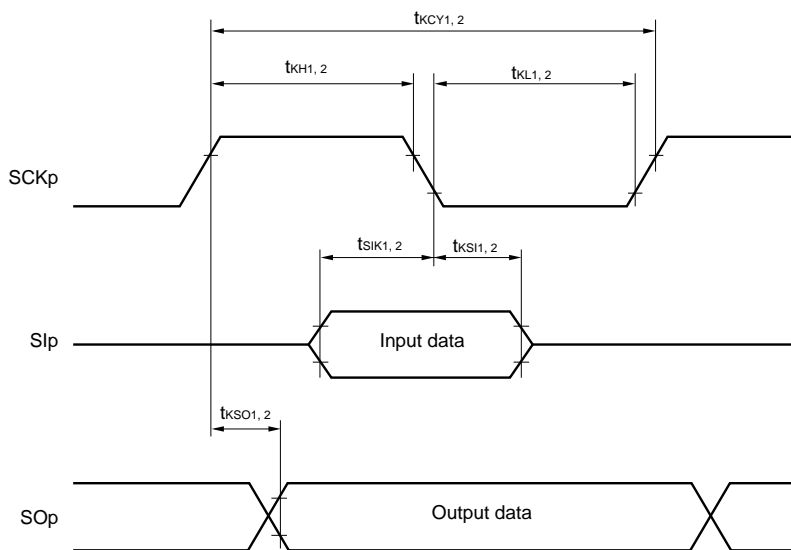
CSI mode connection diagram (during communication at same potential)



**CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



- Remarks 1. p: CSI number (p = 00)
- 2. m: Unit number, n: Channel number (mn = 00)

(4) Communication at different potential (2.5 V, 3 V) (UART mode) (1/2)**($T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---------------|--------|------------|---|--|-----------------------|------|
| | | | | MIN. | MAX. | |
| Transfer rate | | Reception | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ | | $f_{MCK}/6$ Note 1 | bps |
| | | | | Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 2 | | 3.3 |
| | | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ | | $f_{MCK}/6$ Note 1 | bps |
| | | | | Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 2 | | 3.3 |

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

HS (high-speed main) mode: 20 MHz ($2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. $V_b[V]$: Communication line voltage

2. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)

3. f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00 to 03)

(4) Communication at different potential (2.5 V, 3 V) (UART mode) (2/2)(T_A = -40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---------------|--------|--------------|--|---|---------------|-----------------------|
| | | | | MIN. | MAX. | |
| Transfer rate | | Transmission | 4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V | | Note 1 | bps |
| | | | | Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 1.4 kΩ, V _b = 2.7 V | | 2.8 ^{Note 2} |
| | | | 2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V | | Note 3 | bps |
| | | | | Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V | | 1.2 ^{Note 4} |

Notes 1. The smaller maximum transfer rate derived by using f_{mck}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the “Conditions” column are met. See **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using f_{mck}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

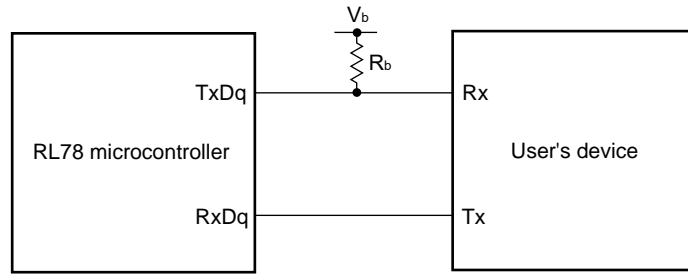
* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the “Conditions” column are met. See **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

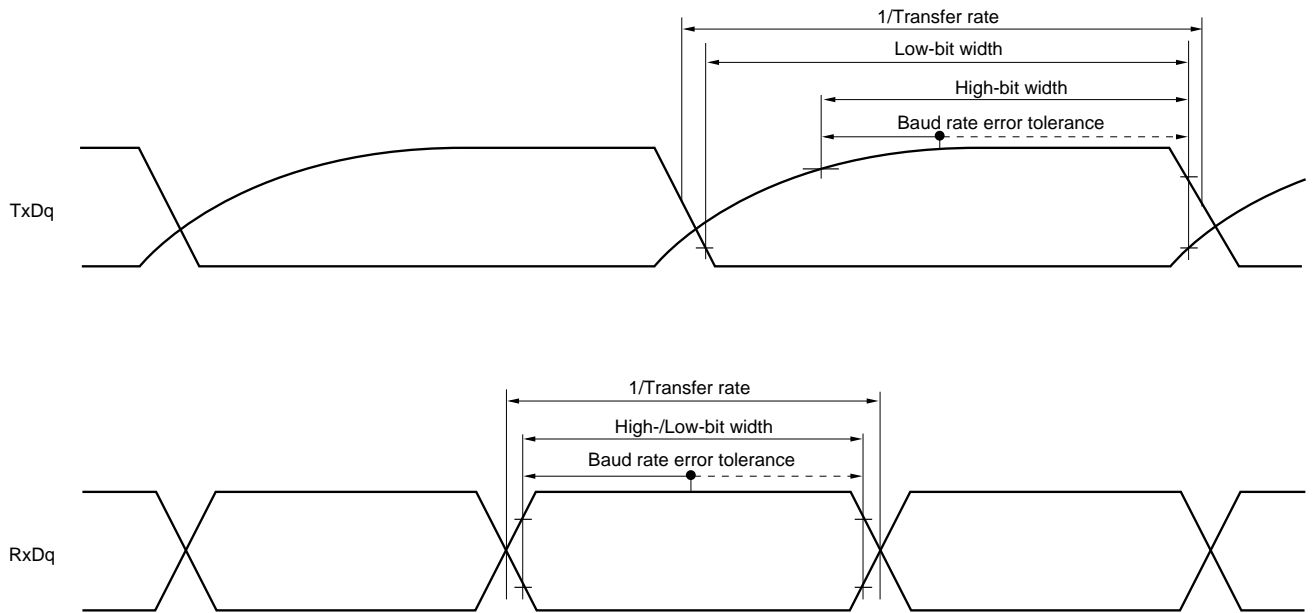
Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks 1.** R_b[Ω]: Communication line (TxDq) pull-up resistance,
C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage
- 2.** q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)
- 3.** f_{mck}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03))

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance, $V_b[V]$: Communication line voltage
 2. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)

(5) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)
($T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

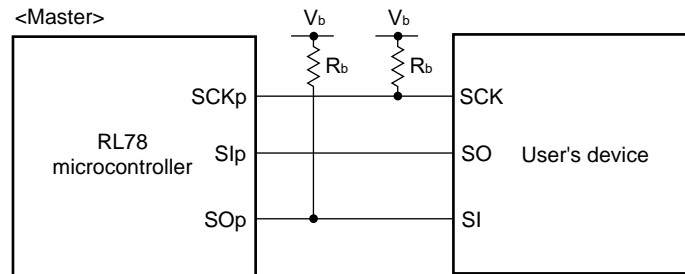
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|--|------------|--|---------------------------|------|------|
| | | | MIN. | MAX. | |
| SCKp cycle time | t_{KCY1} | $t_{KCY1} \geq 4/f_{CLK}$ $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | 600 | | ns |
| | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | 1000 | | ns |
| SCKp high-level width | t_{KH1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | $t_{KCY1}/2 - 80$ | | ns |
| | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | $t_{KCY1}/2 - 170$ | | ns |
| SCKp low-level width | t_{KL1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | $t_{KCY1}/2 - 28$ | | ns |
| | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | $t_{KCY1}/2 - 40$ | | ns |
| Slp setup time (to SCKp \uparrow) ^{Note 1} | t_{SIK1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | 160 | | ns |
| | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | 250 | | ns |
| Slp hold time (from SCKp \uparrow) ^{Note 1} | t_{SH1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | 40 | | ns |
| | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | 40 | | ns |
| Delay time from SCKp \downarrow to SOP output ^{Note 1} | t_{KSO1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | | 160 | ns |
| | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | | 250 | ns |
| Slp setup time (to SCKp \downarrow) ^{Note 2} | t_{SIK1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | 80 | | ns |
| | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | 80 | | ns |
| Slp hold time (from SCKp \downarrow) ^{Note 2} | t_{SH1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | 40 | | ns |
| | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | 40 | | ns |
| Delay time from SCKp \uparrow to SOP output ^{Note 2} | t_{KSO1} | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | | 80 | ns |
| | | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | | 80 | ns |

- Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
 2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

(Caution and Remarks are listed on the next page.)

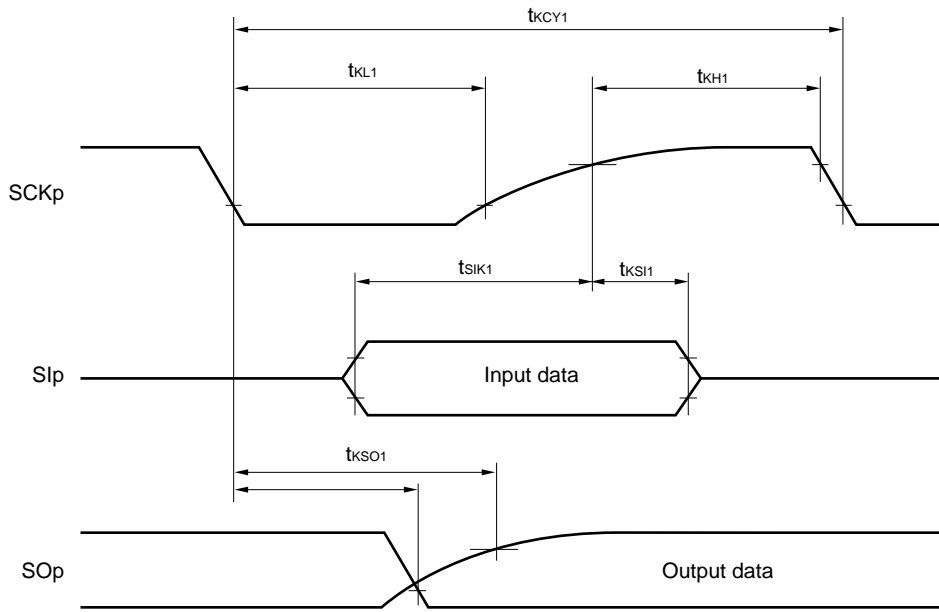
Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)

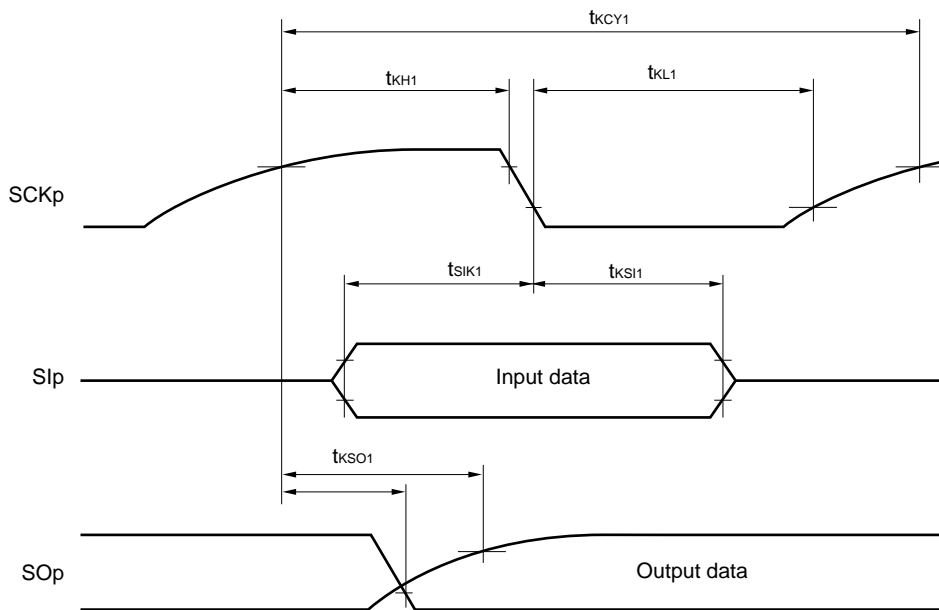


- Remarks**
- $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[\text{F}]$: Communication line (SCKp, SOp) load capacitance, $V_b[\text{V}]$: Communication line voltage
 - p: CSI number ($p = 00$), m: Unit number ($m = 0$), n: Channel number ($n = 0$), g: PIM and POM number ($g = 1$)

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

(6) DALI/UART4 mode**($T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---------------|--------|---|---------------------------|---------------------|------|
| | | | MIN. | MAX. | |
| Transfer rate | | Maximum transfer rate theoretical value $f_{\text{CLK}} = 20\text{ MHz}$, $f_{\text{MCK}} = f_{\text{CLK}}$ | | $f_{\text{MCK}}/12$ | bps |
| | | | | 1.6 | Mbps |

Remark f_{MCK} : Operation clock frequency of DALI/UART.

(Operation clock to be set by the serial clock select register 4 (SPS4).)

3.5.2 Serial interface IICA

(1) I²C standard mode(T_A = -40 to $+125^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---------------------|---|---------------------------|------|------|
| | | | MIN. | MAX. | |
| SCLA0 clock frequency | f _{SCL} | Standard mode: f _{CLK} ≥ 1 MHz | 0 | 100 | kHz |
| Setup time of restart condition | t _{SU:STA} | | 4.7 | | μs |
| Hold time ^{Note 1} | t _{HD:STA} | | 4.0 | | μs |
| Hold time when SCLA0 = "L" | t _{LOW} | | 4.7 | | μs |
| Hold time when SCLA0 = "H" | t _{HIGH} | | 4.0 | | μs |
| Data setup time (reception) | t _{SU:DAT} | | 250 | | ns |
| Data hold time (transmission) ^{Note 2} | t _{HD:DAT} | | 0 | 3.45 | μs |
| Setup time of stop condition | t _{SU:STO} | | 4.0 | | μs |
| Bus-free time | t _{BUF} | | 4.7 | | μs |

- Notes**
1. The first clock pulse is generated after this period when the start/restart condition is detected.
 2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(2) I²C fast mode

($T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

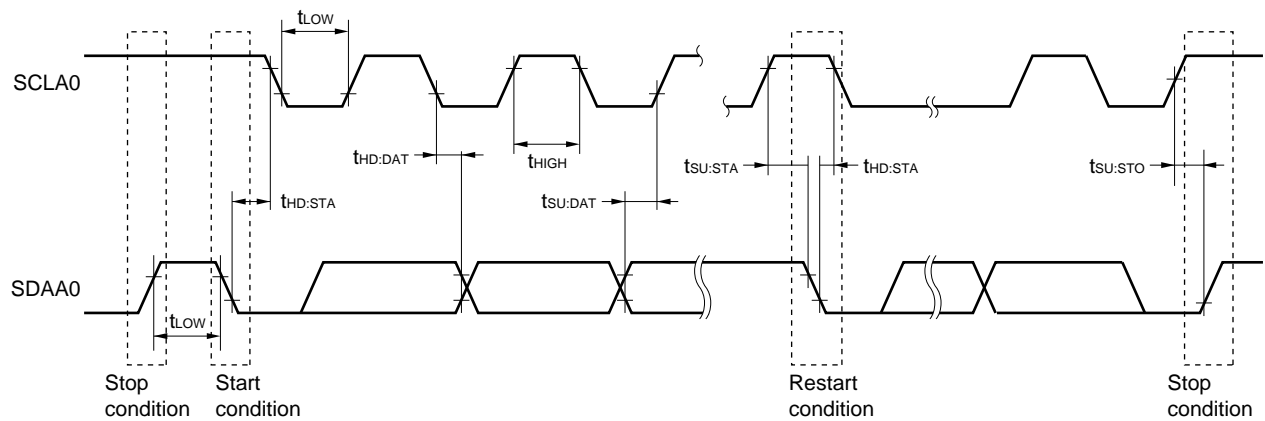
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|--------------|--|---------------------------|------|---------------|
| | | | MIN. | MAX. | |
| SCLA0 clock frequency | f_{SCL} | fast mode: $f_{CLK} \geq 3.5\text{ MHz}$ | 0 | 400 | kHz |
| Setup time of restart condition | $t_{SU:STA}$ | | 0.6 | | μs |
| Hold time ^{Note 1} | $t_{HD:STA}$ | | 0.6 | | μs |
| Hold time when SCLA0 = "L" | t_{LOW} | | 1.3 | | μs |
| Hold time when SCLA0 = "H" | t_{HIGH} | | 0.6 | | μs |
| Data setup time (reception) | $t_{SU:DAT}$ | | 100 | | ns |
| Data hold time (transmission) ^{Note 2} | $t_{HD:DAT}$ | | 0 | 0.9 | μs |
| Setup time of stop condition | $t_{SU:STO}$ | | 0.6 | | μs |
| Bus-free time | t_{BUF} | | 1.3 | | μs |

- Notes**
- The first clock pulse is generated after this period when the start/restart condition is detected.
 - The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

fast mode: $C_b = 320\text{ pF}$, $R_b = 1.1\text{ k}\Omega$

I²C serial transfer timing



3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

| Input channel | Reference Voltage | | |
|--|--|--|--|
| | Reference voltage (+) = AV_{REFP} Reference voltage (-) = AV_{REFM} | Reference voltage (+) = V_{DD} Reference voltage (-) = V_{SS} | Reference voltage (+) = V_{BGR} Reference voltage (-) = AV_{REFM} |
| ANI0 to ANI2, ANI4 to ANI7 | See 3.6.1 (1) . | See 3.6.1 (3) . | See 3.6.1 (4) . |
| ANI16 to ANI19 | See 3.6.1 (2) . | | |
| Internal reference voltage Temperature sensor output voltage | See 3.6.1 (1) . | | – |

(1) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target ANI pin: ANI2, ANI4 to ANI7, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|--|-----------------|--|--|-------|-------------|------|---------------|
| Resolution | RES | | 8 | | 10 | bit | |
| Overall error ^{Note 1} | AINL | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} | | 1.2 | ± 3.5 | LSB | |
| Conversion time | t_{CONV} | 10-bit resolution Target pin: ANI2, ANI4 to ANI7 | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.125 | | 39 | μs |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 3.4 | | 39 | μs |
| | | 10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.375 | | 39 | μs |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 3.8 | | 39 | μs |
| Zero-scale error ^{Notes 1, 2} | E _{ZS} | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} | | | ± 0.25 | %FSR | |
| Full-scale error ^{Notes 1, 2} | E _{FS} | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} | | | ± 0.25 | %FSR | |
| Integral linearity error ^{Note 1} | ILE | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} | | | ± 2.5 | LSB | |
| Differential linearity error ^{Note 1} | DLE | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} | | | ± 1.5 | LSB | |
| Analog input voltage | V_{AIN} | ANI2, ANI4 to ANI7 | 0 | | AV_{REFP} | V | |
| | | Internal reference voltage (HS (high-speed main) mode) | V_{BGR} ^{Note 4} | | | V | |
| | | Temperature sensor output voltage (HS (high-speed main) mode) | V_{TMPS25} ^{Note 4} | | | V | |

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

4. See 3.6.2 Temperature sensor/internal reference voltage characteristics.

(2) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin: ANI16 to ANI19

($T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|--|------------------|---|--|-------|------|-----------------------------|---------------|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error ^{Note 1} | AINL | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} | | | 1.2 | ± 5.0 | LSB |
| Conversion time | t_{CONV} | 10-bit resolution Target ANI pin : ANI16 to ANI19 | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.125 | | 39 | μs |
| | | | $2.7\text{ V} \leq V_{DD} < 5.5\text{ V}$ | 3.4 | | 39 | μs |
| Zero-scale error ^{Notes 1, 2} | E _{ZS} | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} | | | | ± 0.35 | %FSR |
| Full-scale error ^{Notes 1, 2} | E _{FS} | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} | | | | ± 0.35 | %FSR |
| Integral linearity error ^{Note 1} | ILE | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} | | | | ± 3.5 | LSB |
| Differential linearity error ^{Note 1} | DLE | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} | | | | ± 2.0 | LSB |
| Analog input voltage | V _{AIN} | ANI16 to ANI19 | | 0 | | AV_{REFP} and V_{DD} | V |

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 4.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.2\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/Differential linearity error: Add ± 2.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin: ANI0 to ANI2, ANI4 to ANI7, ANI16 to ANI19, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = V_{DD} , Reference voltage (-) = V_{SS})

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit | |
|---|------------|--|--|--------------------------------|------|------------|---------------|---|
| Resolution | RES | | | 8 | | 10 | bit | |
| Overall error ^{Note 1} | AINL | 10-bit resolution | | | 1.2 | ± 7.0 | LSB | |
| Conversion time | t_{CONV} | 10-bit resolution Target pin: ANI0 to ANI2, ANI4 to ANI7, ANI16 to ANI19 | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.125 | | 39 | μs | |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 3.4 | | 39 | μs | |
| Conversion time | t_{CONV} | 10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.375 | | 39 | μs | |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 3.8 | | 39 | μs | |
| Zero-scale error ^{Notes 1, 2} | E_{ZS} | 10-bit resolution | | | | ± 0.60 | %FSR | |
| Full-scale error ^{Notes 1, 2} | E_{FS} | 10-bit resolution | | | | ± 0.60 | %FSR | |
| Integral linearity error ^{Note 1} | ILE | 10-bit resolution | | | | ± 4.0 | LSB | |
| Differential linearity error ^{Note 1} | DLE | 10-bit resolution | | | | ± 2.0 | LSB | |
| Analog input voltage | V_{AIN} | ANI0 to ANI2, ANI4 to ANI7 | | 0 | | V_{DD} | V | |
| | | ANI16 to ANI19 | | 0 | | V_{DD} | V | |
| | | Internal reference voltage (HS (high-speed main) mode) | | V_{BGR} ^{Note 3} | | | | V |
| | | Temperature sensor output voltage (HS (high-speed main) mode) | | V_{TMPS25} ^{Note 3} | | | | V |

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. See 3.6.2 Temperature sensor/internal reference voltage characteristics.

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = $AV_{REFM}/ANI1$ (ADREFM = 1), target pin: ANI0, ANI2, ANI4 to ANI7, ANI16 to ANI19

($T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = $V_{BGR}^{\text{Note 3}}$, Reference voltage (-) = $AV_{REFM}^{\text{Note 4}} = 0\text{ V}$, HS (high-speed main) mode)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|-----------------|------------------|------|------|---------------------------|---------------|
| Resolution | RES | | 8 | | | bit |
| Conversion time | t_{CONV} | 8-bit resolution | 17 | | 39 | μs |
| Zero-scale error ^{Notes 1, 2} | E _{ZS} | 8-bit resolution | | | ± 0.60 | %FSR |
| Integral linearity error ^{Note 1} | ILE | 8-bit resolution | | | ± 2.0 | LSB |
| Differential linearity error ^{Note 1} | DLE | 8-bit resolution | | | ± 1.0 | LSB |
| Analog input voltage | V_{AIN} | | 0 | | $V_{BGR}^{\text{Note 3}}$ | V |

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. See 3.6.2 Temperature sensor/internal reference voltage characteristics.

4. When reference voltage (-) = V_{SS} , the MAX. values are as follows.

Zero-scale error: Add $\pm 0.35\%$ FSR to the MAX. value when reference voltage (-) = AV_{REFM} .

Integral linearity error: Add ± 0.5 LSB to the MAX. value when reference voltage (-) = AV_{REFM} .

Differential linearity error: Add ± 0.2 LSB to the MAX. value when reference voltage (-) = AV_{REFM} .

3.6.2 Temperature sensor/internal reference voltage characteristics

($T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, HS (high-speed main) mode)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------------------------|--------------|---|------|------|------|---------------|
| Temperature sensor output voltage | V_{TMPS25} | Setting ADS register = 80H, $T_A = +25^\circ\text{C}$ | | 1.05 | | V |
| Internal reference voltage | V_{BGR} | Setting ADS register = 81H | 1.38 | 1.45 | 1.5 | V |
| Temperature coefficient | F_{VTMPS} | Temperature sensor that depends on the temperature | | -3.6 | | mV/C |
| Operation stabilization wait time | t_{AMP} | | 5 | | | μs |

3.6.3 Programmable gain amplifier

 $(T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq AV_{\text{REFP}} = V_{\text{DD}} \leq 5.5\text{ V}$, $V_{\text{SS}} = AV_{\text{REFM}} = 0\text{ V}$)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|--------------------|--|---|------------------------|---------|--------------------------------|------------------------|
| Input offset voltage | V_{IOPGA} | | | | ± 5 | ± 10 | mV |
| Input voltage range | V_{IPGA} | | | 0 | | $0.9V_{\text{DD}}/\text{gain}$ | V |
| Gain error ^{Note 1} | | 4, 8 times | | | | ± 1 | % |
| | | 16 times | | | | ± 1.5 | % |
| | | 32 times | | | | ± 2 | % |
| Slew rate ^{Note 1} | SR_{RPGA} | Rising edge | $4.0\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ | 4, 8 times | 4 | | $\text{V}/\mu\text{s}$ |
| | | | | 16, 32 times | 1.4 | | $\text{V}/\mu\text{s}$ |
| | | $2.7\text{ V} \leq V_{\text{DD}} < 4.0\text{ V}$ | 4, 8 times | 1.8 | | $\text{V}/\mu\text{s}$ | |
| | | | 16, 32 times | 0.5 | | $\text{V}/\mu\text{s}$ | |
| | SR_{FPGA} | Falling edge | $4.0\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ | 4, 8 times | 3.2 | | $\text{V}/\mu\text{s}$ |
| | | | | 16, 32 times | 1.4 | | $\text{V}/\mu\text{s}$ |
| $2.7\text{ V} \leq V_{\text{DD}} < 4.0\text{ V}$ | 4, 8 times | 1.2 | | $\text{V}/\mu\text{s}$ | | | |
| | 16, 32 times | 0.5 | | $\text{V}/\mu\text{s}$ | | | |
| Operation stabilization wait time ^{Note 2} | t_{PGA} | 4, 8 times | | 5 | | | μs |
| | | 16, 32 times | | 10 | | | μs |

Notes 1. When $V_{\text{IPGA}} = 0.1V_{\text{DD}}/\text{gain}$ to $0.9V_{\text{DD}}/\text{gain}$.

2. Time required until a state is entered where the DC and AC specifications of the PGA are satisfied after the PGA operation has been enabled ($\text{PGAEN} = 1$).

Remark These characteristics apply when AV_{REFM} is selected as GND of the PGA by using the CVRVS1 bit.

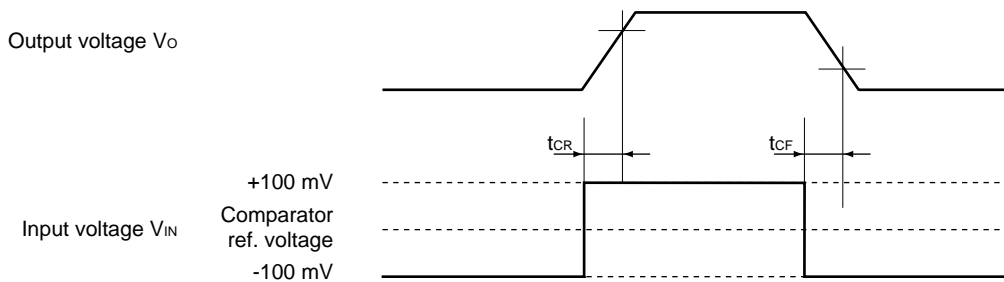
3.6.4 Comparator

($T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$, $V_{SS} = AV_{REFM} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---------------------|---|-------|---------|-------------|---------------|
| Input offset voltage | V_{IOCOMP} | | | ± 5 | ± 40 | mV |
| Input voltage range | V_{ICMP} | CMP0P to CMP5P | 0 | | V_{DD} | V |
| | | CMPCOM | 0.045 | | $0.9V_{DD}$ | V |
| Internal reference voltage deviation | ΔV_{IREF} | CmRVM register values: 7FH to 80H ($m = 0$ to 2) | | | ± 2 | LSB |
| | | Other than above | | | ± 1 | LSB |
| Response time | t_{CR} , t_{CF} | Input amplitude = $\pm 100\text{ mV}$ | | 70 | 150 | ns |
| Operation stabilization wait time ^{Note 1} | t_{CMP} | $3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 1 | | | μs |
| | | $2.7\text{ V} \leq V_{DD} < 3.3\text{ V}$ | 3 | | | μs |
| Reference voltage stabilization wait time | t_{VR} | CVRE: 0 to 1 ^{Note 2} | 10 | | | μs |

- Notes**
- Time required until a state is entered where the DC and AC specifications of the comparator are satisfied after the operation of the comparator has been enabled (CMPnEN bit = 1; $n = 0$ to 5)
 - Enable comparator output (CnOE bit = 1; $n = 0$ to 5) after enabling operation of the internal reference voltage generator (by setting the CVREm bit to 1; $m = 0$ to 2) and waiting for the operation stabilization time to elapse.

Remark These characteristics apply when AV_{REFP} is selected as the power supply source of the internal reference voltage by using the CVRVS0 bit, and when AV_{REFM} is selected as GND of the internal reference voltage by using the CVRVS1 bit.

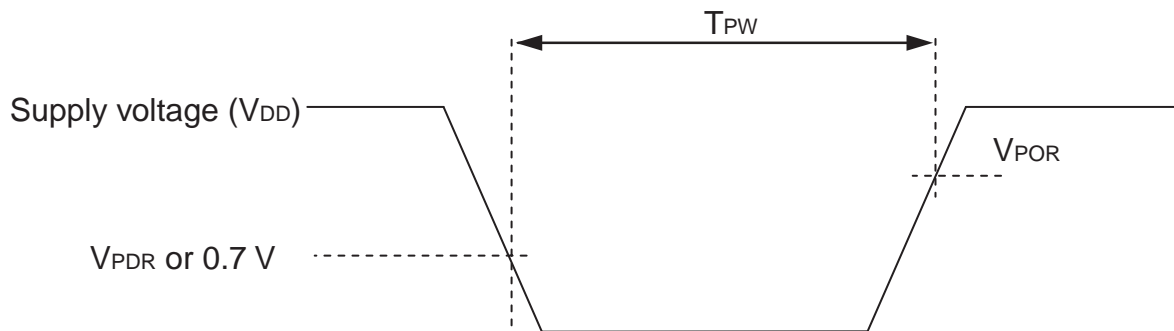


3.6.5 POR circuit characteristics

($T_A = -40$ to $+125^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------------------|-----------|------------------------|------|------|------|---------------|
| Detection voltage | V_{POR} | Power supply rise time | 1.45 | 1.51 | 1.62 | V |
| | V_{PDR} | Power supply fall time | 1.44 | 1.50 | 1.61 | V |
| Minimum pulse width ^{Note} | T_{PW} | | 300 | | | μs |

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR} . This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HISTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



3.6.6 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

($T_A = -40$ to $+125^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|-------------------|----------------------|------------------------|------|------|------|------|---------------|
| Detection voltage | V_{LVD0} | Power supply rise time | 3.97 | 4.06 | 4.25 | V | |
| | | Power supply fall time | 3.89 | 3.98 | 4.15 | V | |
| | V_{LVD1} | Power supply rise time | 3.67 | 3.75 | 3.93 | V | |
| | | Power supply fall time | 3.59 | 3.67 | 3.83 | V | |
| | V_{LVD2} | Power supply rise time | 3.06 | 3.13 | 3.28 | V | |
| | | Power supply fall time | 2.99 | 3.06 | 3.20 | V | |
| | V_{LVD3} | Power supply rise time | 2.95 | 3.02 | 3.17 | V | |
| | | Power supply fall time | 2.89 | 2.96 | 3.09 | V | |
| | V_{LVD4} | Power supply rise time | 2.85 | 2.92 | 3.07 | V | |
| | | Power supply fall time | 2.79 | 2.86 | 2.99 | V | |
| | V_{LVD5} | Power supply rise time | 2.75 | 2.81 | 2.95 | V | |
| | | Power supply fall time | 2.70 | 2.75 | 2.88 | V | |
| | Minimum pulse width | t_{LW} | | 300 | | | μs |
| | Detection delay time | | | | | 300 | μs |

LVD Detection Voltage of Interrupt & Reset Mode

($T_A = -40$ to $+125^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5$ V, $V_{SS} = 0$ V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|---------------------------|-------------------|---|------------------------------|------|------|------|---|
| Interrupt and reset mode | V _{LVD0} | $V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1$, falling reset voltage: 2.7 V | 2.70 | 2.75 | 2.88 | V | |
| | V _{LVD1} | LVIS1, LVIS0 = 1, 0 | Rising release reset voltage | 2.85 | 2.92 | 3.07 | V |
| | | | Falling interrupt voltage | 2.79 | 2.86 | 2.99 | V |
| | V _{LVD2} | LVIS1, LVIS0 = 0, 1 | Rising release reset voltage | 2.95 | 3.02 | 3.17 | V |
| | | | Falling interrupt voltage | 2.89 | 2.96 | 3.09 | V |
| | V _{LVD3} | LVIS1, LVIS0 = 0, 0 | Rising release reset voltage | 3.97 | 4.06 | 4.25 | V |
| Falling interrupt voltage | | | 3.89 | 3.98 | 4.15 | V | |

3.6.7 Supply voltage rise inclination characteristics

($T_A = -40$ to $+125^\circ\text{C}$, $V_{SS} = 0$ V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---------------------|------------------|------------|------|------|------|------|
| Supply voltage rise | S _{VDD} | | | | 54 | V/ms |

Caution Keep the internal reset status by using the LVD circuit or an external reset signal until V_{DD} rises to within the operating voltage range shown in 33.4 AC Characteristics.

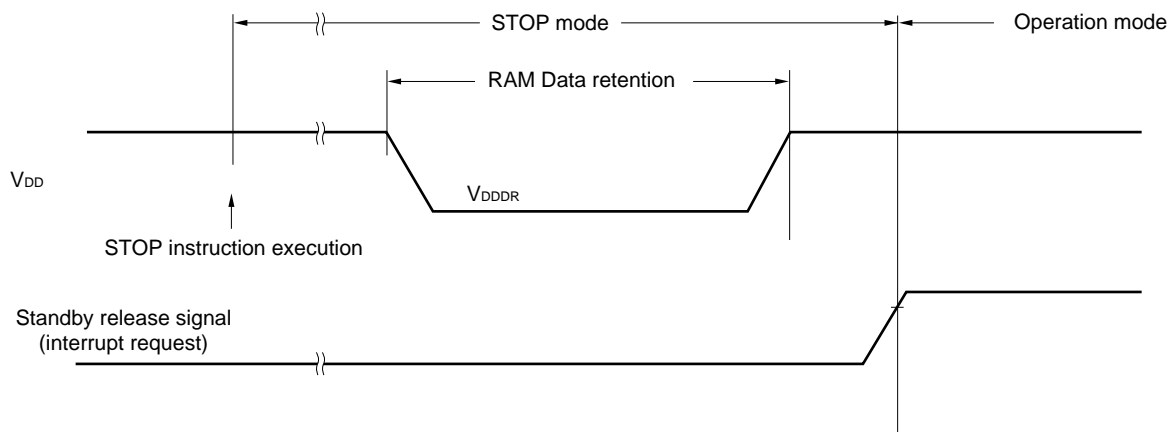
3.7 RAM Data Retention Characteristics

($T_A = -40$ to $+125^\circ\text{C}$, $V_{SS} = 0$ V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|-------------------|------------|------------------------|------|------|------|
| Data retention supply voltage ^{Note 2} | V _{DDDR} | | 1.47 ^{Note 1} | | 5.5 | V |

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.

Caution When CPU is operated at the voltage of out of the operation voltage range, RAM data is not retained. Therefore, set STOP mode before the supplied voltage is below the operation voltage range.



3.8 Flash Memory Programming Characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|------------|--|---------|-----------|------|-------|
| CPU/peripheral hardware clock frequency | f_{CLK} | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 1 | | 32 | MHz |
| Number of code flash rewrites ^{Notes 1, 2, 3} | C_{erwr} | Retained for 20 years, $T_A = 85^\circ\text{C}$ ^{Note 3, 4} | 1,000 | | | Times |
| Number of data flash rewrites ^{Notes 1, 2, 3} | | Retained for 1 year, $T_A = 25^\circ\text{C}$ ^{Note 3, 4} | | 1,000,000 | | |
| | | Retained for 5 years, $T_A = 85^\circ\text{C}$ ^{Note 3, 4} | 100,000 | | | |
| | | Retained for 20 years, $T_A = 85^\circ\text{C}$ ^{Note 3, 4} | 10,000 | | | |

- Notes**
- 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
 2. When using flash memory programmer and Renesas Electronics self programming library
 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.
 4. These are the average temperature of during the retainment.

3.9 Dedicated Flash Memory Programmer Communication (UART)

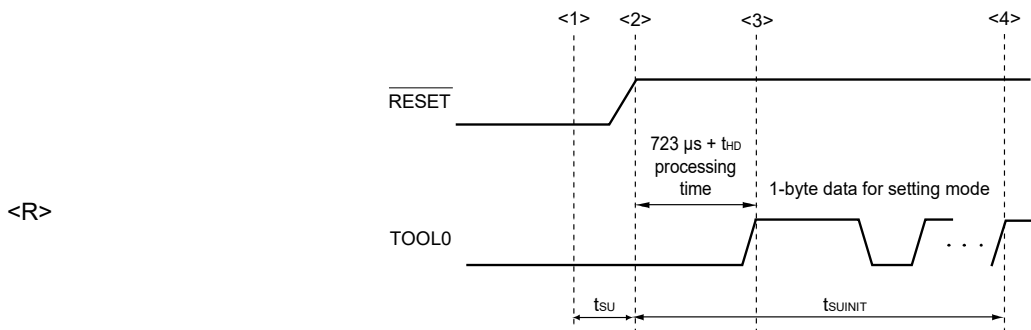
($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---------------|--------|---------------------------|---------|------|------|------|
| Transfer rate | | During serial programming | 115.2 k | | 1 M | bps |

3.10 Timing of Entry to Flash Memory Programming Modes

($T_A = -40$ to $+125^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|----------------------|--|------|------|------|---------------|
| How long from when an external reset ends until the initial communication settings are specified | t_{SUIINIT} | POR and LVD reset must end before the external reset ends. | | | 100 | ms |
| How long from when the TOOL0 pin is placed at the low level until an external reset ends | t_{SU} | POR and LVD reset must end before the external reset ends. | 10 | | | μs |
| How long the TOOL0 pin must be kept at the low level after a reset ends (except soft processing time) | t_{HD} | POR and LVD reset must end before the external reset ends. | 1 | | | ms |



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset ends (POR and LVD reset must end before the pin reset ends.).
- <3> The TOOL0 pin is set to the high level.
- <4> Complete the baud rate setting by UART reception.

Remark t_{SUIINIT} : The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

t_{SU} : How long from when the TOOL0 pin is placed at the low level until an external reset ends

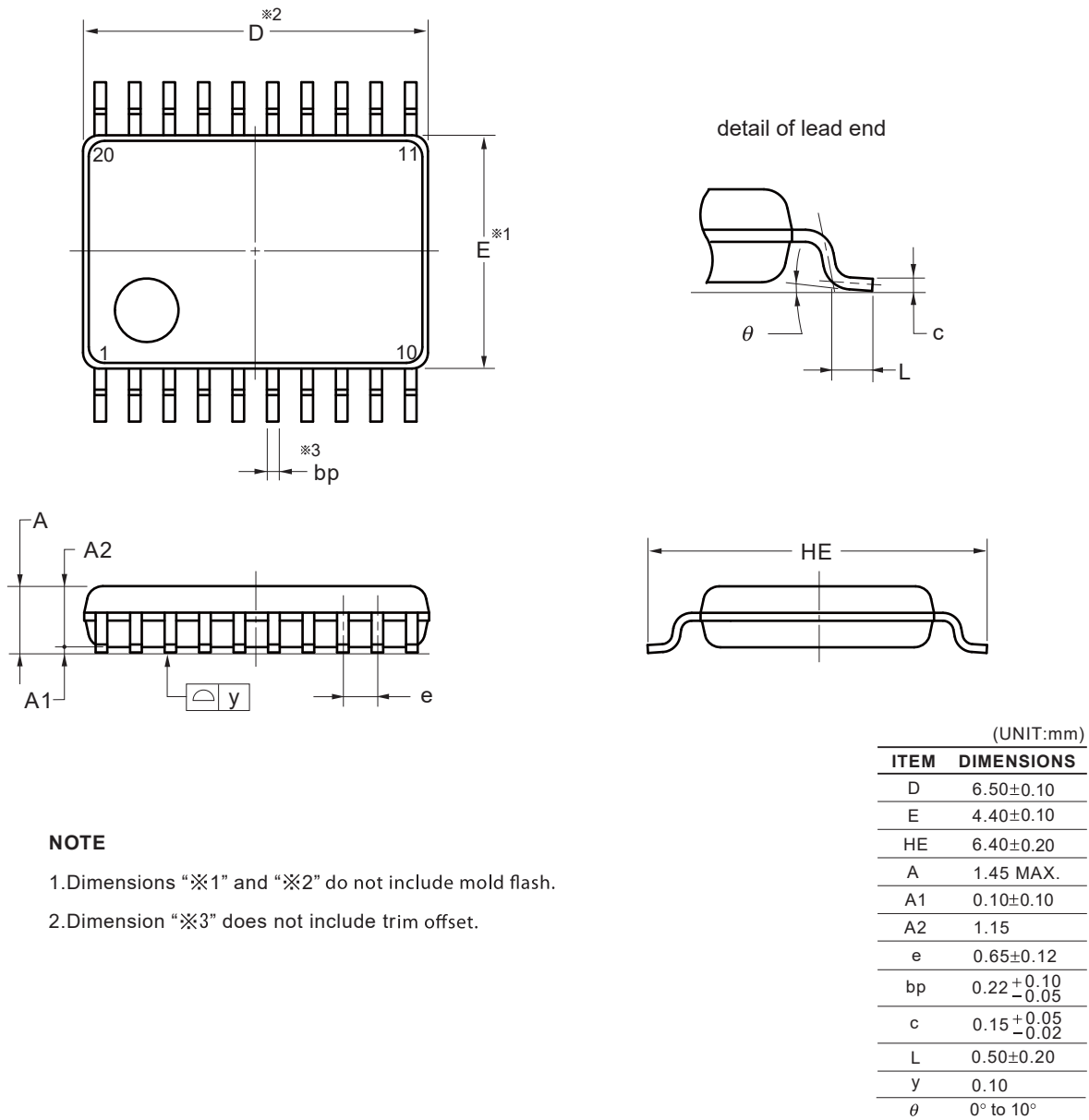
t_{HD} : How long to keep the TOOL0 pin at the low level from when the external and internal resets end (except soft processing time)

4. PACKAGE DRAWINGS

<R> 4.1 20-pin Products

R5F1076CGSP#V0, R5F1076CGSP#X0, R5F1076CMSP#V0, R5F1076CMSP#X0

| | | | |
|------------------------|--------------|----------------|-----------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
| P-LSSOP20-4.4x6.5-0.65 | PLSP0020JB-A | P20MA-65-NAA-1 | 0.1 |



NOTE

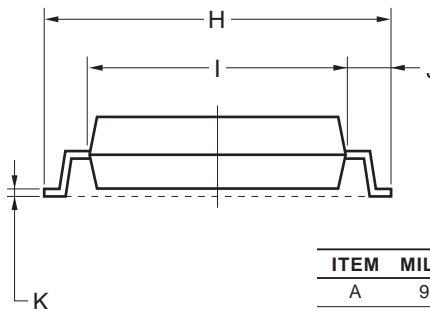
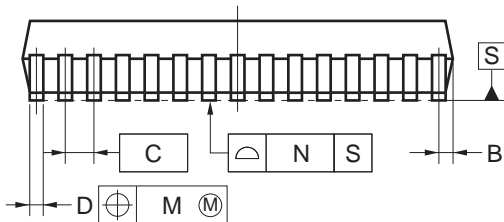
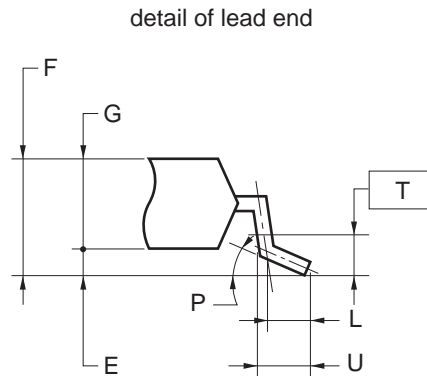
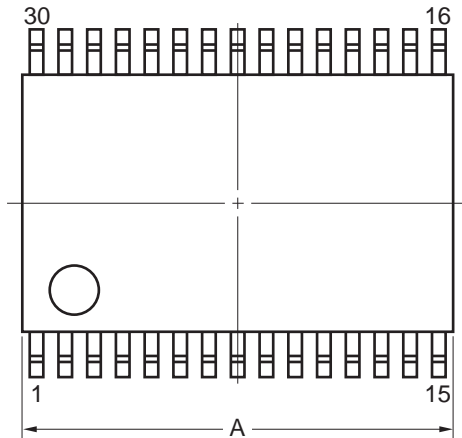
- 1. Dimensions "※1" and "※2" do not include mold flash.
- 2. Dimension "※3" does not include trim offset.

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4.2 30-pin Products

R5F107ACGSP#V0, R5F107AEGSP#V0, R5F107ACGSP#X0, R5F107AEGSP#X0, R5F107ACMSP#V0, R5F107AEMSP#V0, R5F107ACMSP#X0, R5F107AEMSP#X0

| | | | |
|---------------------|--------------|----------------|-----------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
| P-LSSOP30-0300-0.65 | PLSP0030JB-B | S30MC-65-5A4-3 | 0.18 |



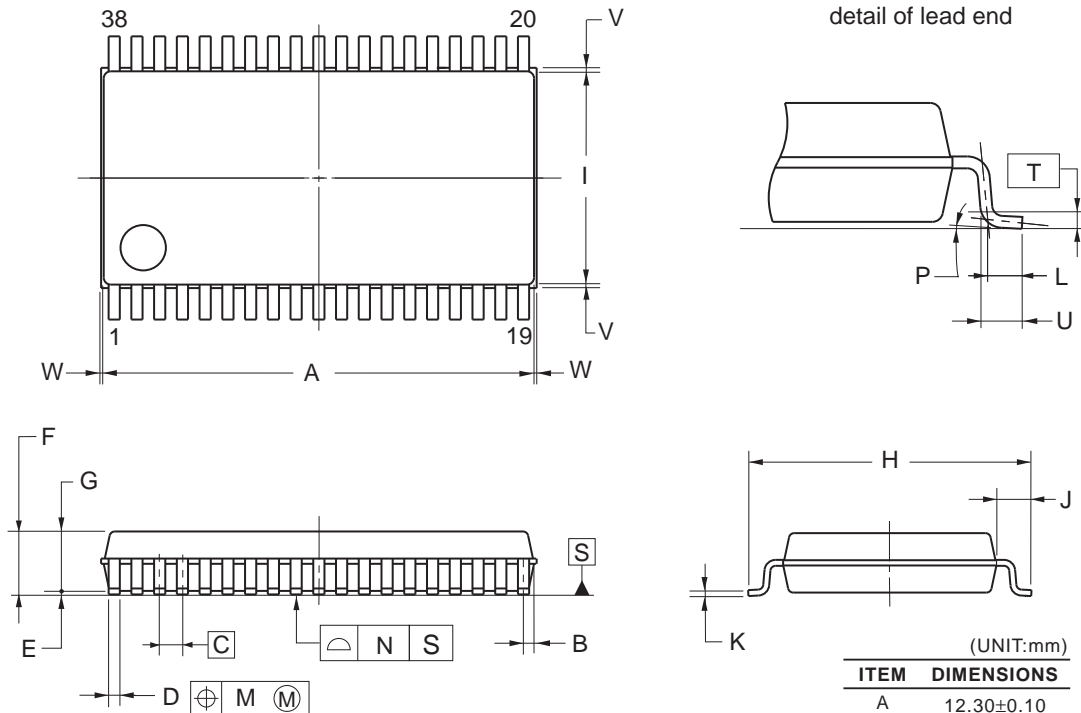
NOTE
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|------|--|
| A | 9.85±0.15 |
| B | 0.45 MAX. |
| C | 0.65 (T.P.) |
| D | 0.24 ^{+0.08} _{-0.07} |
| E | 0.1±0.05 |
| F | 1.3±0.1 |
| G | 1.2 |
| H | 8.1±0.2 |
| I | 6.1±0.2 |
| J | 1.0±0.2 |
| K | 0.17±0.03 |
| L | 0.5 |
| M | 0.13 |
| N | 0.10 |
| P | 3° ^{+5°} _{-3°} |
| T | 0.25 |
| U | 0.6±0.15 |

4.3 38-pin Products

R5F107DEGSP#V0, R5F107DEGSP#X0, R5F107DEMSP#V0, R5F107DEMSP#X0

| | | | |
|--------------------|--------------|----------------|-----------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
| P-SSOP38-0300-0.65 | PRSP0038JA-A | P38MC-65-2A4-2 | 0.3 |



NOTE
 Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

(UNIT:mm)

| ITEM | DIMENSIONS |
|------|--|
| A | 12.30±0.10 |
| B | 0.30 |
| C | 0.65 (T.P.) |
| D | 0.32 ^{+0.08} _{-0.07} |
| E | 0.125±0.075 |
| F | 2.00 MAX. |
| G | 1.70±0.10 |
| H | 8.10±0.20 |
| I | 6.10±0.10 |
| J | 1.00±0.20 |
| K | 0.17 ^{+0.08} _{-0.07} |
| L | 0.50 |
| M | 0.10 |
| N | 0.10 |
| P | 3° ^{+7°} _{-3°} |
| T | 0.25(T.P.) |
| U | 0.60±0.15 |
| V | 0.25 MAX. |
| W | 0.15 MAX. |

| | |
|-------------------------|---------------------------|
| Revision History | RL78/I1A Datasheet |
|-------------------------|---------------------------|

| Rev. | Date | Description | |
|------|--------------|-------------|--|
| | | Page | Summary |
| 3.20 | Sep 29, 2017 | p.1 | Modification of description in 1.1 Features |
| | | p.59 | Modification of figure in 2.10 Timing of Entry to Flash Memory Programming Modes |
| | | p.102 | Modification of figure in 3.10 Timing of Entry to Flash Memory Programming Modes |
| | | p.103 | Modification of figure in 4.1 20-pin Products |

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NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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