



## Revision History

Document No.	Release Date	Change Description
201DSR03	9/29/20	■ Initial release.

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## Specifications

### Absolute Maximum Ratings

**Important:** Stress above what is listed in [Table 1](#) may cause permanent damage to the device. This is a stress rating only—functional operation of the device above what is listed in [Table 1](#) or any other conditions beyond what MaxLinear recommends is not implied. Exposure to conditions above what is listed in [Table 3](#) for extended periods of time may affect device reliability. Solder reflow profile is specified in the IPC/JEDEC J-STD-020C standard.

**Table 1: Absolute Maximum Ratings**

Parameter	Minimum	Maximum	Units
$V_{IN}$	-0.3	18	V
$V_{SW1}, V_{SW2}$	-1	25	V
PGOOD1, PGOOD2, COMP1, COMP2	-0.3	6	V
INTV <sub>CC</sub> , EXTV <sub>CC</sub>	-0.3	6	V
MODE/PLLIN, f <sub>SET</sub> , TRACK1, TRACK2	-0.3	INTV <sub>CC</sub>	V
DIFFOUT	-0.3	INTV <sub>CC</sub> - 1.1V	V
PHASMD	-0.3	INTV <sub>CC</sub>	V
$V_{OUT1}, V_{OUT2}, V_{OUTS1}, V_{OUTS2}$	-0.3	6	V
DIFFP, DIFFN	-0.3	INTV <sub>CC</sub>	V
RUN1, RUN2, V <sub>FB1</sub> , V <sub>FB2</sub>	-0.3	INTV <sub>CC</sub>	V
INTV <sub>CC</sub> Peak Output Current		100	mA
Storage Temperature Range	-65	150	°C
Peak Package Body Temperature		245	°C

### ESD Ratings

**Table 2: ESD Ratings**

Parameter	Limit	Units
HBM (Human Body Model)	2k	V
CDM (Charged Device Model)	500	V



## Operating Conditions

**Table 3: Operating Conditions**

Parameter	Minimum	Maximum	Units
$V_{IN}$	4.5	15	V
$INTV_{CC}$	4.5	5.5	V
$EXTV_{CC}$	4.7	5.5	V
PGOOD	0	5.5	V
Switching Frequency	400	780	kHz
Junction Temperature Range ( $T_J$ )	-40	125	°C
Thermal Resistance from Junction to Ambient ( $\Theta_{JA}$ )		7	°C/W
Thermal Resistance from Junction to PCB ( $\Theta_{JB}$ )		1.5	°C/W
Thermal Resistance from Junction to Top of Module Case ( $\Theta_{Jctop}$ )		3.86	°C/W

## Electrical Characteristics

Specifications are for Operating Junction Temperature of  $T_J = 25^\circ\text{C}$  only; limits applying over the full Operating Junction Temperature range are denoted by a "•". Typical values represent the most likely parametric norm at  $T_J = 25^\circ\text{C}$  and are provided for reference purposes only. Unless otherwise indicated,  $V_{IN} = 12\text{V}$  and  $V_{RUN1}$ ,  $V_{RUN2} = 5\text{V}$ . Per [Figure 18](#) and [Figure 19](#).

**Table 4: Electrical Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
DC Specifications							
$V_{IN(DC)}$	Input DC voltage		• 4.5		15	V	
$V_{OUT1(RANGE)}$ $V_{OUT2(RANGE)}$	Output DC range	$V_{IN} = 4.5\text{V to }15\text{V}$	• 0.6		1.8	V	
$V_{OUT1(DC)}$ $V_{OUT2(DC)}$	$V_{OUT}$ total variation with line and load	$C_{IN} = 22\ \mu\text{F} \times 3$ $C_{OUT} = 100\ \mu\text{F} \times 2$ Ceramic, $470\ \mu\text{F}$ POSCAP, MODE_PLLIN = GND $V_{IN} = 12\text{V}$ , $V_{OUT} = 1.2\text{V}$ , $I_{OUT} = 0\text{A to }25\text{A}$	• 1.182	1.2	1.218	V	
Input Specifications							
$V_{RUN1}$ , $V_{RUN2}$	RUN pin on/off threshold	RUN rising		1.10	1.25	1.40	V
$V_{RUN1HYS}$ , $V_{RUN2HYS}$	RUN pin ON hysteresis				168	mV	
$I_{INRUSH(VIN)}$	Input inrush current at start-up	$I_{OUT} = 0\text{A}$ , $C_{IN} = 3 \times 22\ \mu\text{F}$ , $C_{SS} = 0.01\ \mu\text{F}$ , $C_{OUT} = 3 \times 100\ \mu\text{F}$ , $V_{OUT1} = 1.5\text{V}$ , $V_{OUT2} = 1.5\text{V}$ , $V_{IN} = 12\text{V}$			1	A	
$I_{Q(VIN)}$	Input supply bias current	$V_{IN} = 12\text{V}$ , $V_{OUT1} = V_{OUT2} = 1.2\text{V}$ , pulse-skipping mode			4.95	mA	
		$V_{IN} = 12\text{V}$ , $V_{OUT1} = V_{OUT2} = 1.2\text{V}$ , 500kHz CCM			160	mA	
		Shutdown, RUN = 0, $V_{IN} = 12\text{V}$			56	$\mu\text{A}$	
$I_{S(VIN)}$	Input supply current	$V_{IN} = 4.5\text{V}$ , $V_{OUT} = 1.2\text{V}$ , $I_{OUT} = 25\text{A}$			7.9	A	
		$V_{IN} = 12\text{V}$ , $V_{OUT} = 1.2\text{V}$ , $I_{OUT} = 25\text{A}$			2.9	A	
Output Specifications							
$I_{OUT1(DC)}$ , $I_{OUT2(DC)}$	Output continuous current range <sup>(1)</sup>	$V_{IN} = 12\text{V}$ , $V_{OUT} = 1.2\text{V}$		0	25	A	
$\Delta V_{OUT1(LINE)}/V_{OUT1}$ $\Delta V_{OUT2(LINE)}/V_{OUT2}$	Line regulation accuracy	$V_{OUT} = 1.2\text{V}$ , $V_{IN}$ from $4.5\text{V to }15\text{V}$ $I_{OUT} = 0\text{A}$ for each output	•		0.01	0.1	%/V
$\Delta V_{OUT1(LOAD)}/V_{OUT1}$ $\Delta V_{OUT2(LOAD)}/V_{OUT2}$	Load regulation accuracy <sup>(1)</sup>	Each output; $V_{OUT} = 1.2\text{V}$ , $0\text{A to }25\text{A}$ , $V_{IN} = 12\text{V}$	•		0.5	0.75	%
$V_{OUT1(AC)}$ , $V_{OUT2(AC)}$	Output ripple voltage	For each output; $I_{OUT} = 0\text{A}$ , $C_{OUT} = 100\ \mu\text{F} \times 3$ / X7R / ceramic, $470\ \mu\text{F}$ POSCAP, $V_{IN} = 12\text{V}$ , $V_{OUT} = 1.2\text{V}$ , frequency = $500\text{kHz}$			22		mV <sub>PP</sub>
$f_S$ (each channel)	Output ripple voltage frequency <sup>(2)</sup>	$V_{IN} = 12\text{V}$ , $V_{OUT} = 1.2\text{V}$ , $f_{SET} = 1.2\text{V}$			500		kHz

**Table 4: Electrical Characteristics (Continued)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
$f_{\text{SYNC}}$ (each channel)	SYNC capture range		400		780	kHz	
$\Delta V_{\text{OUT1START}}$ $\Delta V_{\text{OUT2START}}$	Turn-on overshoot	$C_{\text{OUT}} = 100\mu\text{F} / \text{X5R} / \text{ceramic}, 470\mu\text{F}$ POSCAP, $V_{\text{OUT}} = 1.2\text{V}$ , $I_{\text{OUT}} = 0\text{A}$ , $V_{\text{IN}} = 12\text{V}$ Each channel		0		mV	
$t_{\text{START1}}, t_{\text{START2}}$	Turn-on time	$C_{\text{OUT}} = 100\mu\text{F} / \text{X5R} / \text{ceramic},$ $470\mu\text{F}$ POSCAP, No load, TRACK/SS with $0.01\mu\text{F}$ to GND, $V_{\text{IN}} = 12\text{V}$ Each channel		5		ms	
$\Delta V_{\text{OUT(LS)}}$ (Each channel)	Peak deviation for dynamic load	Load: 0% to 50% to 0% of full load, $C_{\text{OUT}} = 22\mu\text{F} \times 3$ Ceramic, $470\mu\text{F}$ POSCAP $V_{\text{IN}} = 12\text{V}$ , $V_{\text{OUT}} = 1.5\text{V}$		30		mV	
$t_{\text{SETTLE}}$ (Each channel)	Settling time for dynamic load step	Load: 0% to 50% to 0% of full load, $V_{\text{IN}} = 12\text{V}$ , $C_{\text{OUT}} = 100\mu\text{F}$ , $470\mu\text{F}$ POSCAP		20		$\mu\text{s}$	
$I_{\text{OUT1(PK)}}$ $I_{\text{OUT2(PK)}}$	Output current limit	$V_{\text{IN}} = 12\text{V}$ , $V_{\text{OUT}} = 1.2\text{V}$ Each channel		35		A	
<b>Control Section</b>							
$V_{\text{FB1}}, V_{\text{FB2}}$	Voltage at $V_{\text{FB}}$ pins	$I_{\text{OUT}} = 0\text{A}$ , $V_{\text{OUT}} = 1.2\text{V}$	•	0.594	0.600	0.606	V
$I_{\text{FB}}$	Current at $V_{\text{FB}}$ pins			-5	-20		nA
$V_{\text{OVL}}$	Feedback overvoltage lockout		•	0.64	0.66	0.68	V
TRACK1 (I), TRACK2 (I)	Track pin soft-start pull-up current	TRACK1 (I), TRACK2 (I) start at 0V		1	1.25	1.5	$\mu\text{A}$
UVLO	Undervoltage lockout	$V_{\text{IN}}$ falling			3.6		V
		$V_{\text{IN}}$ rising			4.2		V
UVLO hysteresis					0.6		V
$t_{\text{ON(MIN)}}$	Minimum on-time				90		ns
$R_{\text{FBHI1}}, R_{\text{FBHI2}}$	Resistance between $V_{\text{OUTS1}}, V_{\text{OUTS2}}$ and $V_{\text{FB1}}, V_{\text{FB2}}$	Each output		60.05	60.4	60.75	k $\Omega$
$V_{\text{PGOOD1 LOW}},$ $V_{\text{PGOOD2 LOW}}$	PGOOD voltage low	$I_{\text{PGOOD}} = 2\text{mA}$			34	300	mV
$I_{\text{PGOOD}}$	PGOOD leakage current	$V_{\text{PGOOD}} = 5\text{V}$				5	$\mu\text{A}$
$V_{\text{PGOOD}}$	PGOOD trip level	$V_{\text{FB}}$ with respect to its steady state value $V_{\text{FB}}$ ramping negative			-10		%
		$V_{\text{FB}}$ with respect to its steady state value $V_{\text{FB}}$ ramping positive			10		

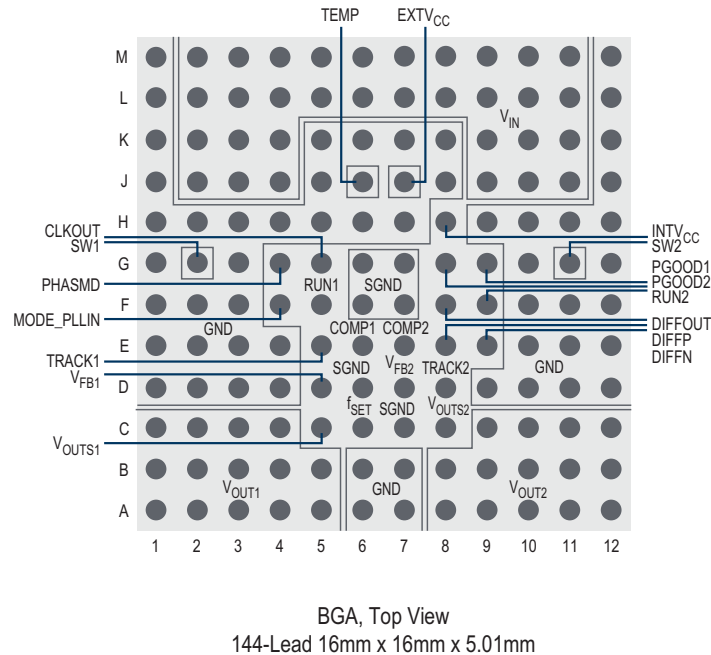
**Table 4: Electrical Characteristics (Continued)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INTV <sub>CC</sub> Linear Regulator						
V <sub>INTVCC</sub>	Internal V <sub>CC</sub> voltage	6V < V <sub>IN</sub> < 15V	4.8	5.0	5.2	V
V <sub>INTVCC</sub> load regulation	INTV <sub>CC</sub> load regulation	I <sub>CC</sub> = 0mA to 50mA		1.05	2.00	%
V <sub>EXTVCC</sub>	EXTV <sub>CC</sub> switchover voltage	EXTV <sub>CC</sub> ramping positive	4.5	4.7		V
V <sub>EXTVCC(DROP)</sub>	EXTV <sub>CC</sub> dropout	I <sub>CC</sub> = 20mA, V <sub>EXTVCC</sub> = 5V		50	100	mV
V <sub>EXTVCC(HYST)</sub>	EXTV <sub>CC</sub> hysteresis			150		mV
Oscillator and Phase-Locked Loop						
Frequency nominal	Nominal frequency	f <sub>SET</sub> = 1.2V	450	500	550	kHz
Frequency low	Lowest frequency	f <sub>SET</sub> = 0.93V		400		kHz
Frequency high	Highest frequency	f <sub>SET</sub> > 2.4V, up to INTV <sub>CC</sub>		780		kHz
I <sub>FSET</sub>	Frequency set current		9	10	11	μA
R <sub>MODE_PLLIN</sub>	MODE_PLLIN input resistance			250		kΩ
CLKOUT	Phase (relative to SW1)	PHASMD = GND		60		Deg
		PHASMD = float		90		Deg
		PHASMD = INTV <sub>CC</sub>		120		Deg
CLK high	Clock High output voltage		2			V
CLK low	Clock Low output voltage				0.2	V
Differential Amplifier						
A <sub>V</sub>	Gain			1		V/V
R <sub>IN</sub>	Input resistance	Measured at DIFFP Input		82		kΩ
V <sub>OS</sub>	Input offset voltage	V <sub>DIFFP</sub> = V <sub>DIFFOUT</sub> = 1.5V, I <sub>DIFFOUT</sub> = 100μA			3	mV
PSRR	Power Supply Rejection Ratio	5V < V <sub>IN</sub> < 15V		90		dB
I <sub>CL</sub>	Maximum Output current			3		mA
V <sub>DIFFOUT(MAX)</sub>	Maximum output voltage	I <sub>DIFFOUT</sub> = 300μA	INTV <sub>CC</sub> - 1.4			V
GBW	Gain Bandwidth Product			2.7		MHz
V <sub>TEMP</sub>	Diode Connected PNP	I = 100μA		0.6		V
TC <sub>VTEMP</sub>	Temperature Coefficient	I = 25μA	•	-2.1		mV/°C
OT	Thermal shutdown threshold	Rising temperature		145		°C
	Thermal hysteresis			15		°C

1. See output current derating curves for different V<sub>IN</sub>, V<sub>OUT</sub> and T<sub>A</sub>.
2. The MxL7225 module is designed to operate from 400kHz to 780kHz.

## Pin Information

### Pin Configuration



**Figure 3: Pin Configuration**

### Pin Description

**Table 5: Pin Description**

Pin Number	Pin Name	Description
A1, A2, A3, A4, A5, B1, B2, B3, B4, B5, C1, C2, C3, C4	V <sub>OUT1</sub>	Output of the channel 1 power stage. Connect the corresponding output load from the V <sub>OUT1</sub> pins to the PGND pins. Direct output decoupling capacitance from V <sub>OUT1</sub> to PGND is recommended.
A6, A7, B6, B7, D1, D2, D3, D4, D9, D10, D11, D12, E1, E2, E3, E4, E10, E11, E12, F1, F2, F3, F10, F11, F12, G1, G3, G10, G12, H1, H2, H3, H4, H5, H6, H7, H9, H10, H11, H12, J1, J5, J8, J12, K1, K5, K6, K7, K8, K12, L1, L12, M1, M12	GND	Ground for the power stage. Connect to the application's power ground plane.
A8, A9, A10, A11, A12, B8, B9, B10, B11, B12, C9, C10, C11, C12	V <sub>OUT2</sub>	Output of the channel 2 power stage. Connect the corresponding output load from the V <sub>OUT2</sub> pins to the PGND pins. Direct output decoupling capacitance from V <sub>OUT2</sub> to PGND is recommended.

**Table 5: Pin Description (Continued)**

Pin Number	Pin Name	Description
C5, C8	V <sub>OUTS1</sub> , V <sub>OUTS2</sub>	These pins are connected internally to the top of the feedback resistor for each output. Connect this pin directly to its specific output or to DIFFOUT when using the remote sense amplifier. When paralleling modules, connect one of the V <sub>OUTS</sub> pins to DIFFOUT when remote sensing or directly to V <sub>OUT</sub> when not remote sensing. These pins must be connected to either DIFFOUT or V <sub>OUT</sub> . This connection provides the feedback path and cannot be left open.
C6	f <sub>SET</sub>	This pin is used to set the operating frequency via one of two methods: <ul style="list-style-type: none"> <li>■ Connect a resistor from this pin to ground</li> <li>■ Drive this pin with a DC voltage</li> </ul> This pin sources a 10μA current. See <a href="#">Figure 24</a> for frequency of operation vs. f <sub>SET</sub> voltage.
C7, D6, G6, G7, F6, F7	SGND	Ground pin for all analog signals and low power circuits. Connect to GND in one place. See layout guidelines in <a href="#">Figure 36</a> .
D5, D7	V <sub>FB1</sub> , V <sub>FB2</sub>	Feedback input to the negative side of the error amplifier for each channel. These pins are each internally connected to V <sub>OUTS1</sub> and V <sub>OUTS2</sub> via a precision 60.4kΩ resistor. Vary each output voltage by adding a feedback resistor from V <sub>FB</sub> to SGND. Tie V <sub>FB1</sub> and V <sub>FB2</sub> together for parallel operation.
E5, D8	TRACK1, TRACK2	Soft-Start and Output Voltage Tracking pins. Each channel has a 1.25μA pull-up current source. When one channel is configured as a master, adding a capacitor from this pin to ground sets a soft-start ramp rate. The other channel can be set up as the slave and have the master output applied through a voltage divider to the slave's output TRACK pin. For coincidental tracking, this voltage divider is equal to the slave's output feedback divider.
E6, E7	COMP1, COMP2	Current control threshold and error amplifier compensation point for each channel. The current comparator threshold increases with this control voltage. The MxL7225 is internally compensated, however a feed-forward C <sub>FF</sub> is frequently required. R <sub>C</sub> and C <sub>C</sub> are required for MxL7225-1 (not MxL7225). Refer to <a href="#">Figure 18</a> , <a href="#">Table 7</a> and <a href="#">Stability and Compensation</a> in the Applications Information section. When paralleling both channels, connect the COMP1 and COMP2 pins together.
E8	DIFFP	This pin is the remote sense amplifier's positive input and is connected to the output voltage's remote sense point. If the remote sense amplifier is not used, connect this pin to SGND.
E9	DIFFN	This pin is the remote sense amplifier's negative input and is connected to the remote sense point GND. If the remote sense amplifier is not used, connect this pin to SGND.
F4	MODE_PLLIN	Selects between Forced Continuous Mode or Pulse-Skipping Mode, or connects to an external clock for frequency synchronization. There are three connection options: <ol style="list-style-type: none"> <li>1. Connect this pin to SGND to force both channels into Forced Continuous Mode.</li> <li>2. Connect this pin to INTV<sub>CC</sub> or leave it floating to enable Pulse-Skipping Mode.</li> <li>3. Connect this pin to an external clock. Both channels will be synchronized to the clock and operate in Forced Continuous Mode.</li> </ol>
F5, F9	RUN1, RUN2	The RUN1 and RUN2 pins each enable and disable their corresponding channel. A voltage above 1.27V on the RUN pin will turn on the corresponding channel. The RUN pin has a hysteresis of about 170mV. There are two supported methods to drive the RUN pin. Either drive it with a logic signal or connect it to a voltage divider whose upper resistor is connected to V <sub>IN</sub> and lower resistor to ground. See <a href="#">Applications Information</a> for important details.
F8	DIFFOUT	Output of the internal remote sense amplifier. If remote sensing on channel 1, connect to V <sub>OUTS1</sub> . If remote sensing on channel 2, connect to V <sub>OUTS2</sub> . When paralleling modules, connect one of the V <sub>OUTS</sub> pins to DIFFOUT when remote sensing.
G2, G11	SW1, SW2	Use these pins to access the switching node of each channel. An RC snubber can be connected to reduce switch node ringing. Otherwise, leave these pins floating.

**Table 5: Pin Description (Continued)**

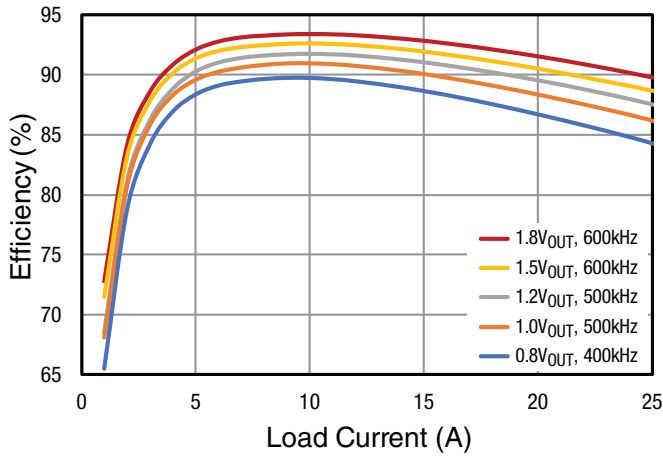
Pin Number	Pin Name	Description
G4	PHASMD	This pin selects the CLKOUT phase as follows: <ul style="list-style-type: none"> <li>■ Connect to SGND for 60 degrees</li> <li>■ Connect to INTV<sub>CC</sub> for 120 degrees</li> <li>■ Leave floating for 90 degrees</li> </ul>
G5	CLKOUT	This is the clock output. Its phase is set with the PHASMD pin. It is used to synchronize multiple modules so that all channels evenly share load current and operate in a multiphase manner. Refer to the Application Section on <b>Multiphase Operation</b> for more details.
G9, G8	PGOOD1, PGOOD2	Power Good outputs. This open-drain output is pulled low when the V <sub>OUT</sub> of its respective channel is more than ±10% outside regulation.
H8	INTV <sub>CC</sub>	Internal 5V Regulator Output. This voltage powers the control circuits and internal gate driver. Decouple to GND with a 4.7µF ceramic capacitor. INTV <sub>CC</sub> is activated when either RUN1 or RUN2 is activated.
J6	TEMP	The internal temperature sensing diode monitors the temperature change with voltage change on V <sub>BE</sub> . Connect to V <sub>IN</sub> through a resistor (R <sub>TEMP</sub> ) to limit the current to 100µA. $R_{TEMP} = (V_{IN} - 0.6V) / 100\mu A$
J7	EXTV <sub>CC</sub>	External power input that is connected through an internal switch to INTV <sub>CC</sub> whenever EXTV <sub>CC</sub> is > 4.7V. Do not exceed 6V on this input. Connect this pin to V <sub>IN</sub> when operating V <sub>IN</sub> on 5V. An efficiency increase that is a function of (V <sub>IN</sub> - INTV <sub>CC</sub> ) multiplied by the power MOSFET driver current occurs when the feature is used. V <sub>IN</sub> must be applied before EXTV <sub>CC</sub> , and EXTV <sub>CC</sub> must be removed before V <sub>IN</sub> .
M2, M3, M4, M5, M6, M7, M8, M9, M10, M11, L2, L3, L4, L5, L6, L7, L8, L9, L10, L11, J2, J3, J4, J9, J10, J11, K2, K3, K4, K9, K10, K11	V <sub>IN</sub>	Power input pins. Connect input voltage between these pins and GND. Direct input decoupling capacitance from V <sub>IN</sub> to GND is recommended.

1. Use test points to monitor signal pin connections.

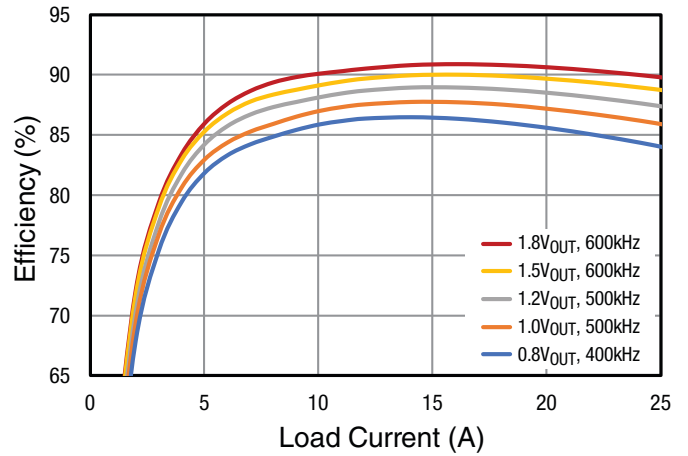
# Typical Performance Characteristics

## Efficiency

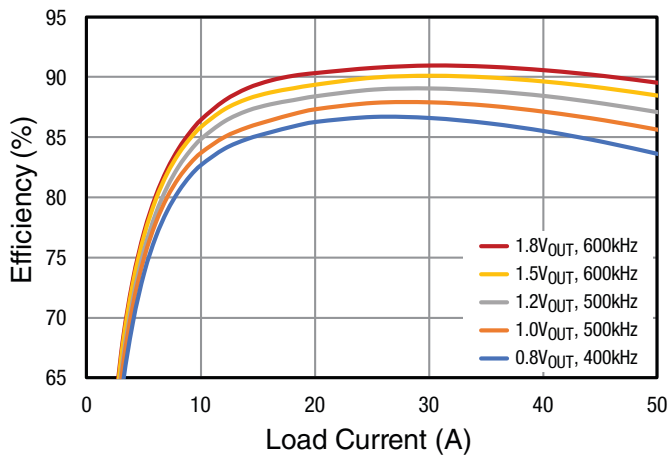
See Figure 18 for typical application schematic.



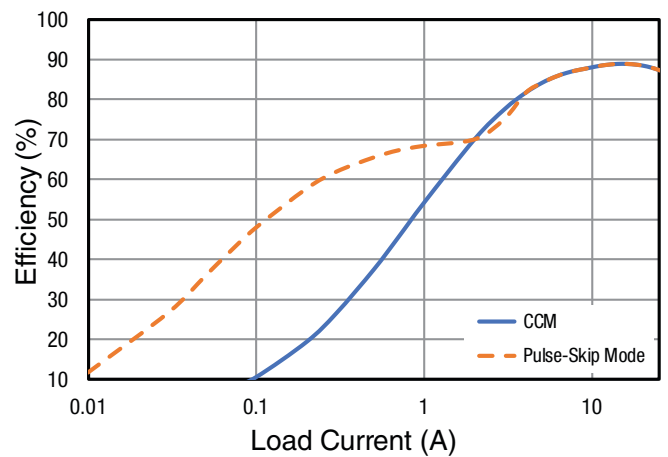
**Figure 4: Efficiency: Single Phase,  $V_{IN} = 5V$**



**Figure 5: Efficiency: Single Phase,  $V_{IN} = 12V$**



**Figure 6: Efficiency: Dual Phase,  $V_{IN} = 12V$**

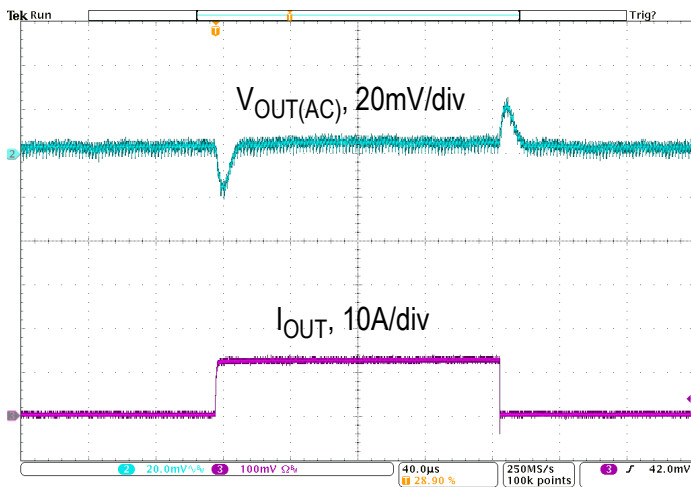


**Figure 7: Efficiency: Pulse-Skipping Mode,  $V_{IN} = 12V$ ,  $V_{OUT} = 1.2V$ , 500kHz**



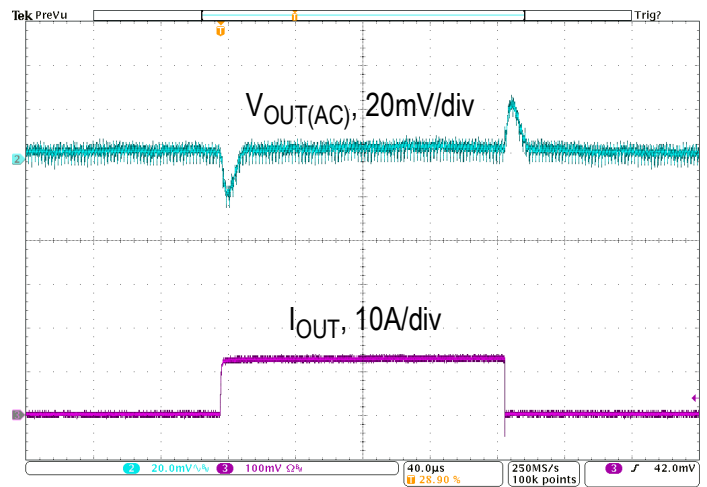
## Load Transient Response, Dual Phase, Single Output

See [Figure 18](#) for typical application schematic.



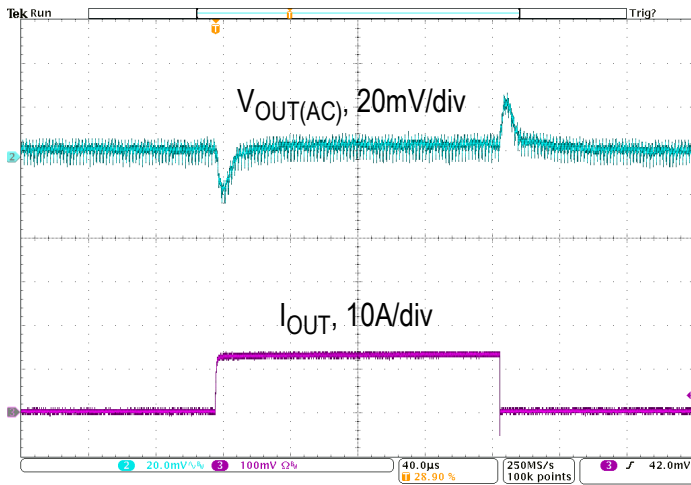
$C_{OUT} = 8 \times 220\mu\text{F}$  Ceramic  
 $C_{FF} = 470\text{pF}$

**Figure 8:** 12V to 1V, 500kHz, 12.5A Load Step, 10A/ $\mu$ s Step-Up and Step-Down



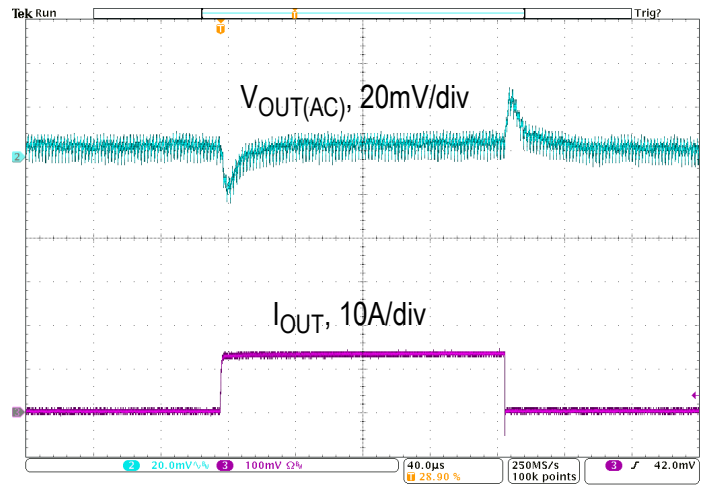
$C_{OUT} = 8 \times 220\mu\text{F}$  Ceramic  
 $C_{FF} = 470\text{pF}$

**Figure 9:** 12V to 1.2V, 500 kHz, 12.5A Load Step, 10A/ $\mu$ s Step-Up and Step-Down



$C_{OUT} = 8 \times 220\mu\text{F}$  Ceramic  
 $C_{FF} = 470\text{pF}$

**Figure 10:** 12V to 1.5V, 600kHz, 12.5A Load Step, 10A/ $\mu$ s Step-Up and Step-Down

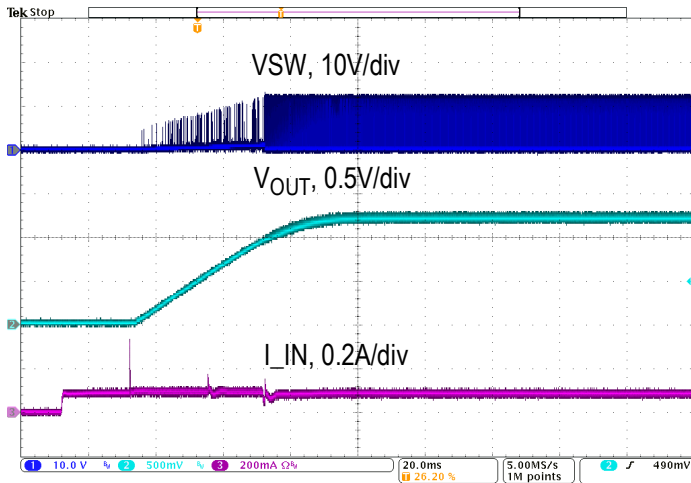


$C_{OUT} = 8 \times 220\mu\text{F}$  Ceramic  
 $C_{FF} = 470\text{pF}$

**Figure 11:** 12V to 1.8V, 600kHz, 12.5A Load Step, 10A/ $\mu$ s Step-Up and Step-Down

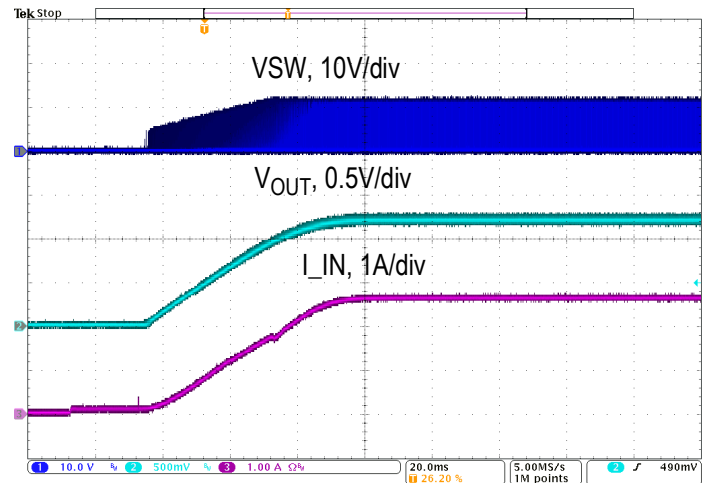
## Start-Up, Single Phase

See Figure 18 for typical application schematic.



$C_{OUT} = 1 \times 470\mu\text{F POSCAP} + 2 \times 100\mu\text{F Ceramic}$   
 $C_{SS} = 0.1\mu\text{F}$

**Figure 12: No Load, 12V to 1.2V, 500kHz**

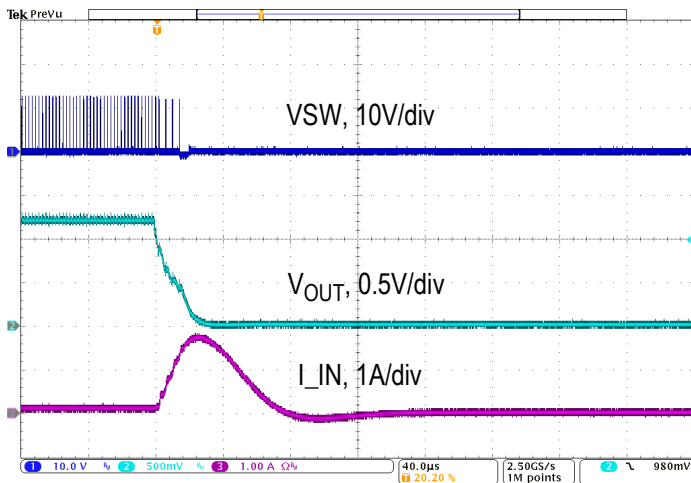


$C_{OUT} = 1 \times 470\mu\text{F POSCAP} + 2 \times 100\mu\text{F Ceramic}$   
 $C_{SS} = 0.1\mu\text{F}$

**Figure 13: 25 A, 12V to 1.2V, 500kHz**

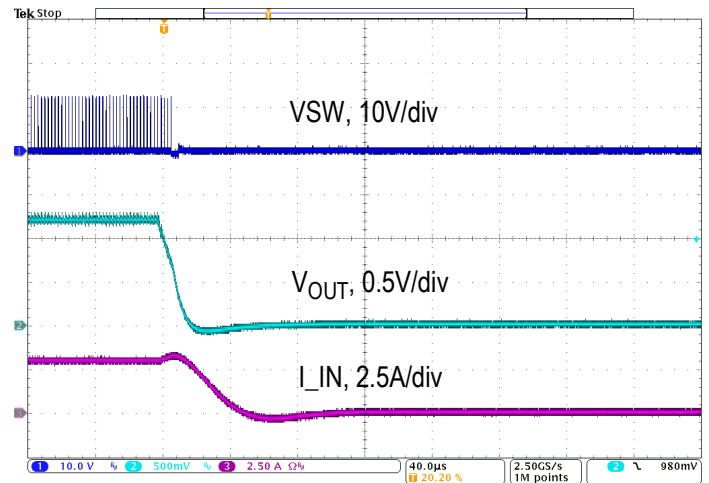
## Short Circuit Protection, Single Phase

See Figure 18 for typical application schematic.



$C_{OUT} = 1 \times 470\mu\text{F POSCAP} + 2 \times 100\mu\text{F Ceramic}$   
 $C_{SS} = 0.1\mu\text{F}$

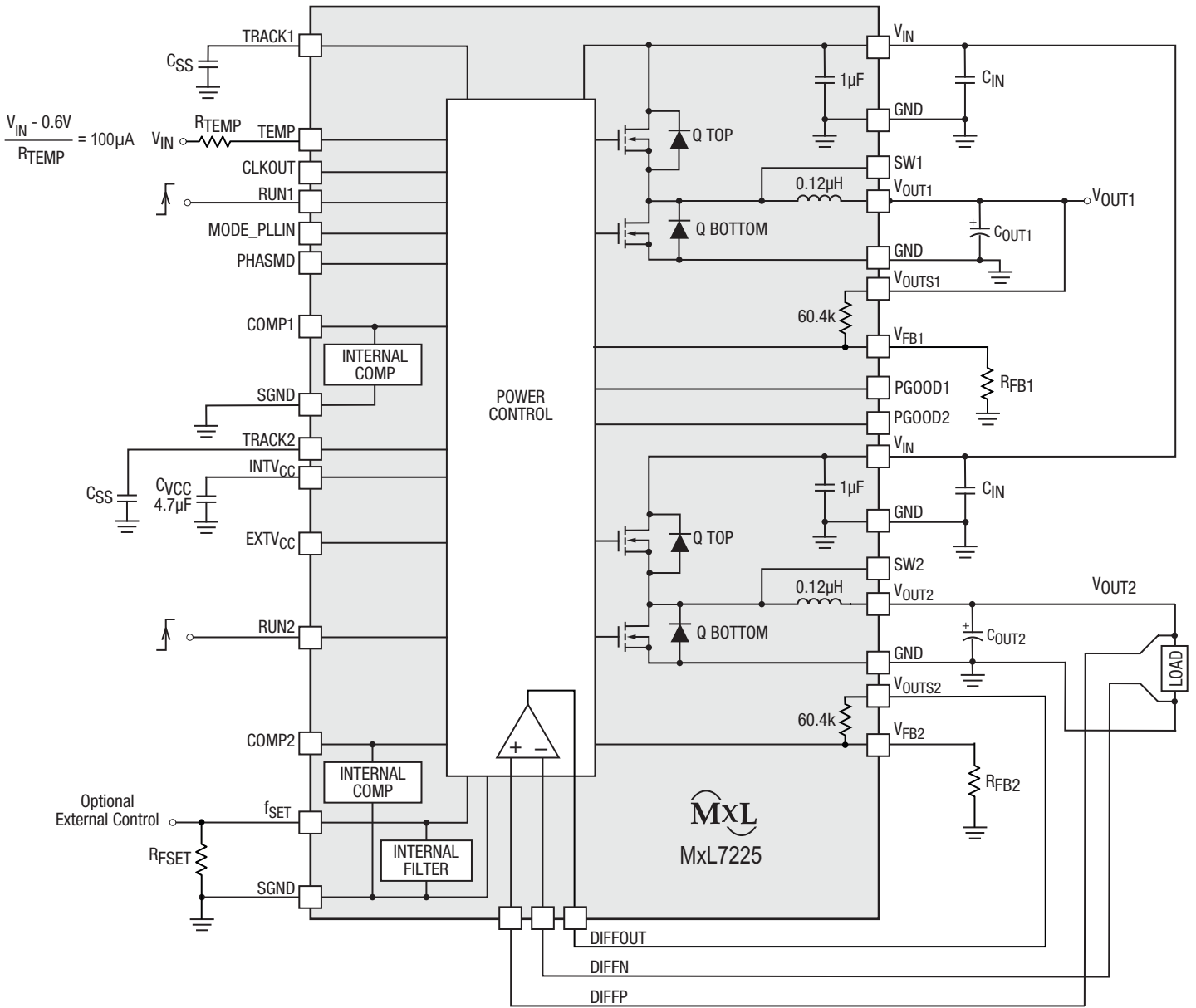
**Figure 14: No Load, 12V to 1.2V, 500kHz**



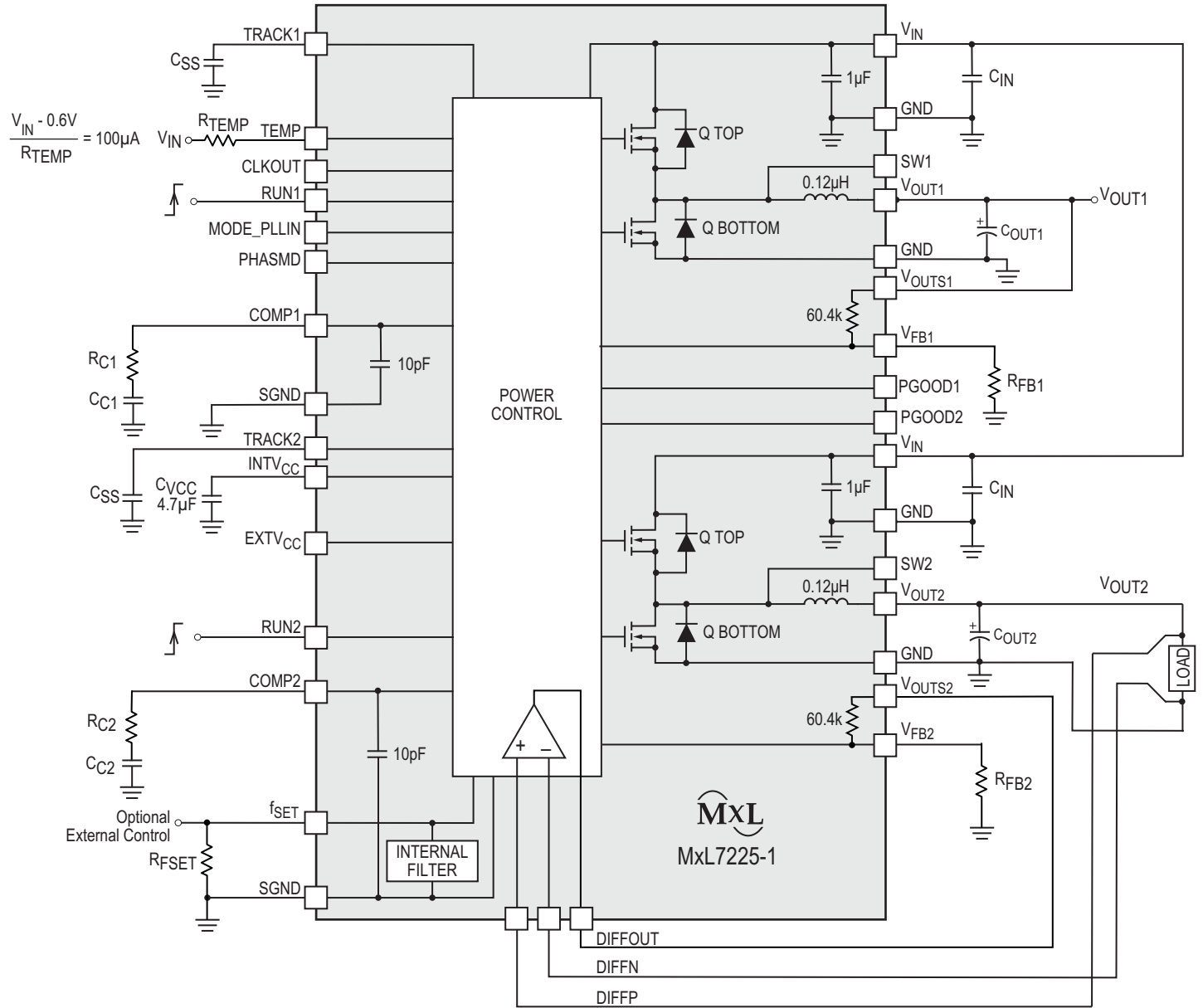
$C_{OUT} = 1 \times 470\mu\text{F POSCAP} + 2 \times 100\mu\text{F Ceramic}$   
 $C_{SS} = 0.1\mu\text{F}$

**Figure 15: 25 A, 12V to 1.2V, 500kHz**

# Functional Block Diagrams



**Figure 16: MxL7225 Functional Block Diagram**



**Figure 17: MxL7225-1 Functional Block Diagram**

## Operation

### Power Module Description

The MxL7225 is a dual-channel, standalone, synchronous step-down power module that provides two 25A outputs or one 50A output. This power module has a continuous input voltage range of 4.5V to 15V and has been optimized for 12V conversions. It provides precisely regulated output voltages from 0.6V to 1.8V that are set by a single external resistor. See the typical application schematic in [Figure 18](#).

The module employs a constant frequency, peak current mode control loop architecture. It also has an internal feedback loop compensation. These features ensure the MxL7225 has sufficient stability margins as well as good transient performance over a wide range of output capacitors, including low ESR ceramic capacitors.

The peak current mode control supports cycle-by-cycle fast current limit and current limit hiccup in overcurrent or output short circuit conditions. The open-drain PGOOD outputs are pulled low when the output voltage exceeds  $\pm 10\%$  of its set point. Once the output voltage exceeds  $+10\%$ , the high side MOSFET is kept off while the low side MOSFET turns on, clamping the output voltage. The overvoltage and undervoltage detection are referenced to the feedback pin.

The RUN1 and RUN2 pins enable and disable the module's two channels. Pulling a RUN pin below 1.1V forces the respective regulator into shutdown mode and turns off both the high side and low side MOSFETs. The TRACK pins are used for either programming the output voltage ramp and voltage tracking during start-up, or for soft-starting the channels.

The MxL7225 includes a differential remote sense amplifier (with a gain of +1). This amplifier can be used to accurately sense the voltage at the load point on one of the module's two outputs or on a single parallel output.

The switching frequency is programmed from 400kHz to 780kHz using an external resistor on the  $f_{SET}$  pin. For noise sensitive applications, the module can be synchronized to an external clock.

The MxL7225 module can be configured to current share between channels or can also be set to current share between modules (multiphase or ganged operation). Using the MODE\_PLLIN, PHASMD and CLKOUT pins, multiphase operation of up to 12 phases is possible with multiple MxL7225s running in parallel.

Using the MODE\_PLLIN pin to operate in pulse-skipping mode results in high efficiency performance at light loads. This light load feature extends battery life.

The EXTV<sub>CC</sub> pin allows an external 5V supply to power the module and eliminate power dissipation in the internal 5V LDO. EXTV<sub>CC</sub> has a threshold of 4.7V for activation and a max operating rating of 5.5V. It must sequence on after V<sub>IN</sub> and sequence off before V<sub>IN</sub>.

Monitor the internal die temperature by using the TEMP pin. Pull the anode up to V<sub>IN</sub> through an external resistor to set the bias current in the diode. Thermal simulation has shown that the thermal monitor on the controller die is within 5°C of the MOSFETs.

The MxL7225-1 is identical to the MxL7225 except that there are no internal control loop compensation components. When dealing with an atypical selection of output capacitors or when further loop optimization is desired, the MxL7225-1 offers more flexibility.

## Applications Information

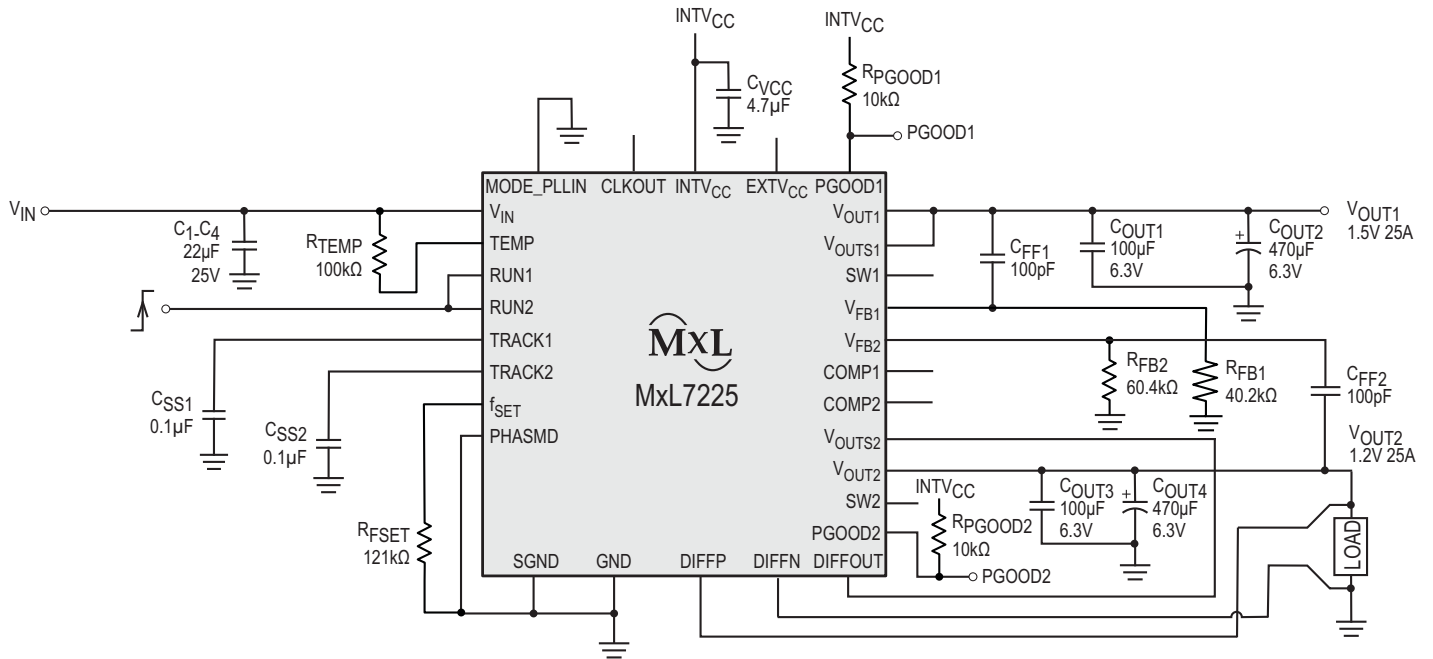
### Typical Application Circuit

The typical MxL7225 application circuit is shown in [Figure 18](#). External component selection is primarily determined by the maximum load current and output voltage. Refer to [Table 7](#) for a selection of various design solutions. Additional information about selecting external compensation components can be found in the [Stability and Compensation](#) section.

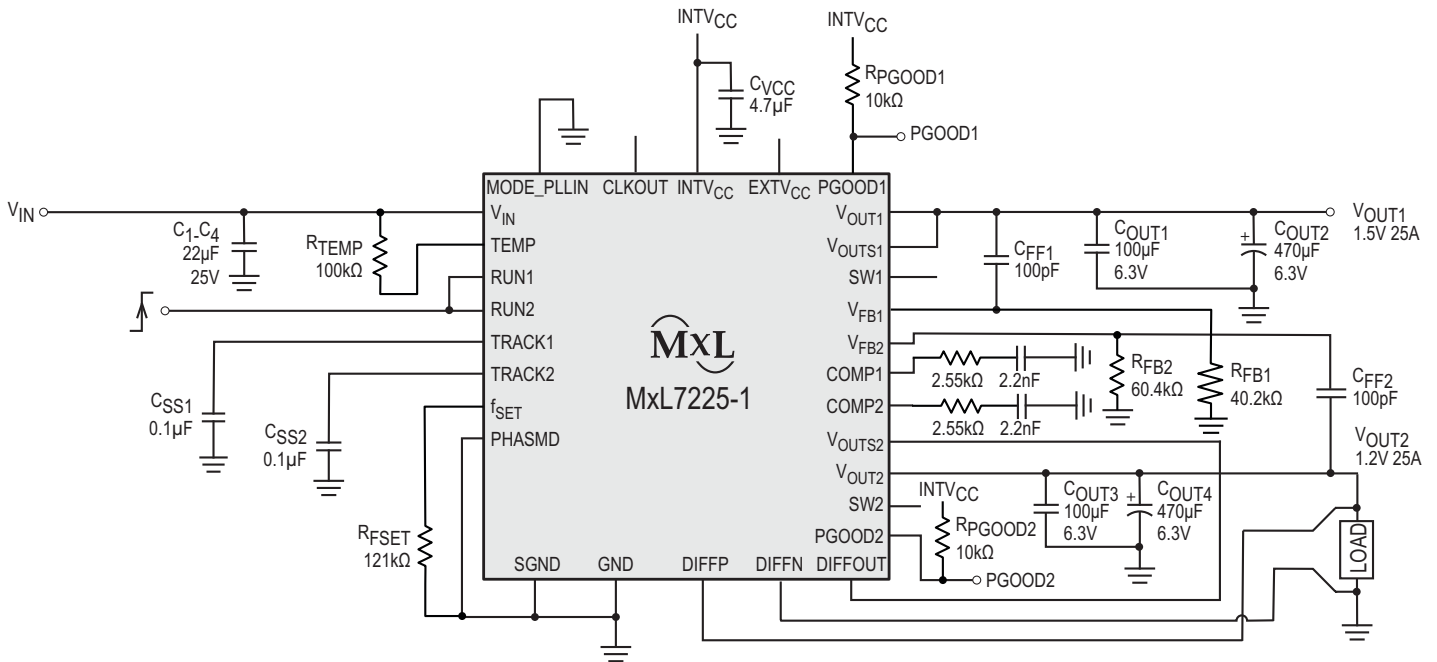
### V<sub>IN</sub> to V<sub>OUT</sub> Step-Down Ratios

For a given input voltage, there are limitations to the maximum possible V<sub>IN</sub> and V<sub>OUT</sub> step-down ratios.

The MxL7225 has a maximum duty cycle of 90% at 500kHz, meaning that the maximum output voltage will be approximately  $0.9 \times V_{IN}$ . When running at a high duty cycle, output current can be limited by the power dissipation in the high-side MOSFET. The minimum output voltage from a given input is controlled by the minimum on-time, which is 90ns. The minimum output voltage is either  $V_{IN} \times f_{SW}(\text{MHz}) \times 0.09\mu\text{s}$  or 0.6V, whichever is higher. To get a lower output voltage, reduce the switching frequency.



**Figure 18:** Typical  $4.5V_{IN}$  to  $15V_{IN}$ , 1.5V and 1.2V at 25A Outputs, MxL7225



**Figure 19:** Typical  $4.5V_{IN}$  to  $15V_{IN}$ , 1.5V and 1.2V at 25A Outputs, MxL7225-1

## Output Voltage Programming

The PWM controller has an internal 0.6V reference. A resistor  $R_{FB}$  between the  $V_{FB}$  and SGND pins programs the output voltage. A 60.4k $\Omega$  internal feedback resistor is connected from  $V_{OUTS1}$  to  $V_{FB1}$  and from  $V_{OUTS2}$  to  $V_{FB2}$ , as illustrated in the functional block diagram.

$R_{FB}$  values for corresponding standard  $V_{OUT}$  values are shown in [Table 6](#). Use the following equation to determine the  $R_{FB}$  value for other  $V_{OUT}$  levels:

$$R_{FB} = \frac{0.6V \times 60.4k\Omega}{V_{OUT} - 0.6V} \quad \text{Equation 1}$$

In the case of paralleling multiple channels and devices, when all  $V_{FB}$  pins are tied together and only one  $V_{OUTS}$  pin is connected to the output, a common  $R_{FB}$  resistor may be used. Select the  $R_{FB}$  as explained above. Note that each  $V_{FB}$  pin has an  $I_{FB}$  max of 20nA. To reduce  $V_{OUT}$  error due to  $I_{FB}$ , use an additional  $R_{FB}$  and connect the corresponding  $V_{OUTS}$  to  $V_{OUT}$  as shown in [Figure 21](#).

**Table 6:  $V_{FB}$  Resistor Table vs. Various Output Voltages**

$V_{OUT}$	0.6V	0.8V	1.0V	1.2V	1.5V	1.8V
$R_{FB}$	Open	182k	90.9k	60.4k	40.2k	30.2k

## Input Capacitors

Use four 22 $\mu$ F ceramic input capacitors to reduce RMS ripple current on the regulator input.

A bulk input capacitor is required if the source impedance is high or the source capacitance is low. For additional bulk input capacitance, use a surface mount 47 $\mu$ F to 100 $\mu$ F aluminum electrolytic bulk capacitor.

## Output Capacitors

The output capacitors, denoted as  $C_{OUT}$ , need to have low enough equivalent series resistance (ESR) to meet output voltage ripple and transient requirements. The MxL7225 can use low ESR tantalum capacitors, low ESR polymer capacitors, ceramic capacitors or a combination of those for  $C_{OUT}$ . Refer to [Table 7](#) for  $C_{OUT}$  recommendations that optimize performance for different output voltages.

## Pulse-Skipping Mode Operation

The pulse-skipping mode enables the module to skip cycles at light loads which reduces switching losses and increases efficiency at low to intermediate currents. To enable this mode, connect the MODE\_PLLIN pin to the INTV<sub>CC</sub> pin.

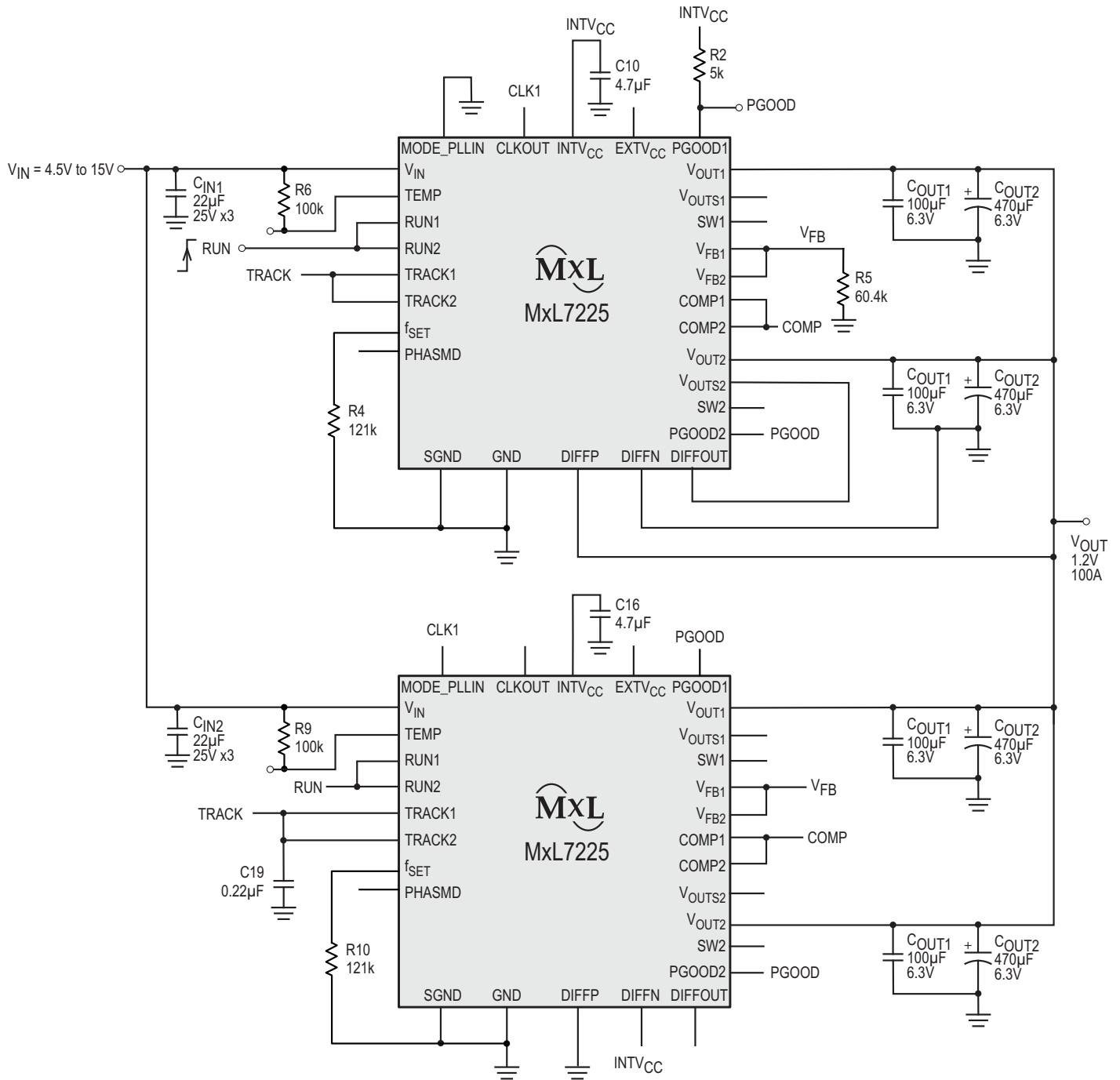
## Forced Continuous Operation

Forced continuous operation is recommended when fixed frequency is more important than light load efficiency, and when the lowest output ripple is desired. To enable this mode, connect the MODE\_PLLIN pin to GND.

## Multiphase Operation

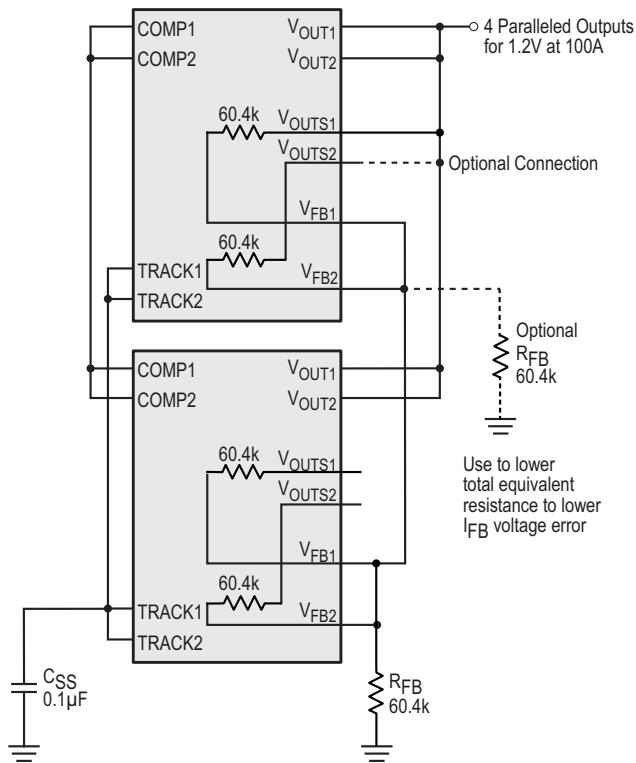
Multiphase operation is used to achieve output currents greater than 25A. It can be used with both MxL7225 channels to achieve one 50A output. It can also be used by paralleling multiple MxL7225s and running them out of phase to attain one single high current output, up to 300A. Ripple current in both the input and output capacitors is substantially lower using a multiphase design, especially when the number of phases multiplied by the output voltage is less than the input voltage. Input RMS ripple current and output ripple amplitude is reduced by the number of phases used while the effective ripple frequency is multiplied by the number of phases used. The MxL7225 is a peak current mode controlled device which results in very good current sharing between parallel modules and balances the thermal loading. [Figure 20](#) shows an example of a 2-module, 4-phase, single output regulator that can handle load current up to 100A.

Up to 12 phases can be paralleled by using each MxL7225 channel's PHASMD, MODE\_PLLIN and CLKOUT pins. When the CLKOUT pin is connected to the following stage's MODE\_PLLIN pin, the frequency and the phase of both devices are locked. Phase difference can be obtained between MODE\_PLLIN and CLKOUT of 120 degrees, 60 degrees or 90 degrees respectively by connecting the PHASMD pin to INTV<sub>CC</sub>, SGND or by floating it. [Figure 21](#) shows an example of parallel operation and [Figure 22](#) shows examples of 2-phase, 4-phase and 6-phase designs.



**Figure 20: MxL7225 2-Module, 4-Phase, 1.2V, 100A Regulator**

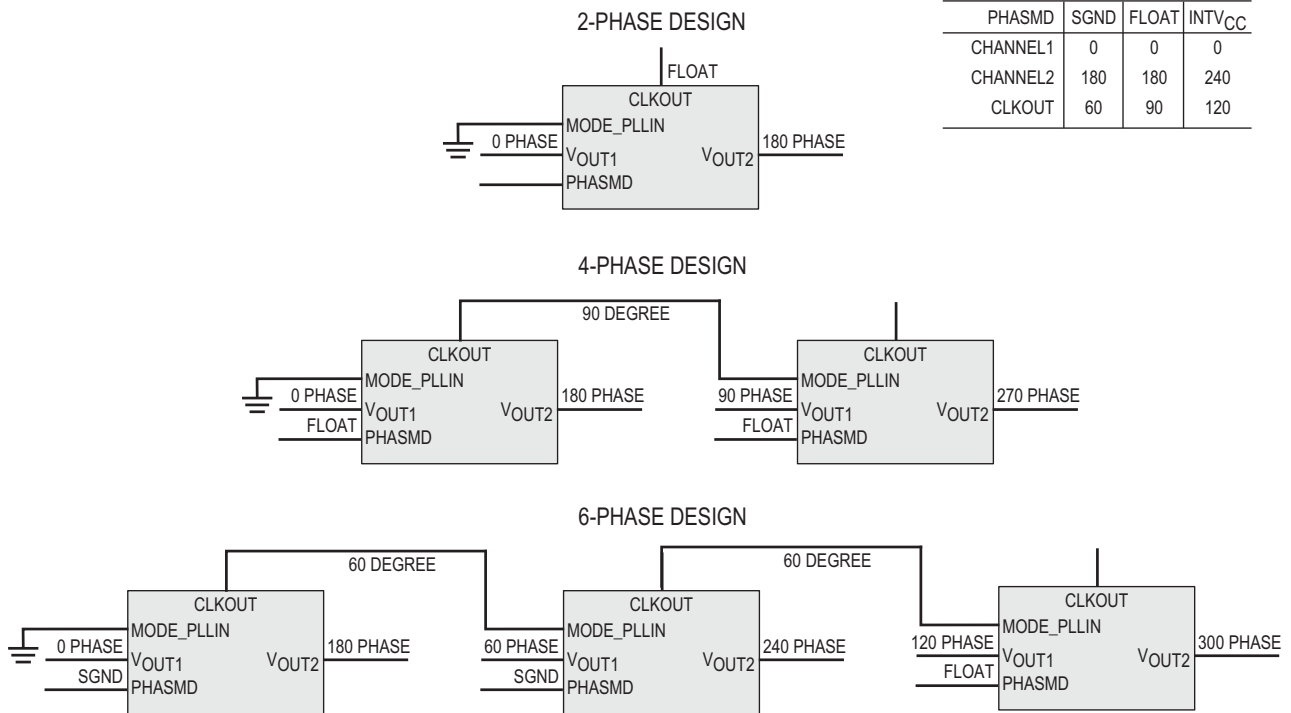




**Figure 21: 4-Phase Parallel Configuration**

When paralleling multiple channels and devices:

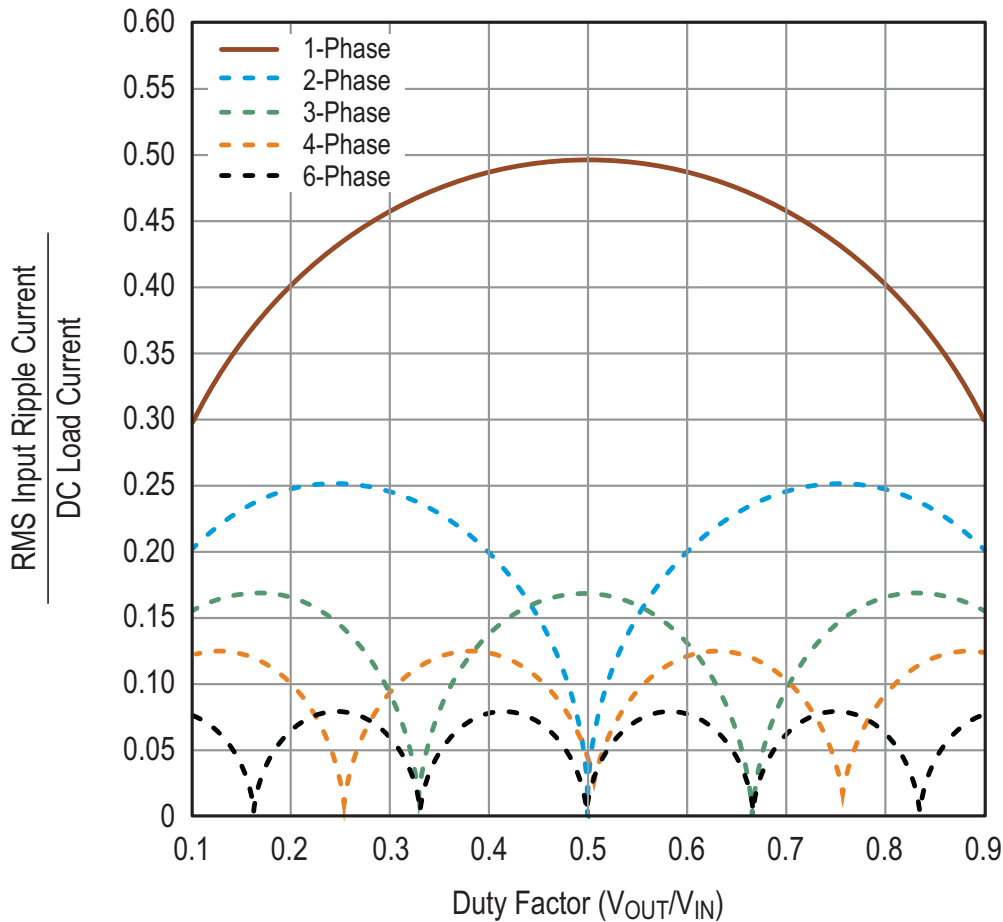
- Tie all V<sub>FB</sub> pins together.
- Tie all RUN pins together.
- Connect only one of the V<sub>OUTS</sub> pins to V<sub>OUT</sub> (or DIFFOUT in the case of remote sensing). In this case, only the R<sub>FB</sub> corresponding to that V<sub>OUTS</sub> pin should be populated. Refer to **Output Voltage Programming** for the calculation of R<sub>FB</sub>. All other V<sub>OUTS</sub> pins should be left floating.
- If V<sub>OUT</sub> offset created by I<sub>FB</sub> (20nA max per channel) is a concern, additional R<sub>FB</sub> resistors may be populated to mitigate the effect. In such a configuration, each R<sub>FB</sub> should be the same resistance value as that in the single R<sub>FB</sub> case, and the corresponding V<sub>OUTS</sub> pin should be connected to V<sub>OUT</sub> (or DIFFOUT in the case of remote sensing).
- If remote sensing, only one differential amplifier should be used.
- In MxL7225-1, external R<sub>C</sub> and C<sub>C</sub> components are required. Only one R<sub>C</sub> and one C<sub>C</sub> are needed given that all COMP pins are tied together.



**Figure 22: Examples of 2-Phase, 4-Phase and 6-Phase Operation with PHASMD Table**

## Input Ripple Current Cancellation

Figure 23 illustrates the RMS ripple current reduction that is expected as a function of the number of interleaved phases.



**Figure 23:** Input RMS Current to DC Load Current Ratio as a Function of Duty Cycle

## Frequency Selection and Phase-Locked Loop

To increase efficiency, the MxL7225 works over a range of frequencies. For lower output voltages or duty cycles, lower frequencies are recommended to lower MOSFET switching losses and improve efficiency. For higher output voltages or duty cycles, higher frequencies are recommended to limit inductor ripple current. Refer to the efficiency graphs and their operating frequency conditions. When selecting an operating frequency, keep the highest output voltage in mind.

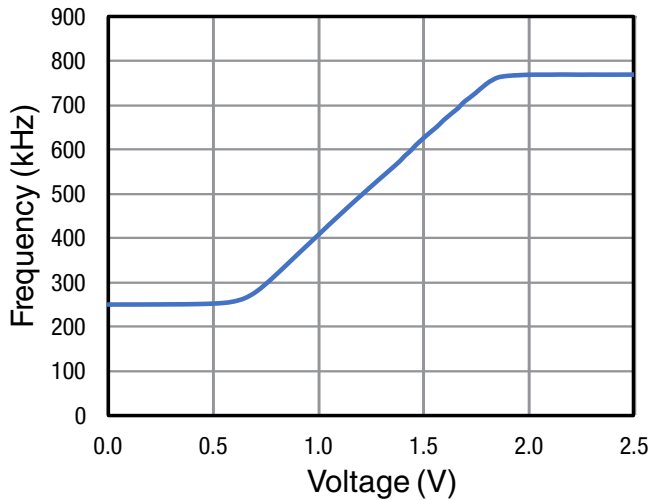
Use an external resistor between the  $f_{SET}$  pin and SGND to set the switching frequency. An accurate  $10\mu A$  current source into the resistor sets a voltage that programs the frequency. Alternatively, a DC voltage can be applied to

$f_{SET}$  to program the frequency. Figure 24 illustrates the operating frequency versus the  $f_{SET}$  pin voltage.

An external clock with a frequency range of 400kHz to 780kHz and a voltage range of 0V to  $INTV_{CC}$  can be connected to the MODE\_PLLIN pin. The high level threshold of the clock input is 1.6V and the low level threshold of the clock input is 1V.

The MxL7225 integrates the PLL loop filter components. Ensure that the initial switching frequency is set with an external resistor before locking to an external clock. Both regulators will operate in continuous mode while being synchronized to an external clock signal.

The PLL phase detector output charges and discharges the internal filter network with a pair of complementary current sources. When an external clock is connected, an internal switch disconnects the external  $f_{SET}$  resistor. The switching frequency then locks to the incoming external clock. If no external clock is connected, then the internal switch is on, which connects the external  $f_{SET}$  resistor.



**Figure 24:** Operating Frequency vs.  $f_{SET}$  Pin Voltage

## Minimum On-Time

Minimum On-Time  $t_{ON(MIN)}$  is the shortest time that the controller can turn on the high-side MOSFET of either channel. Approaching this time may be more of an issue in low duty cycle applications. Use the following equation to make sure the on-time is above this minimum:

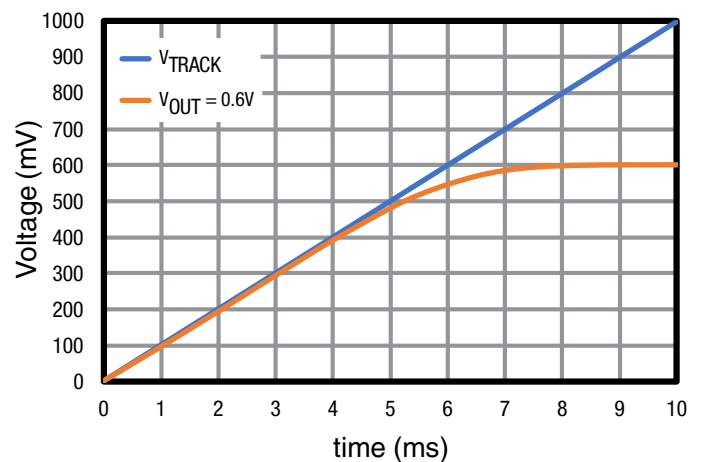
$$\frac{V_{OUT}}{V_{IN} \times \text{FREQ}} > t_{ON(MIN)} \quad \text{Equation 2}$$

If the on-time falls below this minimum, the channel will start to skip cycles. In this case, the output voltage continues to regulate, however output ripple increases. Lowering the switching frequency increases on-time. The minimum on-time specified in the electrical characteristics is 90ns.

## Soft-Start and Output Voltage Tracking

A capacitor  $C_{SS}$  can be connected from the TRACK pin to ground to implement soft-start. The TRACK pin is charged by a  $1.25\mu\text{A}$  current source up to the reference voltage and then on to  $\text{INTV}_{CC}$ . The MxL7225 has a smooth transition from TRACK to  $V_{OUT}$  as shown in Figure 25. If the RUN pin is below 1.2V, the TRACK pin is pulled low. The following equation can be used to calculate soft-start time, defined as when PGOOD asserts:

$$t_{\text{SOFTSTART}} = \frac{C_{SS}}{1.25\mu\text{A}} \times 0.65\text{V} \quad \text{Equation 3}$$

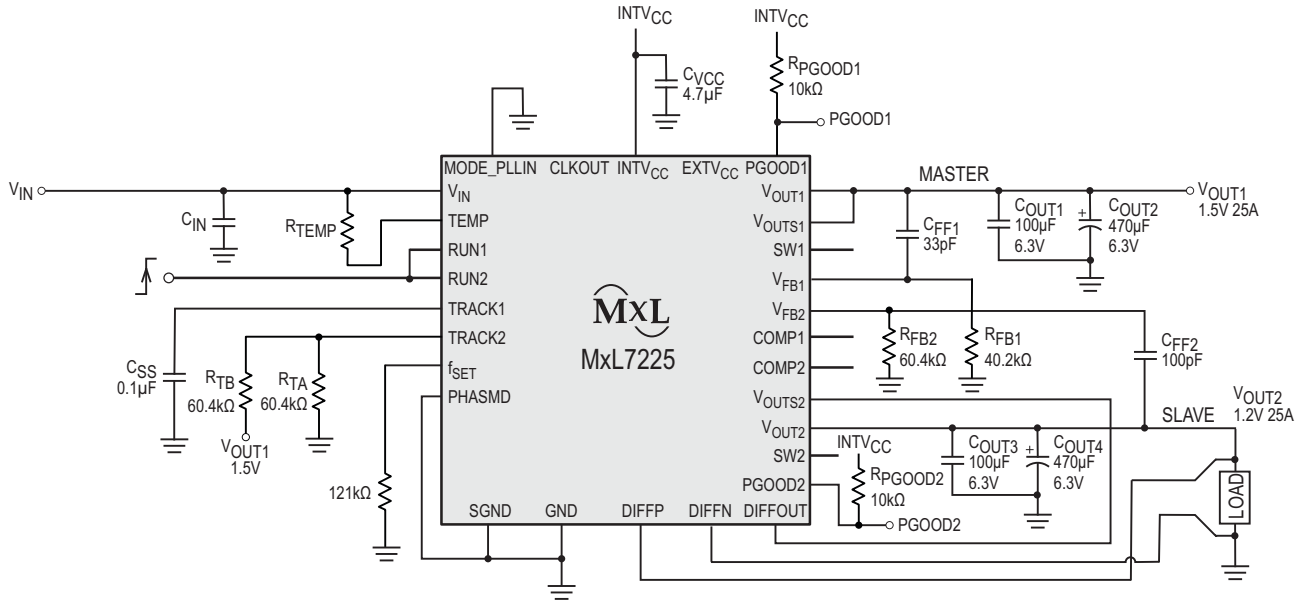


**Figure 25:**  $V_{\text{OUT}}$  and  $V_{\text{TRACK}}$  versus Time

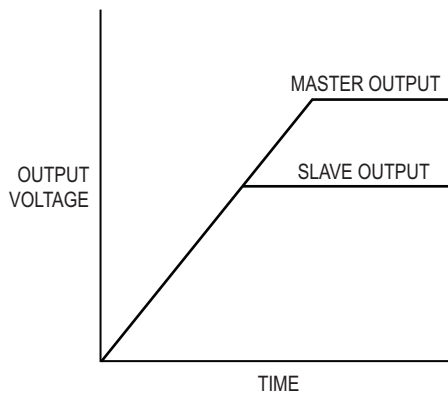
The MODE\_PLLIN pin selects between forced continuous mode or pulse-skipping mode during steady-state operation. Regardless of the mode selected, the module channels will always start in the pulse-skipping mode up to  $\text{TRACK} = 0.54\text{V}$ , beyond which point the operation mode will follow the MODE\_PLLIN setting.

The TRACK pins can be used to externally program the output voltage tracking. The output may be tracked up and down with another regulator. The master regulator's output is divided down with an external resistor divider that is the same as the slave regulator's feedback divider to implement coincident tracking. Note that each MxL7225 channel has an internal accurate  $60.4\text{k}\Omega$  for the top feedback resistor. Refer to the equation below, which is applicable for  $V_{\text{TRACK(SLAVE)}} < 0.8\text{V}$ . An example of coincident tracking is shown in Figure 26.

$$V_{\text{OUT(SLAVE)}} = \left(1 + \frac{60.4\text{k}}{R_{\text{TA}}}\right) \times V_{\text{TRACK(SLAVE)}} \quad \text{Equation 4}$$



**Figure 26: Example of Output Tracking Application Circuit**



**Figure 27: Output Coincident Tracking Waveform**

The ramping voltage is applied to the track pin of the slave. Since the same resistor values are used to divide down the output of the master and to set the output of the slave, the slave tracks with the master coincidentally until its final value is achieved. The master continues from the slave's regulation point to its final value. In [Figure 26](#),  $R_{TA}$  is equal to  $R_{FB2}$  for coincident tracking.

## Power Good

Each channel's open drain PGOOD pin can be used to monitor if its respective  $V_{OUT}$  is outside  $\pm 10\%$  of the set point. The PGOOD pin is pulled low when the output of the corresponding channel is outside the monitoring window, the RUN pin is below its threshold (1.25V), or the MxL7225 is in the soft-start or tracking phase. The PGOOD pin will go high impedance immediately after  $V_{FB}$  voltage is within the monitoring window. Note that there is an internal  $20\mu s$  glitch filtering in PGOOD when  $V_{FB}$  voltage goes out of the monitoring window.

If desired, a pullup resistor can be connected from the PGOOD pins to a supply voltage with a maximum level of 6V.

## Stability and Compensation

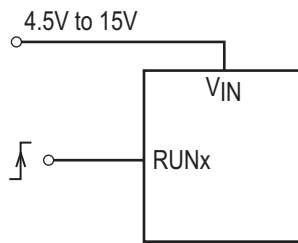
The MxL7225 module is internally compensated for stability over a wide range of operating conditions. Refer to [Table 7](#) for recommended configurations. For other configurations or for MxL7225-1 loop compensation, please consult a Maxlinear Field Applications Engineer.

## Enabling Channels

There are two supported methods to enable and disable each channel.

### Method 1

Method 1 is to drive the RUNx pin of the channel to be enabled (CHx) with a logic signal as shown in [Figure 28](#).



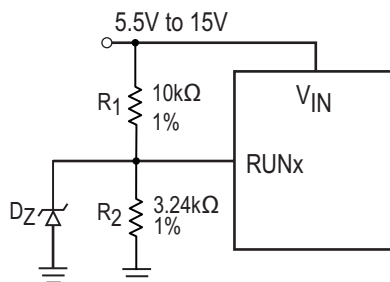
**Figure 28: RUNx Pin Driven by a Logic Signal**

$V_{IN}$  should be in the operating range (4.5V to 15V) before the logic signal at RUNx goes high. The logic high level must be above 1.3V in order to ensure that the RUNx threshold is crossed. To disable a channel (CHx), the logic signal at the corresponding RUNx pin must be brought down to 1.1V or below.

### Method 2

Method 2 is a self-start method. This method uses a resistor divider to divide down  $V_{IN}$  and drive the RUNx pin with the divided voltage. The choice of the resistor divider ratio depends on the  $V_{IN}$  range.

[Figure 29](#) shows the self-start method for an application where  $V_{IN}$  is in the range of 5.5V to 15V.



**Figure 29: Self-Start for  $V_{IN}$  Range of 5.5V to 15V**

Resistors  $R_1$  and  $R_2$  divide  $V_{IN}$  down and the divided voltage drives the RUNx pin. The  $R_1$  and  $R_2$  values are chosen such that  $V_{IN}$  reaches 5V before RUNx crosses the

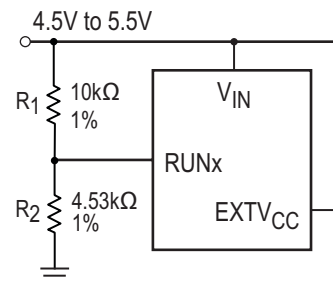
RUN threshold. Equation 5 shows the relationship between  $R_1$ ,  $R_2$  and  $V_{IN(TH)}$  which is the  $V_{IN}$  value when the RUNx voltage crosses 1.26V:

$$1 + \frac{R_1}{R_2} = \frac{V_{IN(TH)}}{1.26V} \quad \text{Equation 5}$$

Select  $R_1$  and  $R_2$  by letting  $V_{IN(TH)} = 5V$ .

If the application is for  $V_{IN} = 12V$ , the choice of  $V_{IN(TH)}$  for Equation 5 can be higher than 5V but less than the minimum of the  $V_{IN}$  tolerance band. For example, if  $V_{IN}$  is  $12V \pm 10\%$ , then choose a  $V_{IN(TH)}$  between 5V and 10V. A zener diode from RUNx pin to ground is optional for protection of the RUNx pin (to clamp RUNx to 5V) in the event of the  $R_2$  resistor not being connected due to a board level fault.

[Figure 30](#) shows the self-start method for an application where  $V_{IN}$  is in the range of 4.5V to 5.5V.



**Figure 30: Self-Start for  $V_{IN}$  Range of 4.5V to 5.5V**

In an application where  $V_{IN}$  is the range of 4.5V to 5.5V, it is required to connect  $V_{IN}$  to  $EXTV_{CC}$ . Select  $R_1$  and  $R_2$  based on Equation 5, but use 4V for  $V_{IN(TH)}$ .

A combination of Method 1 and Method 2 is also recommended where an open drain output drives the RUNx pin with the voltage divider ( $R_1$  and  $R_2$ ) in place. Criteria for the selection of  $R_1$  and  $R_2$  must be followed as described above.

It is important to note that starting up the channels with RUNx floating is not allowed.

## INTV<sub>CC</sub> and EXTV<sub>CC</sub>

The V<sub>IN</sub> input voltage powers an internal 5V low dropout linear regulator. The regulator output (INTV<sub>CC</sub>) provides voltage to the control circuitry of the module. Alternatively, the EXTV<sub>CC</sub> pin allows an external 5V supply to be used to eliminate the 5V LDO power dissipation in power sensitive applications.

## Differential Remote Sense Amplifier

The MxL7225's differential remote sense amplifier can be used to accurately sense voltages at the load. This is particularly useful in high current load conditions. The DIFFP and DIFFN pins must be connected properly to the remote load point, and the DIFFOUT pin must be connected to the corresponding V<sub>OUTS1</sub> or V<sub>OUTS2</sub> pin. The differential amplifier is able to handle an input up to 3.3V.

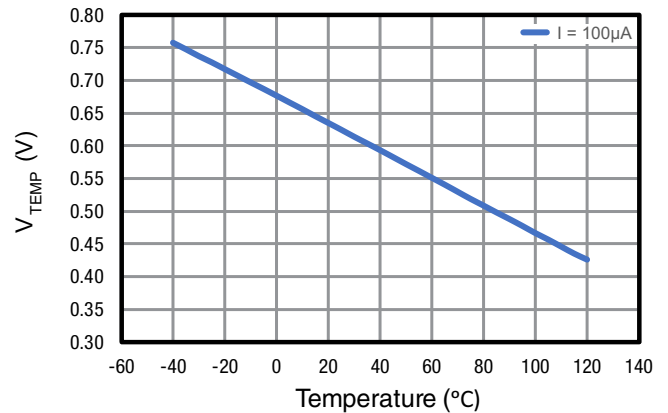
If a C<sub>FF</sub> feed-forward capacitor is desirable in a channel employing the differential amplifier, connect the capacitor between V<sub>FB</sub> and DIFFP instead of DIFFOUT.

## SW Pins

Use the SW pins to monitor the switching node of each channel. These pins are generally used for testing or monitoring. During normal operation, these pins should be unconnected and left floating. However, in conjunction with an external series R-C snubber circuit, these pins can be used to dampen ringing on the switch node caused by LC parasitics in the switched current paths.

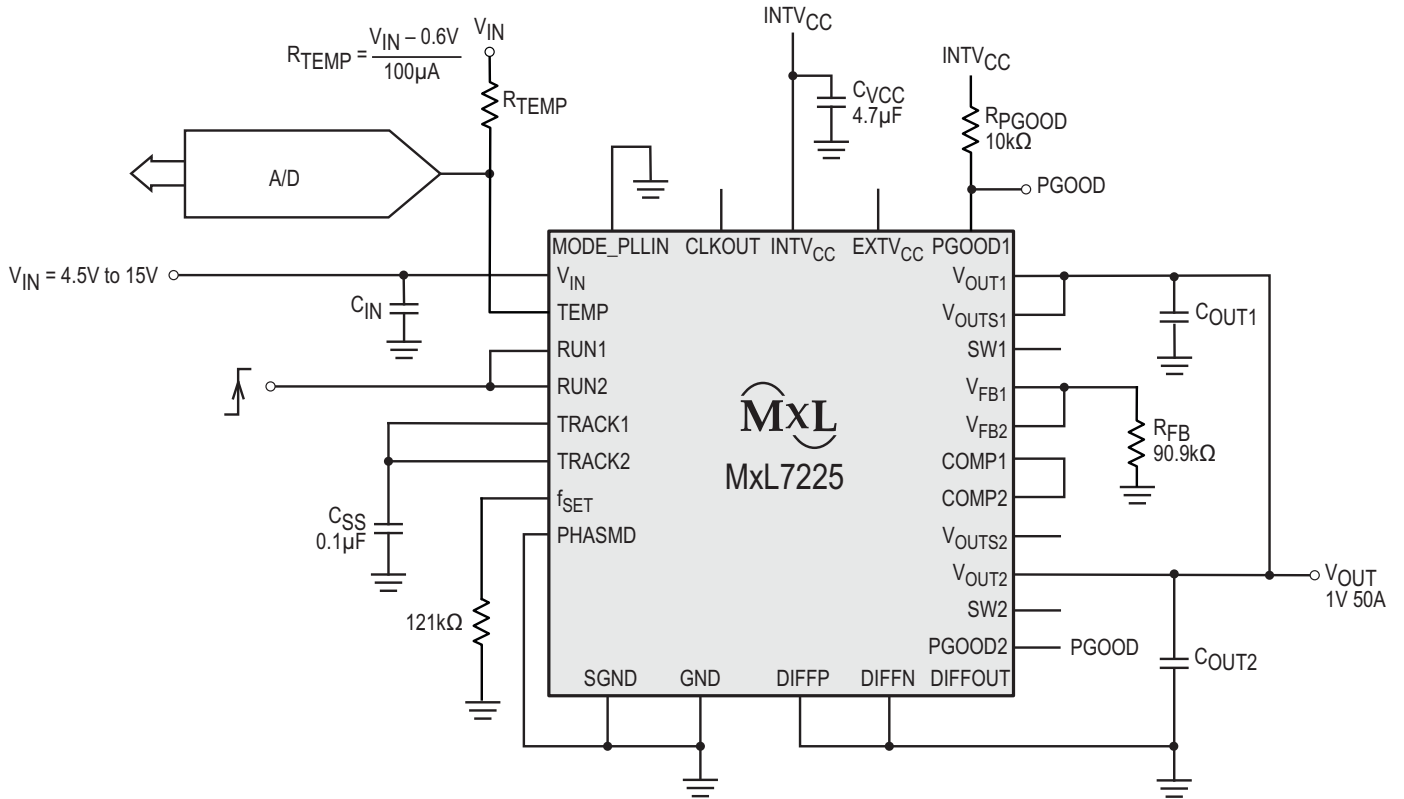
## Temperature Monitoring (TEMP)

An internal temperature sensing diode / PNP transistor is used to monitor its V<sub>BE</sub> voltage over temperature, thus serving as a temperature monitor. Its forward voltage and temperature coefficient are shown in the electrical characteristics section and plotted in Figure 31. It is connected to V<sub>IN</sub> through a pullup resistor R<sub>TEMP</sub> to limit the current to 100μA. It is recommended to set a 60μA minimum current in applications where V<sub>IN</sub> varies over a wide range. See Figure 32 for an example on how to use this feature.



**Figure 31: Diode Voltage vs. Temperature**

For accurate temperature measurement, the temperature sensing diode should first be characterized in a controlled temperature environment such as an oven. Without powering up the module, push a constant current such as 100μA into the TEMP pin and out the GND. Measure the diode voltage at two extreme temperature points. TEMP voltage vs diode temperature for said current is simply a straight line between those two points.



**Figure 32: 2-Phase, 1V at 50A with Temperature Monitoring**

## Fault Protection

The MxL7225 module has built-in overcurrent, output overvoltage, and over-temperature protection.

The overcurrent triggers at a nominal load of 35A. Overcurrent during four consecutive switching cycles initiates a hiccup mode. During hiccup, the high-side and low-side MOSFETs are turned off for 100ms. A soft-start is attempted following the hiccup. If the overcurrent persists, the hiccup will continue.

The overvoltage triggers when the output voltage is 10% above the set-point. In overvoltage mode, the gate-source voltage of the top FET is kept at 0V and the bottom FET is kept on.

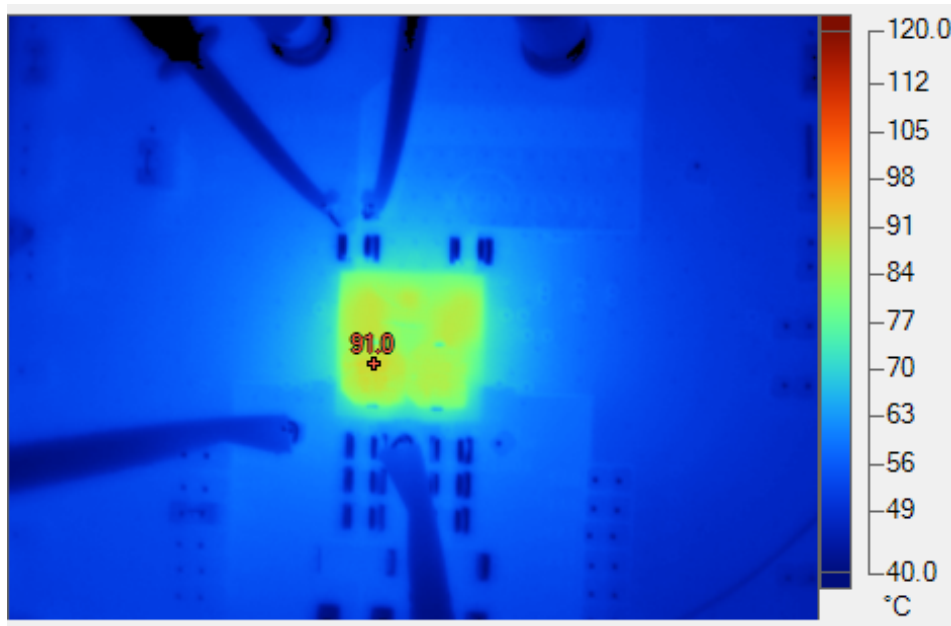
The over-temperature triggers at 145°C. In an over-temperature state, both top and bottom FETs are kept off. When the temperature cools down below 130°C, the module soft-starts.

Since an output overvoltage event is likely caused by a top FET that has failed short, in the case of an input supply that is capable of delivering high power, it is recommended that a fuse be used at the input. This is so that the bottom FET when kept on would cause high input current to flow through the fuse and quickly disengage the input supply and therefore de-energize the faulty module, preventing further damage to the end product.

## Thermal Considerations and Output Current Derating

The design of the MxL7225 module removes heat from the bottom side of the package effectively. Thermal resistance from the bottom substrate material to the printed circuit board is very low.

Proper thermal design is critical in controlling device temperatures and in achieving robust designs. There are many factors that affect the thermal performance. One key factor is the temperature rise of the devices in the package, which is a function of the thermal resistances of the devices inside the package and the power being dissipated. The thermal resistances of the MxL7225 are shown in the **Operating Conditions** section of this datasheet. The JEDEC  $\Theta_{JA}$  thermal resistance provided is based on tests that comply with the JESD51-2A “Integrated Circuit Thermal Test Method Environmental Conditions – Natural Convection” standard. JESD51 is a group of standards whose intent is to provide comparative data based on a standard test condition which includes a defined board construction. Since the actual board design in the final application will be different from the board defined in the standard, the thermal resistances in the final design may be different from those shown.



**Figure 33: Thermal Image 12V to 1V, 50A with No Air Flow<sup>(1)</sup>**

1. Based on a 6-layer 3.9" x 5.1" Printed Circuit Board with 2oz copper on the outer layers and 1 oz copper on all internal layers).

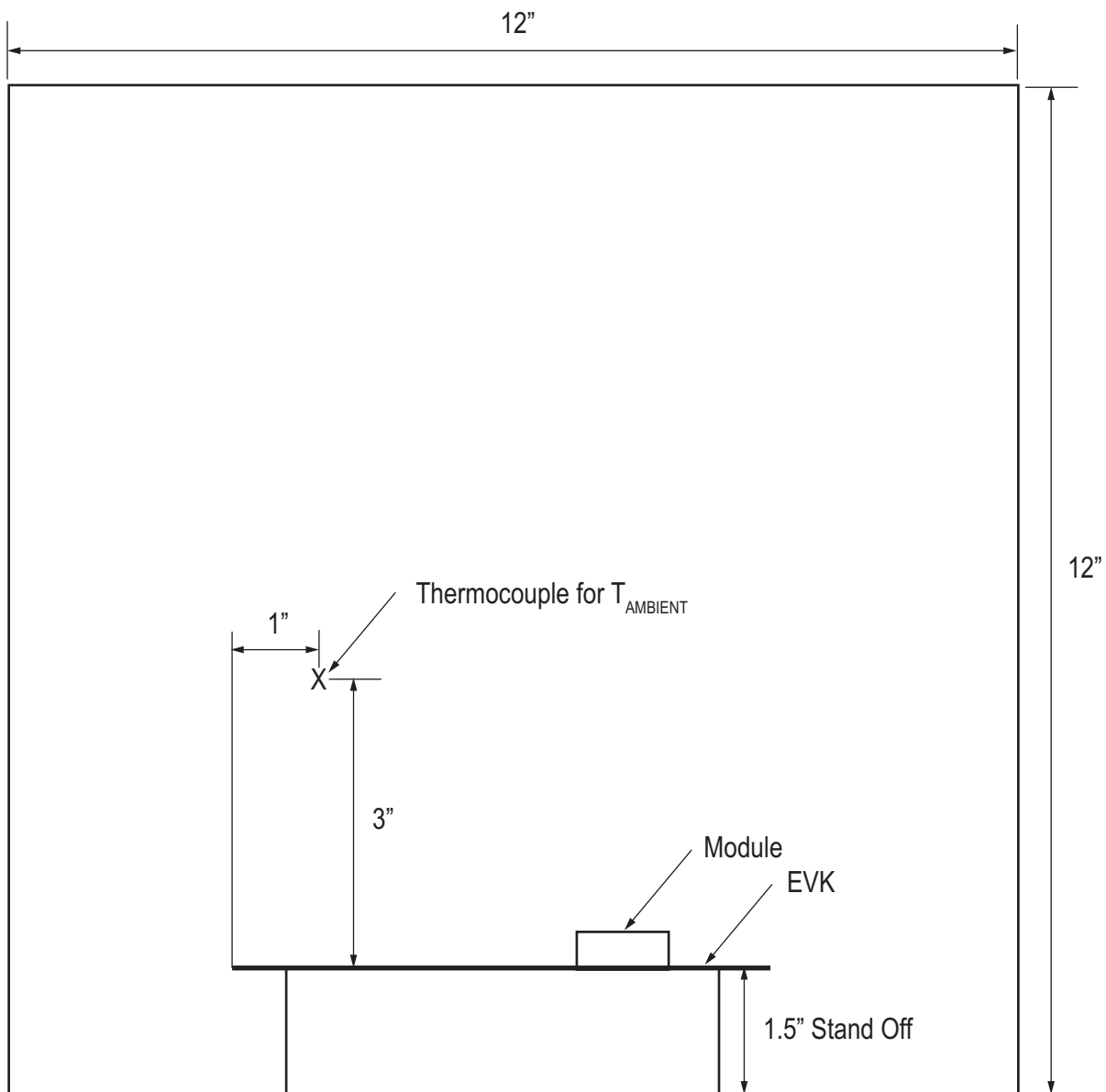


## Power Derating

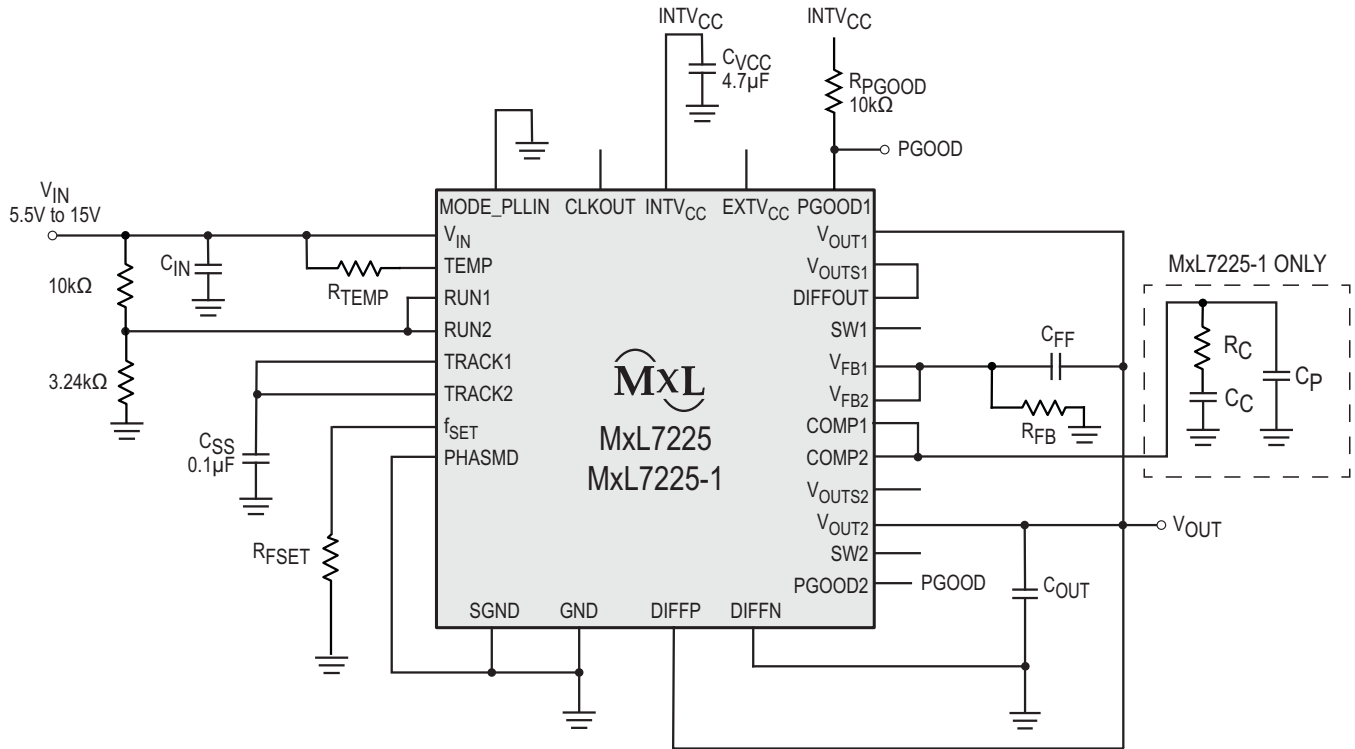
The current derating curves in [Figure 39](#) through [Figure 42](#) were acquired with the test setup in [Figure 34](#). The EVK (see details in [Figure 33](#)) was placed in a 0.5 cubic feet enclosed space with no forced air flow. The EVK was configured as a dual-phase single-output converter. The EVK was first loaded to 50A at room temperature. Ambient temperature was then gradually elevated until the module's temperature sensing diode reached 125°C. This is where

Load Current starts to decrease from 50A in the curves. Beyond this point as ambient temperature increased, Load Current was decreased to maintain the 125°C diode temperature. These curves are accurate for the test setup in [Figure 34](#) and natural convection.

[Figure 37](#) and [Figure 38](#) are the corresponding power dissipation in the module at room temperature.



**Figure 34: Current Derating Curves Measurement Setup**



**Figure 35: Two-Phase Single Output Configuration**

**Table 7: MxL7225 Load Step Response vs. Components, 2-Phase, 1 Output (refer to Figure 35)**

	C <sub>IN</sub>			C <sub>OUT</sub>		
	Vendors	Part Number	Value	Vendors	Part Number	Value
BULK	Panasonic	25SVPF330M	330μF, 25V	Panasonic	ETPF470M5H	470μF, 2.5V, 5mΩ
CERAMIC	Murata	GRM31CR61E226KE15L	22μF, 25V, 1206, X5R	Murata	GRM32ER60J227M	220μF, 6.3V, 1206, X5R
	Würth	885012109014	22μF, 25V, 1210, X5R	Würth	885012109004	100μF, 6.3V, 1210, X5R

**25% Load Step (0 to 12.5A, 10A/μs), Ceramic Output Capacitor Only Solutions**

V <sub>IN</sub>	V <sub>OUT</sub>	C <sub>IN</sub> (BULK)	C <sub>IN</sub> (Ceramic)	C <sub>OUT</sub> (BULK)	C <sub>OUT</sub> (MLCC)	C <sub>FF</sub> (pF)	P-P Deviation (mV) <sup>(1)</sup>	Feedback Loop Bandwidth (kHz)	Phase Margin (deg)	R <sub>FB</sub> (kΩ)	PWM Freq (kHz)
12V	1.0V	330μF	22μF x4	None	220μF x8	220	48	52	46	90.9kΩ	500kHz
12V	1.2V	330μF	22μF x4	None	220μF x8	220	53	54	46	60.4kΩ	500kHz
12V	1.5V	330μF	22μF x4	None	220μF x8	150	55	51	55	40.2kΩ	600kHz
12V	1.8V	330μF	22μF x4	None	220μF x8	150	56	50	62	30.2kΩ	600kHz

**25% Load Step (0 to 12.5A, 10A/μs), Bulk + Ceramic Output Capacitor Solutions**

V <sub>IN</sub>	V <sub>OUT</sub>	C <sub>IN</sub> (BULK)	C <sub>IN</sub> (Ceramic)	C <sub>OUT</sub> (BULK)	C <sub>OUT</sub> (MLCC)	C <sub>FF</sub> (pF)	P-P Deviation (mV) <sup>(1)</sup>	Feedback Loop Bandwidth (kHz)	Phase Margin (deg)	R <sub>FB</sub> (kΩ)	PWM Freq (kHz)
12V	1.0V	330μF	22μF x4	470μF x2	220μF x3	100	61	48	63	90.9kΩ	500kHz
12V	1.2V	330μF	22μF x4	470μF x2	220μF x3	100	62	49	64	60.4kΩ	500kHz
12V	1.5V	330μF	22μF x4	470μF x2	220μF x3	100	66	47	76	40.2kΩ	600kHz
12V	1.8V	330μF	22μF x4	470μF x2	220μF x3	100	64	43	82	30.2kΩ	600kHz

1. Worst case.

**Table 8: MxL7225-1 Load Step Response vs. Components, 2-Phase, 1 Output (refer to Figure 35)**

C <sub>IN</sub> (Ceramic)			C <sub>OUT</sub> (Ceramic)			C <sub>OUT</sub> (Bulk)		
Vendors	Value	Part Number	Vendors	Value	Part Number	Vendors	Value	Part Number
Murata	22μF, 16V, X5R, 1210	GRM32ER61C226KE20L	Murata	100μF, 6.3V, X5R, 1210	GRM32ER60J107ME20L	Panasonic	680μF, 2.5V, 6mΩ	2R5TPF680M6L
Murata	22μF, 16V, X5R, 1206	GRM31CR61C226KE15K	Murata	220μF, 6.3V, X5R, 1210	GRM32ER60J227ME05L	Panasonic	470μF, 2.5V, 3mΩ	EEFGX0E471R
TDK	22μF, 16V, X5R, 1210	C3225X5R1C226M250AA	Würth	100μF, 6.3V, X5R, 1210	885012109004			

**25% Load Step (0A to 12.5A, 10A/μs) Ceramic Output Capacitor Only Solutions**

V <sub>IN</sub>	V <sub>OUT</sub>	C <sub>IN</sub> (BULK)	C <sub>IN</sub> (Ceramic)	C <sub>OUT</sub> (BULK)	C <sub>OUT</sub> (MLCC)	C <sub>P</sub> (pF)	R <sub>C</sub> (kΩ)	C <sub>C</sub> (nF)	C <sub>FF</sub> (pF)	P-P Deviation (mV) <sup>(1)</sup>	Feedback Loop Bandwidth (kHz)	Phase Margin (deg)	R <sub>FB</sub> (kΩ)	PWM Freq (kHz)
12V	1V	330μF	22μF x 4	None	220μF x 6	None	3.24	10	68	55	80	45	90.9	500
12V	1.2V	330μF	22μF x 4	None	220μF x 5	None	2.55	10	68	65	79	50	60.4	500
12V	1.5V	330μF	22μF x 4	None	220μF x 4	None	2.55	10	68	70	87	53	40.2	600
12V	1.8V	330μF	22μF x 4	None	220μF x 4	None	2.55	10	68	72	98	60	30.2	600

**25% Load Step (0A to 12.5A, 10A/μs) Bulk + Ceramic Output Capacitor Solutions**

V <sub>IN</sub>	V <sub>OUT</sub>	C <sub>IN</sub> (BULK)	C <sub>IN</sub> (Ceramic)	C <sub>OUT</sub> (BULK)	C <sub>OUT</sub> (MLCC)	C <sub>P</sub> (pF)	R <sub>C</sub> (kΩ)	C <sub>C</sub> (nF)	C <sub>FF</sub> (pF)	P-P Deviation (mV) <sup>(1)</sup>	Feedback Loop Bandwidth (kHz)	Phase Margin (deg)	R <sub>FB</sub> (kΩ)	PWM Freq (kHz)
12V	1V	330μF	22μF x 4	470μF x 2	100μF x 4	None	4.52	4.7	47	52	89	58	90.9	500
12V	1.2V	330μF	22μF x 4	470μF x 2	100μF x 4	None	4.52	4.7	47	58	82	59	60.4	500
12V	1.5V	330μF	22μF x 4	470μF x 2	100μF x 4	None	5.11	4.7	None	64	70	46	40.2	600
12V	1.8V	330μF	22μF x 4	470μF x 2	100μF x 4	None	5.11	4.7	None	68	69	51	30.2	600

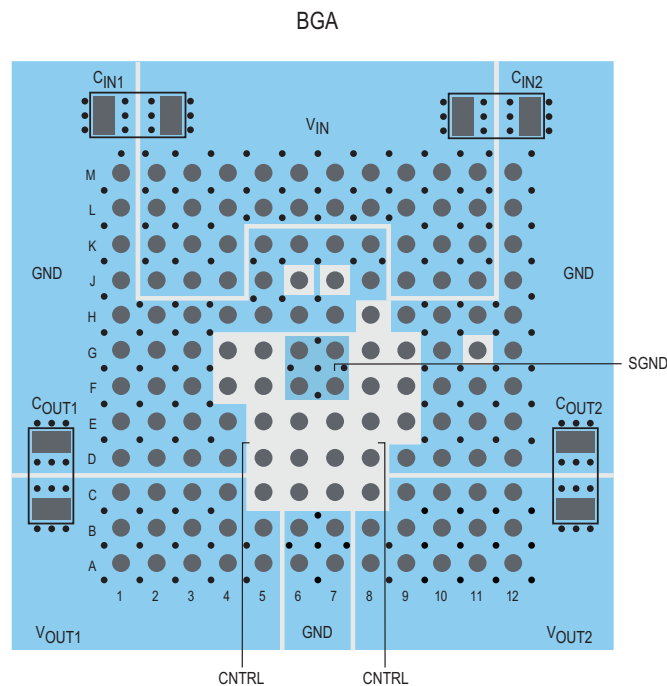
1. Worst case.

## Layout Guidelines and Example

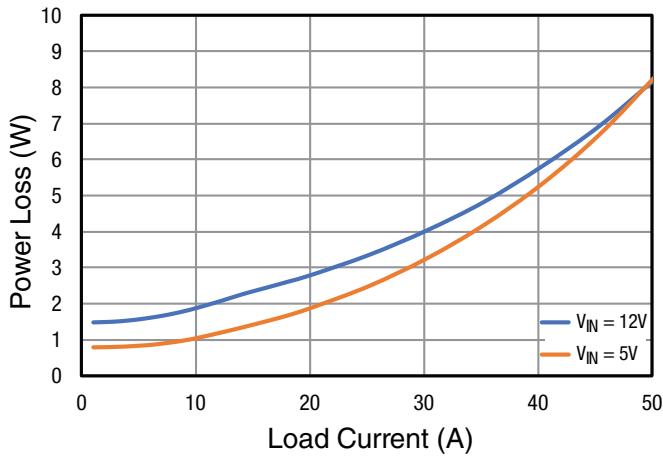
The MxL7225's high level of integration simplifies PCB board design. However, some layout considerations are still recommended for optimal electrical and thermal performance.

- Use large PCB copper areas for high current paths, including  $V_{IN}$ ,  $V_{OUT1}$  and  $V_{OUT2}$  and GND to minimize conduction loss and thermal stress in the PCB.
- Use a dedicated power ground layer, placed under the module.
- Use multiple vias to interconnect the top layer and other power layers to minimize via conduction loss and module thermal stress.
- Cap or plate over any vias that are directly placed on the pad.
- Use a separated SGND ground copper area for components that are connected to the signal pins. The SGND to GND should be connected underneath the module.
- Place high frequency ceramic input and output capacitors next to the  $V_{IN}$ ,  $V_{OUT}$  and PGND pins to minimize high frequency noise.
- When paralleling modules, connect the  $V_{FB}$ ,  $V_{OUT}$ , and COMP pins together closely with an internal layer. For soft-start mode, the TRACK pins may be tied together via a common capacitor.
- Test points can be brought out for monitoring the signal pins. Only bring out signals for testing purposes when absolutely necessary. Keep test points as close as possible to the module, if possible, to minimize chances of noise coupling.
- COMP1 and COMP2 are sensitive nodes. Make every effort to avoid overlapping a COMP trace with a signal that has fast edges, such as the CLKOUT, the synchronization clock, and the SW. If overlapping is unavoidable, place the COMP trace and the fast edge signal on layers that are separated by a ground plane.

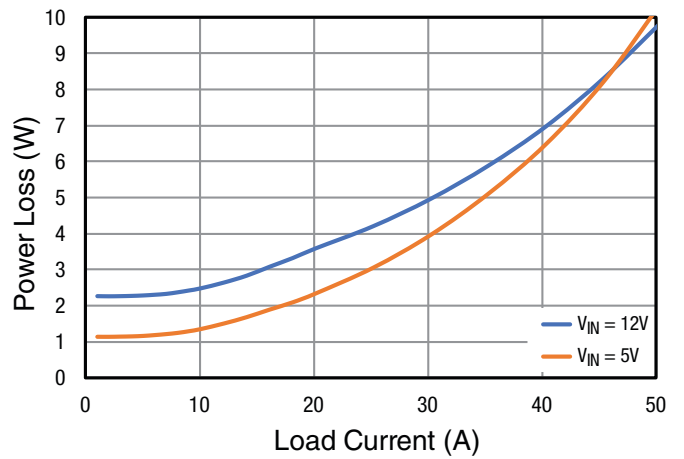
An example layout for the top PCB layer for the BGA package is recommended in [Figure 36](#).



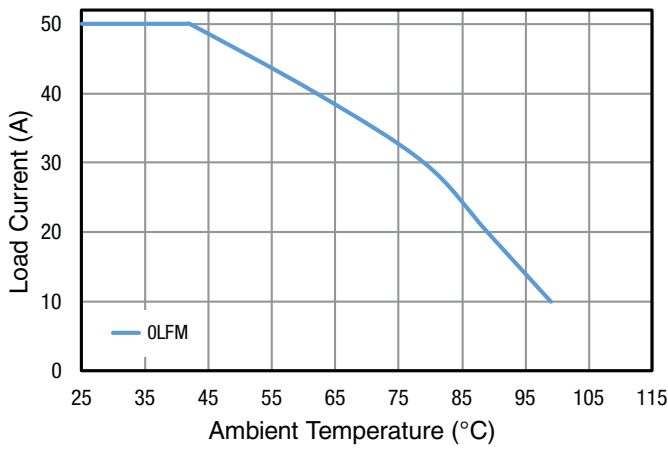
**Figure 36: Recommended PCB Layout**



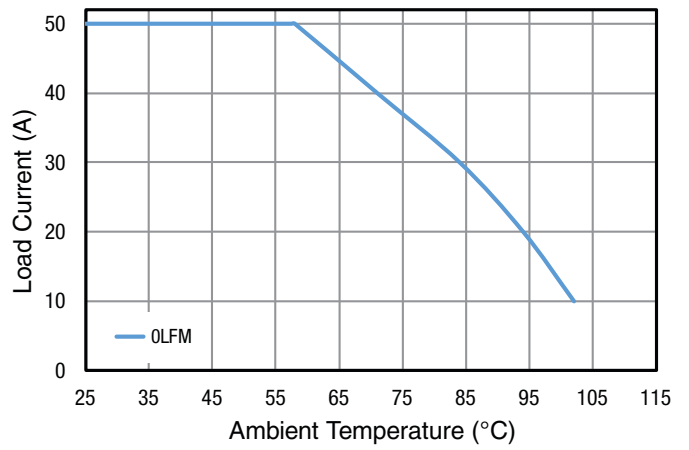
**Figure 37: 0.9V Output Power Loss**



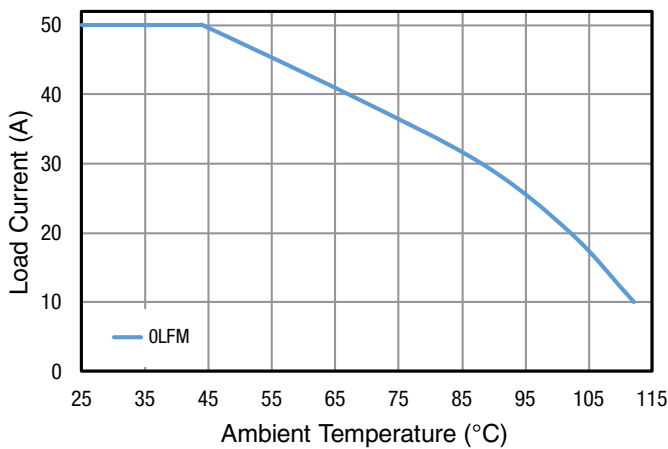
**Figure 38: 1.5V Output Power Loss**



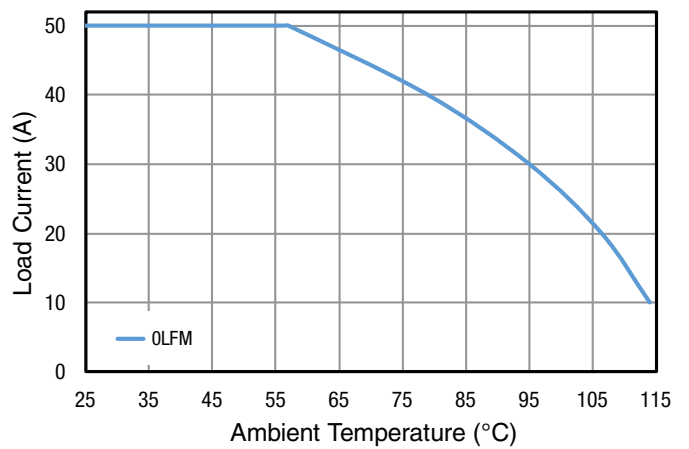
**Figure 39: 12V to 1.5V Current Derating**



**Figure 40: 12V to 0.9V Current Derating**



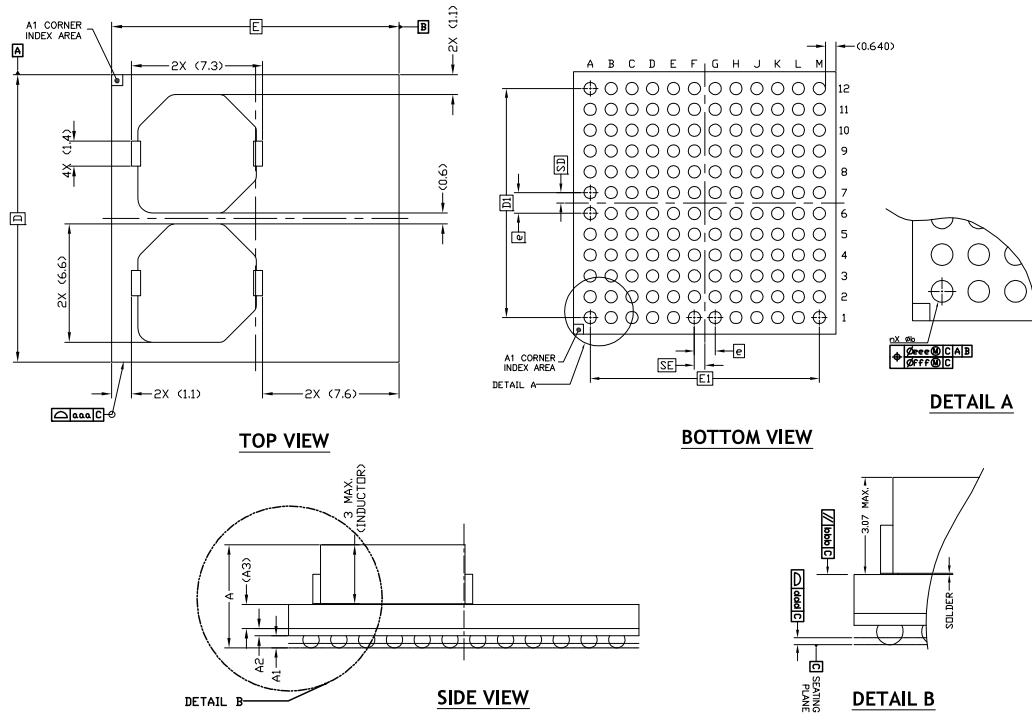
**Figure 41: 5V to 1.5V Current Derating**



**Figure 42: 5V to 0.9V Current Derating**

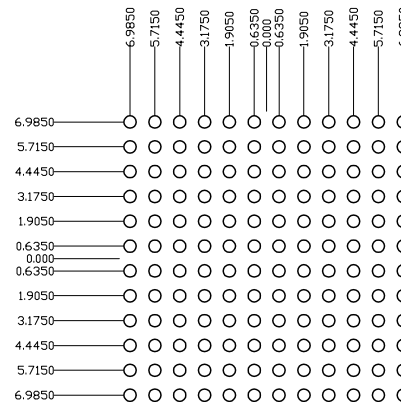
# Mechanical Dimensions

## 16mm x 16mm x 5.01mm BGA



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOM.	MAX.
TOTAL THICKNESS	A	---	4.725	5.21
STAND OFF	A1	0.45	---	0.65
SUBSTRATE THICKNESS	A2	0.295	0.345	0.395
MOULD THICKNESS	A3		1.1	REF
BODY SIZE	D		16	BSC
	E		16	BSC
BALL DIAMETER			0.7	
BALL OPENING		0.55	0.6	0.65
BALL WIDTH	bb	0.6	---	0.9
BALL PITCH	e		1.27	BSC
BALL COUNT	n		144	
EDGE BALL CENTER TO CENTER	DI		13.97	BSC
	E1		13.97	BSC
BODY CENTER TO CONTACT BALL	SD		0.635	BSC
	SE		0.635	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOULD FLATNESS	bbb		0.25	
COPLANARITY	ddd		0.2	
BALL OFFSET (PACKAGE)	eee		0.3	
BALL OFFSET (BALL)	fff		0.15	

TERMINAL DETAILS



PAD LOCATION

NOTE : ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.

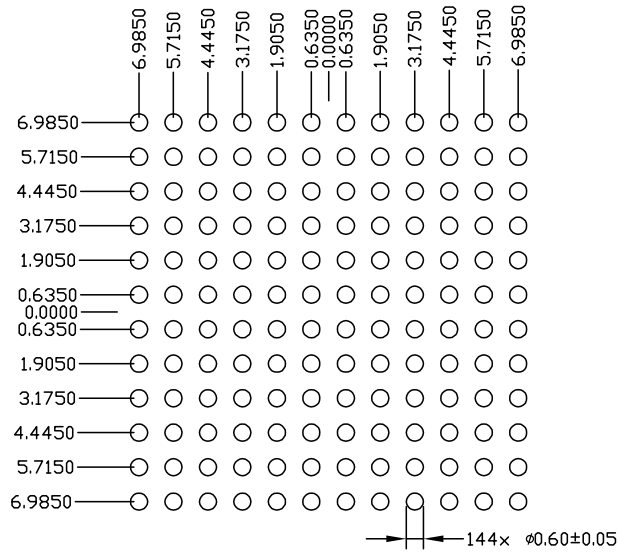
Drawing No.: POD-00000149

Revision: A.1

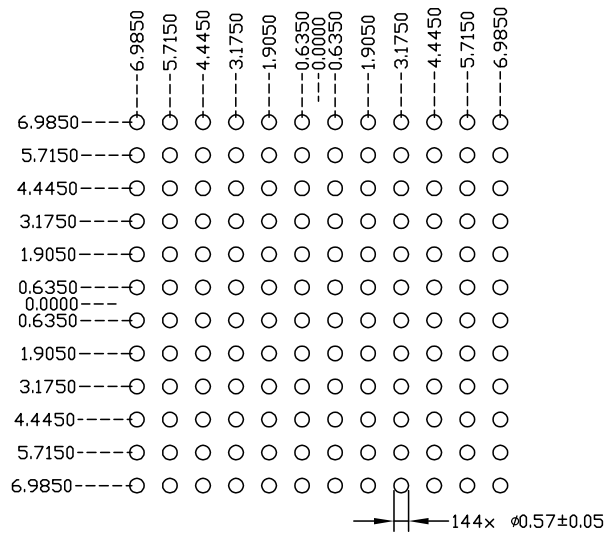
Figure 43: Mechanical Dimensions, BGA

# Recommended Land Pattern and Stencil

## 16mm x 16mm x 5.01mm BGA



**TYPICAL RECOMMENDED LAND PATTERN**



**TYPICAL RECOMMENDED STENCIL**

NOTE : ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.

Drawing No.: POD-00000149

Revision: A.1

**Figure 44: Recommended Land Pattern and Stencil, BGA**



## Module Pinout

**Table 9: Module Pinout**

Pin ID	Function	Pin ID	Function	Pin ID	Function	Pin ID	Function	Pin ID	Function	Pin ID	Function
A1	V <sub>OUT1</sub>	B1	V <sub>OUT1</sub>	C1	V <sub>OUT1</sub>	D1	GND	E1	GND	F1	GND
A2	V <sub>OUT1</sub>	B2	V <sub>OUT1</sub>	C2	V <sub>OUT1</sub>	D2	GND	E2	GND	F2	GND
A3	V <sub>OUT1</sub>	B3	V <sub>OUT1</sub>	C3	V <sub>OUT1</sub>	D3	GND	E3	GND	F3	GND
A4	V <sub>OUT1</sub>	B4	V <sub>OUT1</sub>	C4	V <sub>OUT1</sub>	D4	GND	E4	GND	F4	MODE_PLLIN
A5	V <sub>OUT1</sub>	B5	V <sub>OUT1</sub>	C5	V <sub>OUTS1</sub>	D5	V <sub>FB1</sub>	E5	TRACK1	F5	RUN1
A6	GND	B6	GND	C6	f <sub>SET</sub>	D6	SGND	E6	COMP1	F6	SGND
A7	GND	B7	GND	C7	SGND	D7	V <sub>FB2</sub>	E7	COMP2	F7	SGND
A8	V <sub>OUT2</sub>	B8	V <sub>OUT2</sub>	C8	V <sub>OUTS2</sub>	D8	TRACK2	E8	DIFFP	F8	DIFFOUT
A9	V <sub>OUT2</sub>	B9	V <sub>OUT2</sub>	C9	V <sub>OUT2</sub>	D9	GND	E9	DIFFN	F9	RUN2
A10	V <sub>OUT2</sub>	B10	V <sub>OUT2</sub>	C10	V <sub>OUT2</sub>	D10	GND	E10	GND	F10	GND
A11	V <sub>OUT2</sub>	B11	V <sub>OUT2</sub>	C11	V <sub>OUT2</sub>	D11	GND	E11	GND	F11	GND
A12	V <sub>OUT2</sub>	B12	V <sub>OUT2</sub>	C12	V <sub>OUT2</sub>	D12	GND	E12	GND	F12	GND
G1	GND	H1	GND	J1	GND	K1	GND	L1	GND	M1	GND
G2	SW1	H2	GND	J2	V <sub>IN</sub>	K2	V <sub>IN</sub>	L2	V <sub>IN</sub>	M2	V <sub>IN</sub>
G3	GND	H3	GND	J3	V <sub>IN</sub>	K3	V <sub>IN</sub>	L3	V <sub>IN</sub>	M3	V <sub>IN</sub>
G4	PHASMD	H4	GND	J4	V <sub>IN</sub>	K4	V <sub>IN</sub>	L4	V <sub>IN</sub>	M4	V <sub>IN</sub>
G5	CLKOUT	H5	GND	J5	GND	K5	GND	L5	V <sub>IN</sub>	M5	V <sub>IN</sub>
G6	SGND	H6	GND	J6	TEMP	K6	GND	L6	V <sub>IN</sub>	M6	V <sub>IN</sub>
G7	SGND	H7	GND	J7	EXTV <sub>CC</sub>	K7	GND	L7	V <sub>IN</sub>	M7	V <sub>IN</sub>
G8	PGOOD2	H8	INTV <sub>CC</sub>	J8	GND	K8	GND	L8	V <sub>IN</sub>	M8	V <sub>IN</sub>
G9	PGOOD1	H9	GND	J9	V <sub>IN</sub>	K9	V <sub>IN</sub>	L9	V <sub>IN</sub>	M9	V <sub>IN</sub>
G10	GND	H10	GND	J10	V <sub>IN</sub>	K10	V <sub>IN</sub>	L10	V <sub>IN</sub>	M10	V <sub>IN</sub>
G11	SW2	H11	GND	J11	V <sub>IN</sub>	K11	V <sub>IN</sub>	L11	V <sub>IN</sub>	M11	V <sub>IN</sub>
G12	GND	H12	GND	J12	GND	K12	GND	L12	GND	M12	GND

## Ordering Information

**Table 10: Ordering Information<sup>(1)</sup>**

Ordering Part Number	Operating Temperature Range	MSL Rating	Lead-Free	Package	Packaging Method
MxL7225-ABA-T	-40°C ≤ T <sub>J</sub> ≤ 125°C	3	Yes <sup>(2)</sup>	BGA144 16x16	Tray
MxL7225-1-ABA-T <sup>(3)</sup>					
MxL7225-EVK-1	MxL7225 Evaluation Board, Single Device, Dual Output				
MxL7225-EVK-2	MxL7225 Evaluation Board, 4 Devices, Multiphase				
MxL7225-1-EVK-1	MxL7225-1 Evaluation Board, Single Device, Dual Output				
MxL7225-1-EVK-2	MxL7225-1 Evaluation Board, 4 Devices, Multiphase				

1. Refer to [www.maxlinear.com/MxL7225](http://www.maxlinear.com/MxL7225) for most up-to-date Ordering Information.
2. Visit [www.maxlinear.com](http://www.maxlinear.com) for additional information on Environmental Rating.
3. With external compensation.



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