Description

The F159V is a Dual-Path RF Transmitter IC that has an operating frequency range of 450MHz to 2800MHz. The device provides two independent transmit paths each with 18.3dB typical maximum gain with corresponding output noise floor of -142.5dBm/Hz, +31dBm OIP3, and +14dBm output P1dB designed to operate with a single +3.3V supply while consuming only 685mA DC current.

Each signal path includes a quadrature modulator, voltage variable attenuator (VVA), digital step attenuator (DSA), and a fixed gain amplifier. The device supports a total of 32dB VVA adjustment range using a SPI-controlled 11-bit DAC, and each DSA has 31dB gain control range in 1dB steps using SPI control.

An on-chip frequency synthesizer is shared by both paths and is optimized for use in multi-carrier, multi-mode FDD and TDD base station transmitters achieving GSM-grade performance. The synthesizer offers both an integer mode and fractional mode. It requires an external loop filter and an external reference oscillator in the frequency range of 10MHz to 250MHz.

The F159V is packaged in a 10mm x 10mm, 68-pin QFN with 110Ω differential drive from external I/Q DACs and single-ended 50Ω RF output impedance for ease of integration into the signal-path lineup for each of the two transmitter paths. Each path has independent power supply control thereby allowing optimum power efficiency.

Competitive Advantage

- High level of integration includes frequency synthesizer / PLL, dual-path DSA, Modulator, and VVA
- High reliability
- Low DC current
- *Zero Distortion™* technology
- *GlitchFree™* technology

Typical Applications

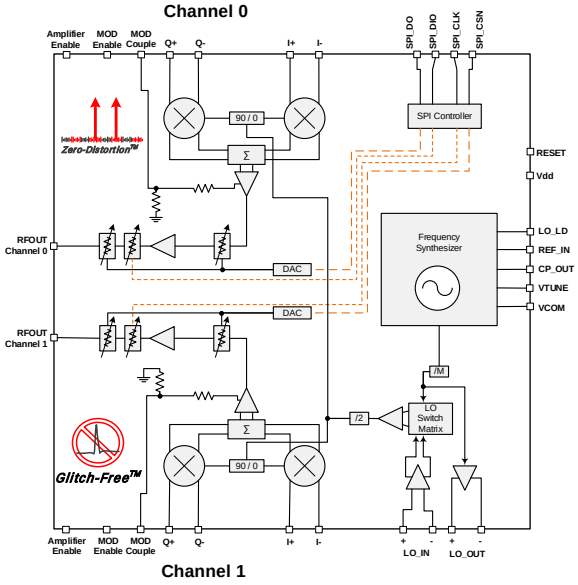
- Application Multi-mode, Multi-carrier Transmitters
- PCS1900 Base Stations
- DCS1800 Base Stations
- WiMAX and LTE Base Stations
- UMTS/WCDMA 3G Base Stations
- PHS/PAS Base Stations
- Distributed Antenna Systems
- Digital Radio

Features

- Independent dual-path operation
- RF output frequency: 450MHz to 2800MHz
- 18.3dB typical maximum gain (no attenuation)
- +31dBm OIP3 (no attenuation)
- +14dBm Output P1dB (no attenuation)
- 13dB NF corresponds to -142.5dBm/Hz output noise floor (no attenuation)
- Output noise floor -152.3dBm/Hz (VVA=14dB, DSA=1dB)
- Channel Isolation: 47dB
- DSA with 31dB total gain range in 1dB steps
- Multiple VVAs with 32dB gain range controlled by on-chip SPI controlled 11-bit DAC
- Variable Gain amplifier (VGA) is comprised of DSAs, VVAs, and a fixed-gain amplifier
- I lead Q by 90 degrees for high side LO injection
- Supports ZIF or CIF architectures
- Common-mode voltage range: +0.1V to +0.8V
- Integer-N and Fractional-N Synthesizer
- Direct 110Ω differential driven from I/Q DAC
- 50Ω single-ended RF output impedance
- Internal or external LO select
- +3.3V supply voltage at 685mA (LO_Out not turned on)
- Specified Case Temperature; -20°C to +115°C
- 10mm x 10mm, 68-pin QFN package

Block Diagram

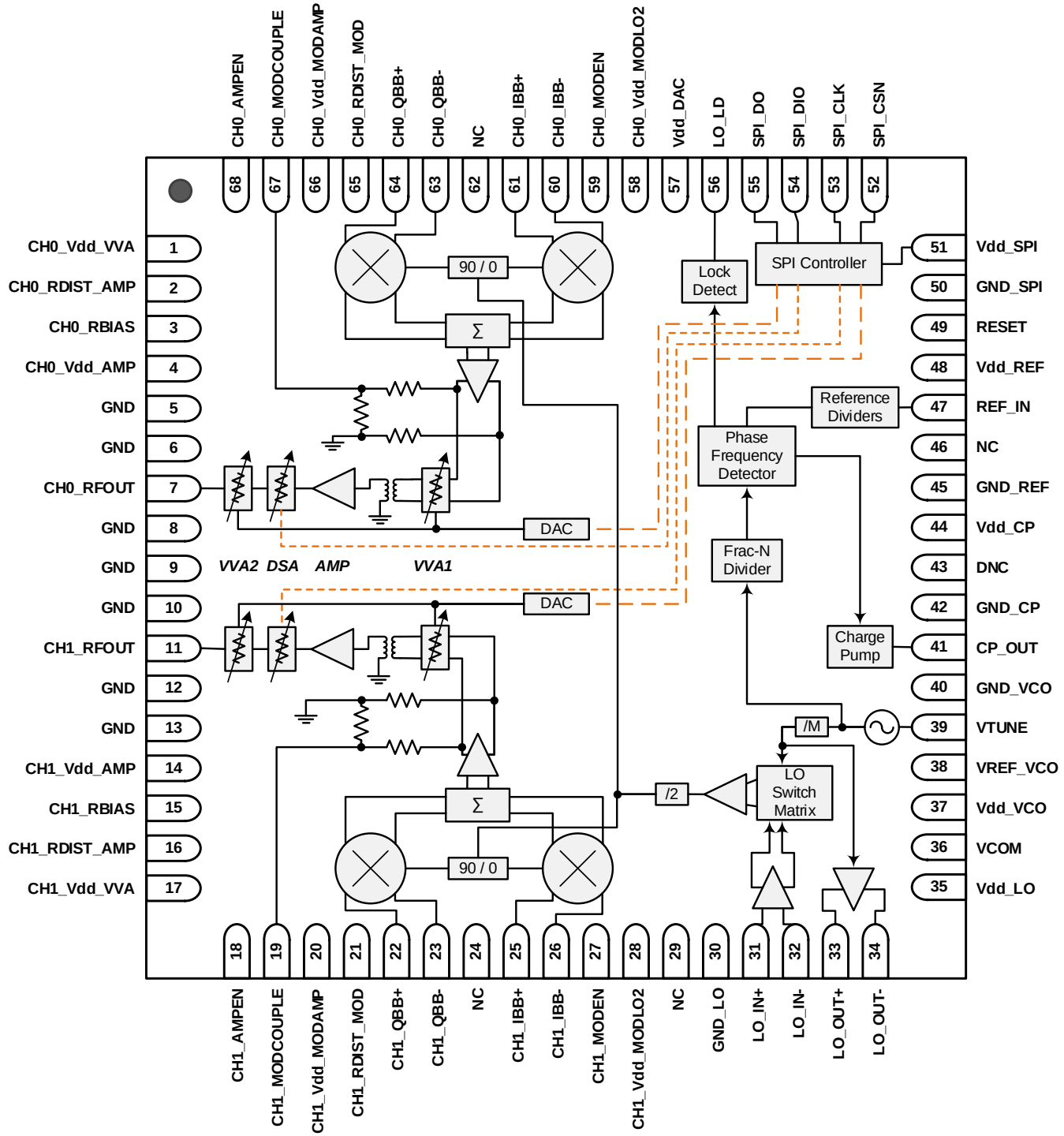
Figure 1. Block Diagram



Contents

1. Pin Assignments

Figure 2. Pin Assignments for 10mm x 10mm x 0.9mm QFN Package – Top View



2. Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Description
1	CH0_Vdd_VVA	Channel 0 voltage variable attenuator (VVA) power supply. Place bypass capacitors to GND as close to this pin as possible.
2	CH0_RDIST_AMP	Channel 0 VGA amplifier distortion bias.
3	CH0_RBIAS	Channel 0 VGA amplifier current bias.
4	CH0_Vdd_AMP	Channel 0 variable gain amplifier (VGA) power supply. Place bypass capacitors to GND as close to this pin as possible.
5	GND	Internally grounded. This pin must be grounded as close to the device as possible.
6	GND	Internally grounded. This pin must be grounded as close to the device as possible.
7	CH0_RFOUT	Channel 0 RF output. Must be AC-coupled.
8	GND	Internally grounded. This pin must be grounded as close to the device as possible.
9	GND	Internally grounded. This pin must be grounded as close to the device as possible.
10	GND	Internally grounded. This pin must be grounded as close to the device as possible.
11	CH1_RFOUT	Channel 1 RF output. Must be AC-coupled.
12	GND	Internally grounded. This pin must be grounded as close to the device as possible.
13	GND	Internally grounded. This pin must be grounded as close to the device as possible.
14	CH1_Vdd_AMP	Channel 1 variable gain amplifier (VGA) power supply. Place bypass capacitors to GND as close to this pin as possible.
15	CH1_RBIAS	Channel 1 VGA amplifier current bias.
16	CH1_RDIST_AMP	Channel 1 VGA amplifier distortion bias.
17	CH1_Vdd_VVA	Channel 1 voltage variable attenuator (VVA) power supply. Place bypass capacitors to GND as close to this pin as possible.
18	CH1_AMPEN	Channel 1 Amplifier Enable / Disable. Logic LOW enable (normal operation); logic HIGH or NC for disable (power down).
19	CH1_MODCOUPLE	Channel 1 modulator coupled output.
20	CH1_Vdd_MODAMP	Channel 1 modulator power supply pin. Place bypass capacitors to GND as close to this pin as possible.
21	CH1_RDIST_MOD	Channel 1 modulator amplifier bias
22	CH1_QBB+	Channel 1 *Quadrature* differential baseband input. Internally matched to 110Ω.
23	CH1_QBB-	
24	NC	No internal connection. This pin can be left unconnected, have a voltage applied, or be connected to ground (recommended).
25	CH1_IBB+	Channel 1 *In-Phase* differential baseband input. Internally matched to 110Ω.
26	CH1_IBB-	

Table 2. Pin Descriptions (Cont.)

Number	Name	Description
27	CH1_MODEN	Enable or disable Channel 1 modulator output. Logic LOW will enable the output (normal operation). Logic HIGH or NC will disable the output (power down).
28	CH1_Vdd_MODLO2	Channel 1 modulator LO driver power supply. Place bypass capacitors to GND as close as possible to the pin.
29	NC	No internal connection. This pin can be left unconnected, have a voltage applied, or be connected to ground (recommended).
30	GND_LO	Internally grounded. This pin must be grounded as close to the device as possible.
31	LO_IN+	Local oscillator (LO) 100Ω differential input. Pins must be AC-coupled.
32	LO_IN-	
33	LO_OUT+	Local oscillator (LO) 100Ω differential output. Pins must be AC-coupled.
34	LO_OUT-	
35	Vdd_LO	Power supply pin. Place bypass capacitors to GND as close as possible to the pin.
36	VCOM	Requires a capacitor from this pin to Vdd_VCO or to VREF_VCO for noise reduction.
37	Vdd_VCO	Power Supply Voltage. Place bypass capacitors to GND as close as possible to the pin.
38	VREF_VCO	Place decoupling capacitors (≥ 0.1µF) to ground, as close to the pin as possible. This pin indicates voltage 2.8V when part is turned on.
39	VTUNE	Voltage control input to tune the VCO.
40	GND_VCO	Internally grounded. This pin must be grounded as close to the device as possible.
41	CP_OUT	Charge Pump Output. When enabled, this output provides ± ICP to the external loop filter. The output of the loop filter is connected to VTUNE to drive the internal VCO.
42	GND_CP	Internally grounded. This pin must be grounded as close to the device as possible.
43	DNC	Do not connect anything to this pin.
44	Vdd_CP	Charge Pump Power Supply. Vdd_CP must have the same value as Vdd. Place decoupling capacitors to the ground plane as close to this pin as possible.
45	GND_REF	Internally grounded. This pin must be grounded as close to the device as possible.
46	NC	No internal connection. This pin can be left unconnected, have a voltage applied, or be connected to ground (recommended).
47	REF_IN	Reference Input. This CMOS input has a nominal threshold of Vdd/2 and a DC equivalent input resistance of 100kΩ. This input can be driven from a TTL or CMOS crystal oscillator, or it can be AC-coupled.
48	Vdd_REF	Power supply for reference path. Place bypass capacitors to GND as close as possible to the pin.
49	RESET	HIGH: Reset PLL. Resets all settings to default. LOW: Normal Operating
50	GND_SPI	Internally grounded. This pin must be grounded as close to the device as possible.
51	Vdd_SPI	SPI power supply pin. Place bypass capacitors to GND as close to this pin as possible.
52	SPI_CSN	Serial chip Select. CSN pin can be pulled up to Vdd and down to GND.
53	SPI_CLK	Serial Clock Input.
54	SPI_DIO	Data write/read of 3-wire serial interface.

Table 3. Pin Descriptions (Cont.)

Number	Name	Description
55	SPI_DO	Data read of 4-wire serial interface.
56	LO_LD	LO Lock Detect output. Logic HIGH indicates PLL lock. Logic LOW indicates loss of PLL lock.
57	Vdd_DAC	Power supply for DACs. Place bypass capacitors to GND as close as possible to the pin.
58	CH0_Vdd_MODLO2	Channel 0 modulator LO driver power supply. Place bypass capacitors to GND as close as possible to the pin.
59	CH0_MODEN	Channel 0 modulator Enable / Disable. Logic LOW enable (normal operation); logic HIGH or NC for disable (power down).
60	CH0_IBB-	Channel 0 *In-Phase* differential baseband input. Internally matched to 110Ω.
61	CH0_IBB+	
62	NC	No internal connection. This pin can be left unconnected, have a voltage applied, or be connected to ground (recommended).
63	CH0_QBB-	Channel 0 *Quadrature* differential baseband input. Internally matched to 110Ω.
64	CH0_QBB+	
65	CH0_RDIST_MOD	Channel 0 modulator amplifier bias.
66	CH0_Vdd_MODAMP	Channel 0 modulator power supply pin. Place bypass capacitors to GND as close to this pin as possible.
67	CH0_MODCOUPLE	Channel 0 modulator coupled output.
68	CH0_AMPEN	Enable or disable Channel 0 modulator output. Logic LOW will enable the output (normal operation). Logic HIGH or NC will disable the output (power down).
	-EPAD	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the noted RF performance.

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the F159V at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
All V_{DD} pins to GND	V_{DD}	-0.3	+3.6	V
SPI_DIO, SPI_CLK, SPI_DO, SPI_CSN, LO_LD	$VSPI_{Logic}$	-0.3	V_{DD} + 0.25	V
CH0_MODEN, CH1_MODEN, CH0_AMPEN, CH1_AMPEN	$VEnable_{Logic}$	-0.3	V_{DD} + 0.25	V
CH0_RDIST_AMP, CH1_RDIST_AMP	V_{RDIST}	-0.3	0.3	V
CH0_RBIAS, CH1_RBIAS	V_{RBIAS}	-0.3	1	V
CH0_MODCOUPLE, CH1_MODCOUPLE	V_{MODOUT}	-0.3	V_{DD} + 0.25	V
CH0_RDIST_MOD, CH1_RDIST_MOD	V_{RDIST_MOD}	-0.3	0.6	V
CH0_QBB+, CH0_QBB-, CH0_IBB+, CH0_IBB- CH1_QBB+, CH1_QBB-, CH1_IBB+, CH1_IBB-	V_{BBIQ}	-0.3	1.8	V
LO_IN-, LO_IN+, LO_OUT-, LO_OUT+	V_{LO}	-0.3	V_{DD} + 0.25	V
REF_IN, CP_OUT, VTUNE	V_{LOGIC}	-0.3	V_{DD} + 0.25	V
CH0_RFOUT, CH1_RFOUT externally applied DC voltage	V_{RFOUT}	0	1.8	V
RESET	V_{RESET}	-0.3	V_{DD} + 0.25	V
VCOM	V_{VCOM}	-0.3	V_{DD} + 0.25	V
VREF_VCO	V_{REFVCO}	-0.3	V_{DD} + 0.25	V
Continuous Power Dissipation	P_{diss}		2.7	W
Junction Temperature	T_J		+150	°C
Storage Temperature Range	T_{STOR}	-65	+150	°C
Lead Temperature (soldering, 10s)			+260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)	V_{ESDHBM}		1000 (Class 1C)	V
Electrostatic Discharge – CDM (JEDEC 22-C101F)	V_{ESDCDM}		750 (Class C2)	V

4. Recommended Operating Conditions

Table 5. Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Supply Voltage(s)	V_{DD}	All V_{DD} pins	3.15	3.3	3.45	V
Operating Temperature Range [a]	T_{EP}	Exposed Paddle Temperature	-20	+25	+115	°C
Min/Max VCO Tuning Voltage	VCO_{VOLT1}	Auto-calibration off	0.15		3.15	V
	VCO_{VOLT2}	Auto-calibration on	0.35		2.95	
Baseband Input Frequency Range	f_{BB}	Based on RF Power degraded from Maximum Gain to Minimum Gain	DC		600	MHz
LO Input Frequency Range [b]	f_{LO}		450		2800	MHz
LO Input Power	P_{LO}		-8		0	dBm
RF Output Frequency Range [b]	f_{RF}		450		2800	MHz
Baseband Common Mode Voltage	V_{CM}	T_{EP} = -20°C to +115°C	0.1	0.325	0.8	V
Baseband Input Voltage Compliance Range	V_{BB}	Each baseband pin	0		1	Vpeak
Baseband Input Port Impedance	Z_{BB0I_IN} Z_{BB1I_IN} Z_{BB0Q_IN} Z_{BB1Q_IN}	Differential		110		Ω
LO Input Port Impedance	Z_{LO_IN}	Differential		100		Ω
LO Output Port Impedance	Z_{LO_OUT}	Differential		100		Ω
RF Output Impedance	Z_{RFO}	Single Ended		50		Ω
Modulator Output Impedance	Z_{MODO}	Single Ended		50		Ω

[a] On startup of the device, the temperature can be as low as -40°C. Device will not lose PLL lock with auto-calibration on after it warms up. Device functions normally but not specified for temperatures below -20°C.

[b] Expect a slight performance degradation from 600MHz to 450MHz.

5. Electrical Characteristics

Table 6. General Characteristics

See the F159V Typical Application Circuit. Operated as a dual-path transmitter, V_{DD} = +3.3V, Internal f_{LO} = 2050MHz to generate f_{RF} = 2000MHz, LO_SW_OUT= +4dBm setting, T_{EP} = +25°C, maximum gain setting, all Enable pins = GND, BB_IQ frequency = 49MHz or 50MHz, I leads Q by 90 degrees, BB_I&Q levels = 100mVp-p each tone differential, I and Q = 0.325V common-mode bias, Z_{BB_DIFF} = 110Ω, Z_{RFO} = 50Ω, parameters measured at RF output, Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
DC						
Logic Input HIGH	V_{IH}	JEDEC 1.8 and JEDEC 3.3	*+1.1 [a]*		*V_{DD} + 0.25*	V
Logic Input LOW	V_{IL}	JEDEC 1.8 and JEDEC 3.3	*0.0*		*+0.6*	V
Logic Output High	$V_{OH\_1.8}$	JEDEC 1.8	*+1.4*		*+2.1*	V
	$V_{OH\_3.3}$	JEDEC 3.3	*+2.0*		*+3.6*	
Logic Output Low	$V_{OL\_1.8}$	JEDEC 1.8	*0.0*		*+0.4*	V
	$V_{OL\_3.3}$	JEDEC 3.3	*0.0*		*+0.66*	
Logic Current – High Logic	I_{IH}		*-100*		*100*	µA
Logic Current – Low Logic	I_{IL}		*-100*		*100*	µA
Supply Current – Both paths [b]	I_{DD_PLL}	Frequency Synthesizer		132	*170*	mA
	I_{DD_LO}	External LO Driver at maximum LO_buffer gain		33	*40*	
	I_{DD_2MOD}	2 modulators		387	*450*	
	I_{DD_2AMP}	2 VGAs		153	*183*	
	I_{DD_DAC}	2 DACs		14	*17*	
	$I_{DD\_Enable2}$	Standby Mode dual path		51		
Supply Current – One path [b]	I_{DD_PLL}	Frequency Synthesizer		132	*170*	mA
	I_{DD_LO}	External LO Driver at maximum LO_buffer gain		33	*40*	
	I_{DD_1MOD}	1 modulator		194	*235*	
	I_{DD_1AMP}	1 VGA		79	*95*	
	I_{DD_DAC}	2 DACs		14	*17*	
Charge Pump Current	I_{CP}	Programmable in ~0.3mA steps	*0.2*		*6*	mA
General						
LO output power	LOP_{out}	LO_OUT Setting = +4dBm	*-2*		*+4*	dBm
External LO input Return Loss	RL_{LO_IN}	Differential 100Ω	8	15		dB
External LO output Return Loss	RL_{LO_OUT}	Differential 100Ω	10	15		dB
SPI						
Serial Clock Speed	SPI_{CLK}				*20*	MHz

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

[b] Values valid for CP current set to 0.94mA, LO_SW_OUT = 0dBm.

Table 7. Electrical Characteristics

See the F159V Typical Application Circuit. Operated as a dual-path transmitter, V_{DD} = +3.3V, Internal f_{LO} = 2050MHz to generate f_{RF} = 2000MHz, LO_SW_OUT= +4dBm setting, T_{EP} = +25°C, maximum gain setting, all Enable pins = GND, BB_IQ frequency = 49MHz or 50MHz, I leads Q by 90 degrees, BB_I&Q levels = 100mVp-p each tone differential, I and Q = 0.325V common-mode bias, Z_{BB_DIFF} = 110Ω, Z_{RFO} = 50Ω, parameters measured at RF output, Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Digital Step Attenuator						
DSA adjustment range	G_{DSA}			31		dB
DSA step	$G_{DSASTEP}$			1		dB
Max DSA Glitching	$ATTN_G$	During DSA state change		+2 / -2.3		dB
Gain Accuracy	DSA_{ACCMAX}	Gain Error vs. line (A_{MIN} ref)	± (0.05 + 5% ATTN value)			dB
Relative Phase Shift	DSA_PH	Worst case 4dB step		4		Deg
		Worst case 8dB step		6		
		f_{RF} = 2.8GHz Worst case 2dB step		4		
DSA Gain Settling Time	DSA_{ST}	0dB to Max attenuation Maximum attenuation to 0dB End DSA register configuration to output within 0.1dB		1	2	µs
Voltage Variable Attenuator						
VVA adjustment range	G_{VVA}	DAC input 0 for maximum attenuation 2047 for minimum attenuation	***26*** [a]	32		dB
VVA step	$G_{VVASTEP}$	Using on-chip 11-bit DAC		0.02		dB
Relative Phase Shift	VVA_{PHASE}	Worst case 2dB step		4		Deg
Relative Error	VVA_{ERROR}	Gain variation from DAC code 250 to 1750 relative to typical gain variation	-2		2	dB
Settling Time to within 0.1dB	$T_{SETTL0.1dB}$	Any 1dB step Includes DAC + VVA response		0.40		µs

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

Table 8. Electrical Characteristics (Cont.)

See the F159V Typical Application Circuit. Operated as a dual-path transmitter, V_{DD} = +3.3V, Internal f_{LO} = 2050MHz to generate f_{RF} = 2000MHz, LO_SW_OUT= +4dBm setting, T_{EP} = +25°C, maximum gain setting, all Enable pins = GND, BB_IQ frequency = 49MHz or 50MHz, I leads Q by 90 degrees, BB_I&Q levels = 100mVp-p each tone differential, I and Q = 0.325V common-mode bias, Z_{BB_DIFF} = 110Ω, Z_{RFO} = 50Ω, parameters measured at RF output, Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Modulator Stage						
Modulator power coupled output	P_{M_OUT}	BB input = 210mVp-p differential Modulator output Maximum VVA & DSA attenuation	***-31*** [a]	-28		dBm
P1dB at Modulator coupled output	$OP1dB_{M\_OUT}$	Maximum VVA & DSA attenuation	***-9***	-6		dBm
IP3 at Modulator coupled output	$OIP3_{M\_OUT}$	BB input = 210mVp-p differential per tone Maximum VVA & DSA attenuation		10.7		dBm
$f_{LO} \pm 2*f_{BB}$ Rejection	$2BB_{REJ\_CPL}$	$f_{BB} \leq$ 100MHz Mod output coupled node BB input = 210mVp-p differential Maximum VVA & DSA attenuation		-82	-50	dBc
$f_{LO} \pm 3*f_{BB}$ Rejection	$3BB_{REJ\_CPL}$	$f_{BB} \leq$ 100MHz Mod output coupled node BB input = 210mVp-p differential Maximum VVA & DSA attenuation		-80	-50	dBc
$f_{LO} \pm 5*f_{BB}$ Rejection	$5BB_{REJ\_CPL}$	$F_{BB} \leq$ 100MHz Mod output coupled node BB input = 210mVp-p differential Maximum VVA & DSA attenuation		-96		dBc
Turn-on time	P_{ON}	Enable = LOW to HIGH. Power is within 0.05dB of final power		0.6		µs
Turn off time	P_{OFF}	Enable = HIGH to LOW. Power is -30dBc from initial output power		0.1		µs
Cascaded VGA						
Turn-on time	P_{ON}	Enable = LOW to HIGH. Power is within 0.05dB of final power		0.8		µs
Turn off time	P_{OFF}	Enable = HIGH to LOW. Power is -30dBc from initial output power		0.1		µs

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

Table 9. Electrical Characteristics – Frequency Synthesizer

See the F159V Typical Application Circuit. Operated as a dual-path transmitter, V_{DD} = +3.3V, Internal f_{LO} = 2050MHz to generate f_{RF} = 2000MHz, LO_SW_OUT= +4dBm setting, T_{EP} = +25°C, maximum gain setting, all Enable pins = GND, BB_IQ frequency = 49MHz or 50MHz, I leads Q by 90 degrees, BB_I&Q levels = 100mVp-p each tone differential, I and Q = 0.325V common-mode bias, Z_{BB_DIFF} = 110Ω, Z_{RFO} = 50Ω, parameters measured at RF output, Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

Synthesizer conditions include: PLL Ref = 30.72MHz, CP current = 0.63mA, LO_OUT power = +4dBm, Cal_LoPN_Mode = 0, Ref Doubler = ON, Reference Divider is set for 1. Synthesizer performance will be evaluated at the LO output pins. The evaluation board and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Frequency Synthesizer / VCO						
Synthesizer Output Frequency	$F_{RFSYNTH\_OUT}$	Divider values; 1, 2, 4, 8	***450*** [a]		***2800***	MHz
Input Reference Frequency [b]	F_{REF_IN}		***10***	30.72	***250***	MHz
PLL Reference Input Level	V_{REF_pp}	Single-ended, peak-peak AC coupled	***0.7***		***3.3***	V
VCO Frequency	F_{VCO}	Fundamental VCO Mode	***2000***		***4000***	MHz
Maximum Lock Time	T_{LOCK}	Includes SPI configuration time using a 10MHz SPI		360		µs
Power-up Time	$T_{POWERUP}$	End of SPI configuration to LO_LD logic high		1.25		ms
Spurs (non-harmonics)	$SPUR_1$	100kHz – 30MHz offset		< -90		dBc
	$SPUR_2$	>30MHz offset		< -90		
PLL Phase Noise Performance LO = 942.5MHz (Use internal VCO at 3770MHz and divide by 4)	PN_200K	200kHz offset		-97		dBc/Hz
	PN_400K	400kHz offset		-126		
	PN_600K	600kHz offset		-136		
	PN_1.2M	1.2MHz offset		-140		
	PN_1.8M	1.8MHz offset		-146		
	PN_6M	6.0MHz offset		-152		
PLL Phase Noise Performance LO = 1847.5MHz (Use internal VCO at 3695MHz and divide by 2)	PN_200K	200kHz offset		-94		dBc/Hz
	PN_400K	400kHz offset		-123		
	PN_600K	600kHz offset		-131		
	PN_1.2M	1.2MHz offset		-137		
	PN_1.8M	1.8MHz offset		-141		
	PN_6M	6.0MHz offset		-150		

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

[b] When input reference frequency is between 10MHz and 20MHz, the reference doubler must be turned on.

Table 10. Electrical Characteristics – Frequency Synthesizer (Cont.)

See the F159V Typical Application Circuit. Operated as a dual-path transmitter, V_{DD} = +3.3V, Internal f_{LO} = 2050MHz to generate f_{RF} = 2000MHz, LO_SW_OUT= +4dBm setting, T_{EP} = +25°C, maximum gain setting, all Enable pins = GND, BB_IQ frequency = 49MHz or 50MHz, I leads Q by 90 degrees, BB_I&Q levels = 100mVp-p each tone differential, I and Q = 0.325V common-mode bias, Z_{BB_DIFF} = 110Ω, Z_{RFO} = 50Ω, parameters measured at RF output, Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

Synthesizer conditions include: PLL Ref = 30.72MHz, CP current = 0.63mA, LO_OUT power = +4dBm, Cal_LoPN_Mode = 0, Reference Doubler = ON, Reference Divider is set for 1. Synthesizer performance will be evaluated at the LO output pins. The evaluation board and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
PLL Phase Noise Performance LO = 2155MHz (Use internal VCO frequency at 2155MHz and divide by 1)	PN_2.1M	2.1MHz offset		-138		dBc/Hz
	PN_3.5M	3.5MHz offset		-143		
	PN_7.5M	7.5MHz offset		-152		
PLL Phase Noise Performance LO = 2655MHz (Use internal VCO frequency at 2655MHz and divide by 1)	PN_2.1M	2.1MHz offset		-138		dBc/Hz
	PN_3.5M	3.5MHz offset		-143		
	PN_7.5M	7.5MHz offset		-151		

Table 11. Electrical Characteristics – Signal Path Cascaded Performance

See the F159V Typical Application Circuit. Operated as a dual-path transmitter, V_{DD} = +3.3V, Internal f_{LO} = 2050MHz to generate f_{RF} = 2000MHz, LO_SW_OUT= +4dBm setting, T_{EP} = +25°C, maximum gain setting, all Enable pins = GND, BB_IQ frequency = 49MHz or 50MHz, I leads Q by 90 degrees, BB_I&Q levels = 100mVp-p each tone differential, I and Q = 0.325V common-mode bias, Z_{BB_DIFF} = 110Ω, Z_{RFO} = 50Ω, parameters measured at RF output, Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Power Gain	PGain max	Input power is sum of I + Q For BB_I = BB_Q = 94mVp-p differential each, total power = -17dBm	***16*** [a]	18.3	***21***	dB
	PGain min			-45		
Gain Variation	$G_{VAR\_\Delta T}$	T_{EP} from -20°C to +115°C		-1 to +0.5		dB
Gain Flatness	G_{FLAT}	1400MHz to 2700MHz measured using 100MHz steps		0.0021	0.005	dB/MHz
Power Gain at 450MHz RF	G_{450}	f_{RF} = 450MHz f_{LO} = 500MHz		13.5		dB

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

Table 12. Electrical Characteristics – Signal Path Cascaded Noise Figure Performance

See the F159V Typical Application Circuit. Operated as a dual-path transmitter, V_{DD} = +3.3V, Internal f_{LO} = 2050MHz to generate f_{RF} = 2000MHz, LO_SW_OUT= +4dBm setting, T_{EP} = +25°C, maximum gain setting, all Enable pins = GND, BB_IQ frequency = 49MHz or 50MHz, I leads Q by 90 degrees, BB_I&Q levels = 100mVp-p each tone differential, I and Q = 0.325V common-mode bias, Z_{BB_DIFF} = 110Ω, Z_{RFO} = 50Ω, parameters measured at RF output, Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Noise Figure	NF_{GMAX}	No attenuation		13.0	14.3 [a]	dB
	NF_{G-15}	VVA 14dB attenuation DSA 1dB attenuation		17.9	19.7	
	NF_{G-19}	VVA 14dB attenuation DSA 5dB attenuation		21.4		
	NF_{G-31}	VVA 14dB attenuation DSA 17dB attenuation		23.3		
	NF_{G-40}	VVA 14dB attenuation DSA 26dB attenuation		23.6		
	NF_{G-6}	VVA 5dB attenuation DSA 1dB attenuation T_{EP} = +115°C		15.5	16.8	
	NF_{G-10}	VVA 5dB attenuation DSA 5dB attenuation T_{EP} = +115°C		16.9		
	NF_{G-22}	VVA 5dB attenuation DSA 17dB attenuation T_{EP} = +115°C		18		
	NF_{G-31}	VVA 5dB attenuation DSA 26dB attenuation T_{EP} = +115°C		19.6		
	NF_{G-23}	VVA 22dB attenuation DSA 1dB attenuation T_{EP} = -20°C		19.7	21.2	
	NF_{G-27}	VVA 22dB attenuation DSA 5dB attenuation T_{EP} = -20°C		23		
	NF_{G-39}	VVA 22dB attenuation DSA 17dB attenuation T_{EP} = -20°C		24.8		
	NF_{G-48}	VVA 22dB attenuation DSA 26dB attenuation T_{EP} = -20°C		30.4		
Output Noise Floor	NFloor	VVA 14dB attenuation DSA 1dB attenuation		-152.3		dBm/Hz

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

Table 13. Electrical Characteristics – Signal Path Cascaded IP3 Performance

See the F159V Typical Application Circuit. Operated as a dual-path transmitter, V_{DD} = +3.3V, Internal f_{LO} = 2050MHz to generate f_{RF} = 2000MHz, LO_SW_OUT= +4dBm setting, T_{EP} = +25°C, maximum gain setting, all Enable pins = GND, BB_IQ frequency = 49MHz or 50MHz, I leads Q by 90 degrees, BB_I&Q levels = 100mVp-p each tone differential, I and Q = 0.325V common-mode bias, Z_{BB_DIFF} = 110Ω, Z_{RFO} = 50Ω, parameters measured at RF output, Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Output IP3 f_{LO} = 900MHz f_{RF} = 850MHz	$OIP3_1$	VVA 14dB attenuation DSA 1dB attenuation P_{IN} = -13dBm/tone		28.6		dBm
Output IP3 f_{LO} = 2050MHz f_{RF} = 2000MHz	$OIP3_2$	No attenuation		31		dBm
	$OIP3_{G-15}$	VVA 14dB attenuation DSA 1dB attenuation P_{IN} = -13dBm/tone	***25*** [a]	31		
	$OIP3_{G-19}$	VVA 14dB attenuation DSA 5dB attenuation P_{IN} = -9dBm/tone		28.4		
	$OIP3_{G-31}$	VVA 14dB attenuation DSA 17dB attenuation P_{IN} = -9dBm/tone		16.4		
	$OIP3_{G-40}$	VVA 14dB attenuation DSA 26dB attenuation P_{IN} = -9dBm/tone		6.8		
	$OIP3_{G-6}$	VVA 5dB attenuation DSA 1dB attenuation P_{IN} = -13dBm/tone T_{EP} = +115°C		25		
	$OIP3_{G-10}$	VVA 5dB attenuation DSA 5dB attenuation P_{IN} = -9dBm/tone T_{EP} = +115°C		25		
	$OIP3_{G-22}$	VVA 5dB attenuation DSA 17dB attenuation P_{IN} = -9dBm/tone T_{EP} = +115°C		16.4		
	$OIP3_{G-31}$	VVA 5dB attenuation DSA 26dB attenuation P_{IN} = -9dBm/tone T_{EP} = +115°C		7.4		
	$OIP3_{G-23}$	VVA 22dB attenuation DSA 1dB attenuation P_{IN} = -13dBm/tone T_{EP} = -20°C		19		

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

Table 14. Electrical Characteristics – Signal Path Cascaded IP3 Performance (Cont.)

See the F159V Typical Application Circuit. Operated as a dual-path transmitter, V_{DD} = +3.3V, Internal f_{LO} = 2050MHz to generate f_{RF} = 2000MHz, LO_SW_OUT= +4dBm setting, T_{EP} = +25°C, maximum gain setting, all Enable pins = GND, BB_IQ frequency = 49MHz or 50MHz, I leads Q by 90 degrees, BB_I&Q levels = 100mVp-p each tone differential, I and Q = 0.325V common-mode bias, Z_{BB_DIFF} = 110Ω, Z_{RFO} = 50Ω, parameters measured at RF output, Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Output IP3 f_{LO} = 2050MHz f_{RF} = 2000MHz	$OIP3_{G-27}$	VVA 22dB attenuation DSA 5dB attenuation P_{IN} = -9dBm/tone T_{EP} = -20°C		20.4		dBm
	$OIP3_{G-39}$	VVA 22dB attenuation DSA 17dB attenuation P_{IN} = -9dBm/tone T_{EP} = -20°C		8.7		
	$OIP3_{G-48}$	VVA 22dB attenuation DSA 26dB attenuation P_{IN} = -9dBm/tone T_{EP} = -20°C		-2		
Output IP3 f_{LO} = 2750MHz f_{RF} = 2700MHz	$OIP3_{G-15}$	VVA 14dB attenuation DSA 1dB attenuation P_{IN} = -13dBm/tone		28		dBm
Output IP3 f_{LO} = 500MHz f_{RF} = 450MHz	$OIP3_{450}$	VVA 14dB attenuation DSA 1dB attenuation P_{IN} = -13dBm/tone		28		dBm

Table 15. Electrical Characteristics – Signal Path Cascaded P1dB Performance

See the F159V Typical Application Circuit. Operated as a dual-path transmitter, V_{DD} = +3.3V, Internal f_{LO} = 2050MHz to generate f_{RF} = 2000MHz, LO_SW_OUT= +4dBm setting, T_{EP} = +25°C, maximum gain setting, all Enable pins = GND, BB_IQ frequency = 49MHz or 50MHz, I leads Q by 90 degrees, BB_I&Q levels = 100mVp-p each tone differential, I and Q = 0.325V common-mode bias, Z_{BB_DIFF} = 110Ω, Z_{RFO} = 50Ω, parameters measured at RF output, Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Output P1dB f_{LO} = 2050MHz f_{RF} = 2000MHz	$OP1dB_1$	No attenuation		14		dBm
	$OP1dB_{G-15}$	VVA 14dB attenuation DSA 1dB attenuation	***10*** [a]	12		
	$OP1dB_{G-19}$	VVA 14dB attenuation DSA 5dB attenuation		11.2		
	$OP1dB_{G-31}$	VVA 14dB attenuation DSA 17dB attenuation		-0.8		
	$OP1dB_{G-40}$	VVA 14dB attenuation DSA 26dB attenuation		-10		
	$OP1dB_{G-6}$	VVA 5dB attenuation DSA 1dB attenuation T_{EP} = +115°C		12.6		
	$OP1dB_{G-10}$	VVA 5dB attenuation DSA 5dB attenuation T_{EP} = +115°C		12.6		
	$OP1dB_{G-22}$	VVA 5dB attenuation DSA 17dB attenuation T_{EP} = +115°C		2.8		
	$OP1dB_{G-31}$	VVA 5dB attenuation DSA 26dB attenuation T_{EP} = +115°C		-6.2		
	$OP1dB_{G-23}$	VVA 22dB attenuation DSA 1dB attenuation T_{EP} = -20°C		6.6		
	$OP1dB_{G-27}$	VVA 22dB attenuation DSA 5dB attenuation T_{EP} = -20°C		2.9		
	$OP1dB_{G-39}$	VVA 22dB attenuation DSA 17dB attenuation T_{EP} = -20°C		-9.4		
	$OP1dB_{G-48}$	VVA 22dB attenuation DSA 26dB attenuation T_{EP} = -20°C		-18.7		
Output P1dB f_{LO} = 500MHz f_{RF} = 450MHz	$OP1dB_{450}$			13.8		dBm

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

Table 16. Electrical Characteristics – Signal Path Cascaded General Performance

See the F159V Typical Application Circuit. Operated as a dual-path transmitter, V_{DD} = +3.3V, Internal f_{LO} = 2050MHz to generate f_{RF} = 2000MHz, LO_SW_OUT= +4dBm setting, T_{EP} = +25°C, maximum gain setting, all Enable pins = GND, BB_IQ frequency = 49MHz or 50MHz, I leads Q by 90 degrees, BB_I&Q levels = 100mVp-p each tone differential, I and Q = 0.325V common-mode bias, Z_{BB_DIFF} = 110Ω, Z_{RFO} = 50Ω, parameters measured at RF output, Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Channel Isolation	ISO_{IQBB}	From CH0_IBB/QBB to CH1_IBB_QBB and vice versa		89		dB
	ISO_{VGA}	See note [b]	45 [a]	47		
LO (Carrier) Suppression	LO_{supp}	Native, uncorrected		-25	*-18*	dBm
Sideband (Image) Suppression	SS	Native, uncorrected		-40	*-23*	dBc
Output IP2 at 850MHz	$OIP2_1$	f_{LO} = 900MHz, measured at $f_{LO} + (f_{BB1} \pm f_{BB2})$		78		dBm
Output IP2 at 2.00GHz	$OIP2_2$	f_{LO} = 2050MHz, measured at $f_{LO} + (f_{BB1} \pm f_{BB2})$	59	62		dBm
Output IP2 at 2.85GHz	$OIP2_3$	f_{LO} = 2900MHz, measured at $f_{LO} + (f_{BB1} \pm f_{BB2})$		61		dBm
$f_{LO} \pm 2 * f_{BB}$ Rejection	$2BB_{REJ}$	$f_{BB} \leq$ 100MHz		-72	-67	dBc
$f_{LO} \pm 3 * f_{BB}$ Rejection	$3BB_{REJ}$	$f_{BB} \leq$ 100MHz		-95	-75	dBc
$f_{LO} \pm 5 * f_{BB}$ Rejection	$5BB_{REJ}$	$f_{BB} \leq$ 100MHz		-87	-78	dBc
2nd Harmonic of the LO	HD2	$f_{BB} \leq$ 100MHz		-42		dBc
3rd Harmonic of the LO	HD3	$f_{BB} \leq$ 100MHz		-67		dBc
RF Output Return Loss	RL_{RFO}	Within DPD bandwidth VVA = 14dB DSA = 1dB	10	12		dB
Group Delay Error	GD	Between 2 channels with any attenuator setting		±3		ns

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

[b] Baseband signals applied to CH0 baseband inputs (CH1 baseband inputs) with CH1 baseband inputs (CH0 baseband inputs) turned off. Measure the difference in the RF power between CH0_RFOUT (CH1_RFOUT) and CH1_RFOUT (CH0_RFOUT). This difference is the channel isolation.

6. Thermal Characteristics

Table 17. Package Thermal Characteristics

Parameter	Symbol	Value	Units
Junction to Ambient Thermal Resistance	θ_{JA}	32	°C/W
Junction to Case Thermal Resistance. (Case is defined as the exposed paddle)	$\theta_{JC\text{-}BOT}$	3	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL 3	

7. Typical Operating Conditions (TOC)

Unless otherwise noted, for the TOC graphs on the following pages, the following conditions apply:

- Baseband I and Q levels = -20dBm each tone (~ 100mVp-p differential/channel/tone across 110Ω)
- Baseband I and Q tones = 49MHz, 50MHz
- Maximum Gain Setting
- Use internal LO with LO_SW_OUT for +4dBm setting
- T_{EP} = +25°C
- V_{DD} = +3.3V
- V_{CM} = +0.325V
- Internal f_{LO} = 2050MHz
- OIP2 Measured at $f_{LO} + (f_{BB1} \pm f_{BB2})$
- Enable pins = GND
- EVKit RF output trace and connector losses de-embedded

8. Typical Performance Characteristics

Figure 3. Baseband Differential Input Return Loss

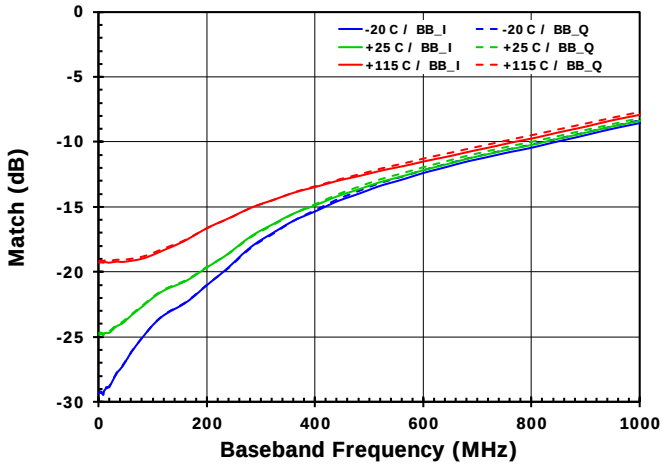


Figure 4. LO Differential Input Return Loss

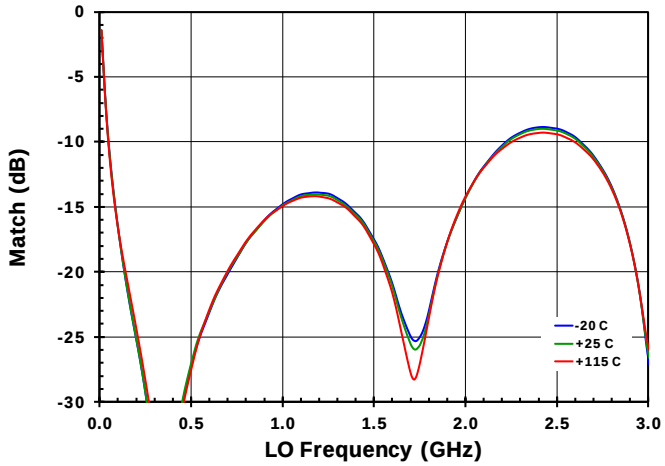


Figure 5. Modulator Coupled Output Return Loss

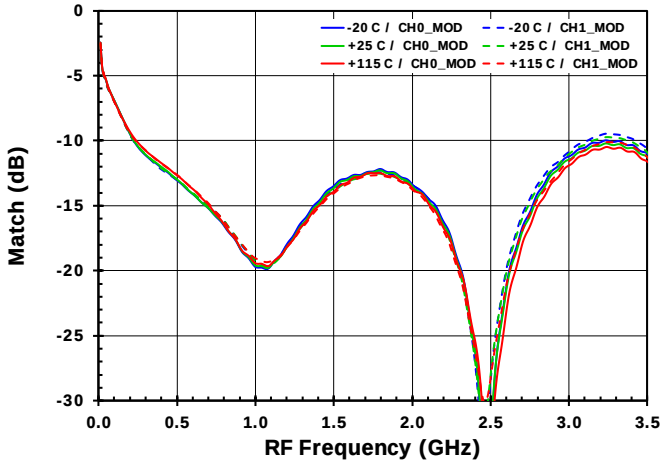


Figure 6. LO Differential Output Return Loss

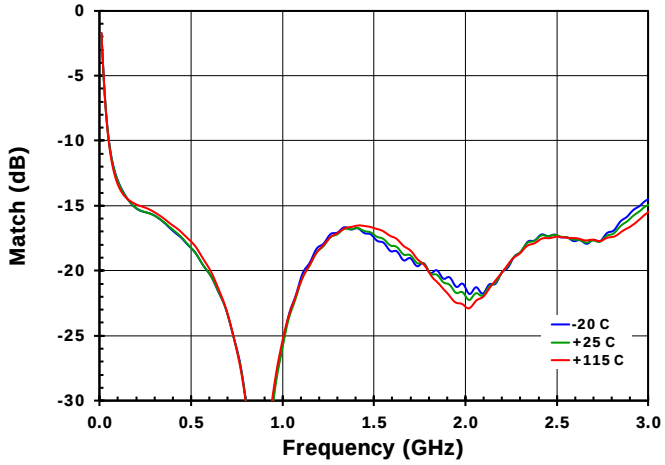


Figure 7. RF Output Return Loss (Maximum Gain)

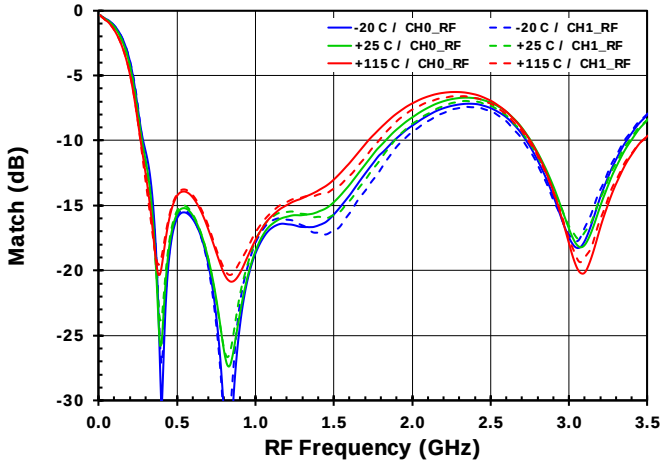
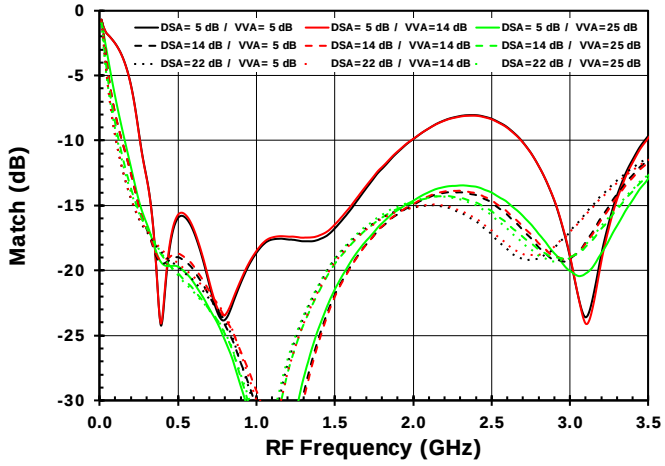


Figure 8. RF Output Return Loss (+25 °C)



9. Typical Performance Characteristics - VVA

Figure 9. Gain versus VVA DAC Setting (+3.3V, 2GHz)

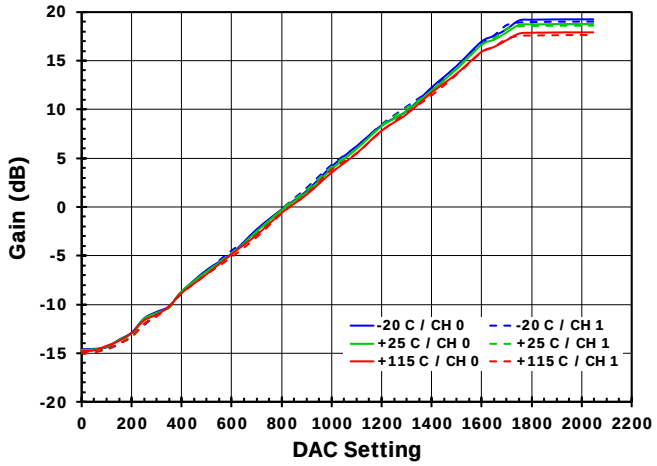


Figure 10. Relative Phase versus VVA DAC Setting (+3.3V, +25°C)

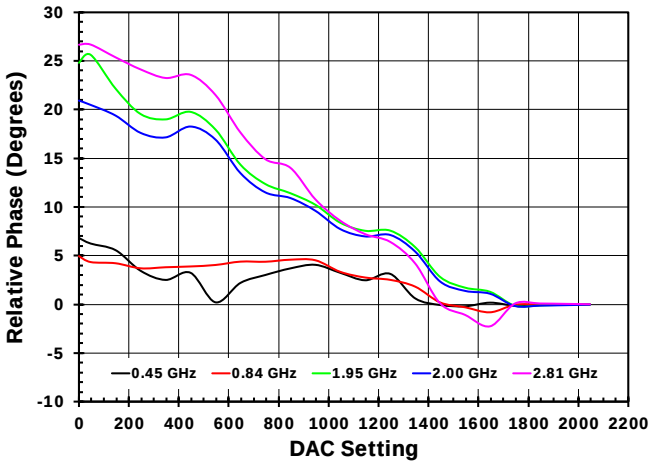


Figure 11. OIP3 versus VVA DAC Setting (+3.3V, 2GHz)

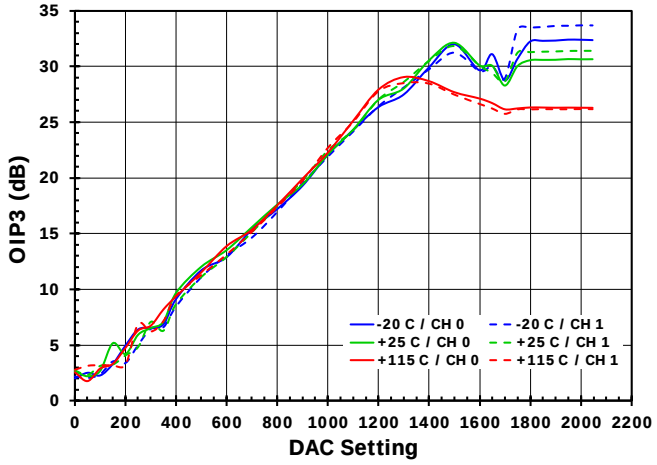


Figure 12. VVA Maximum to Minimum Switching (+3.3V, +25°C, 2GHz)

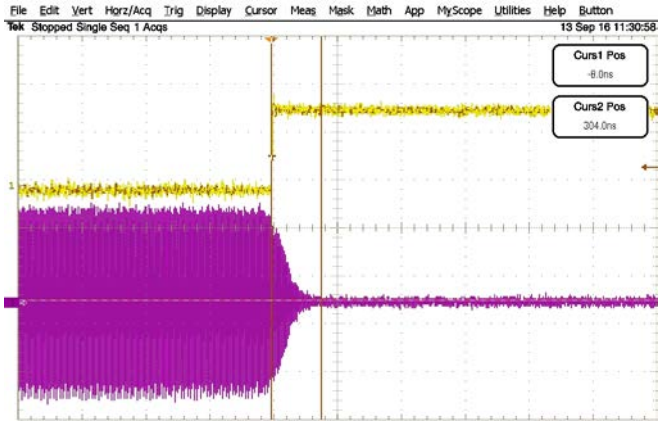
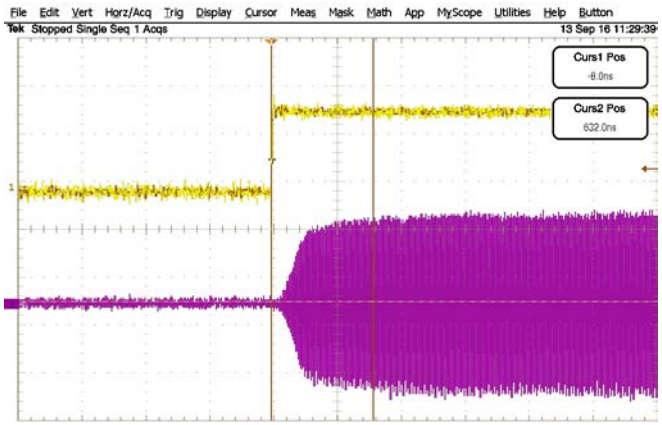


Figure 13. VVA Minimum to Maximum Switching (+3.3V, +25°C, 2GHz)



10. Typical Performance Characteristics - DSA

Figure 14. Gain versus DSA (+3.3V)

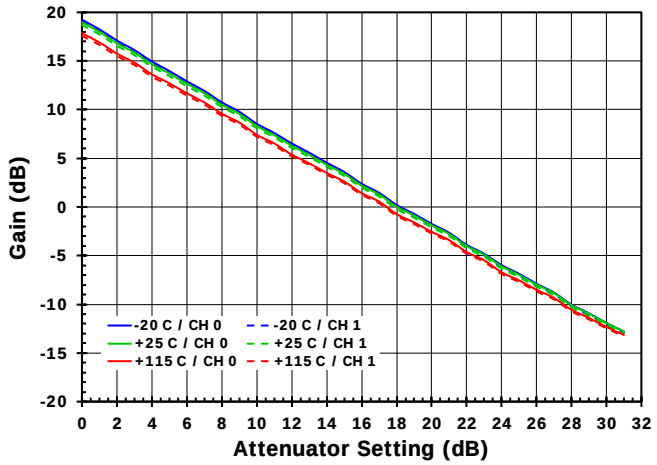


Figure 15. Relative Phase versus DSA (+3.3V, +25°C)

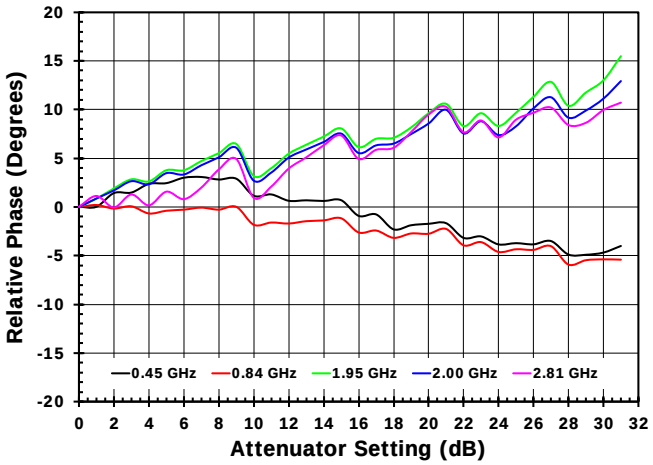


Figure 16. Gain Accuracy versus DSA (+3.3V)

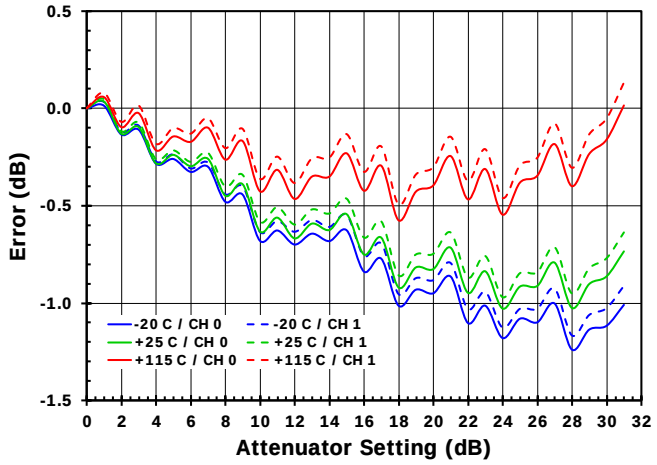


Figure 17. DSA Maximum to Minimum Switching (+3.3V, +25°C)

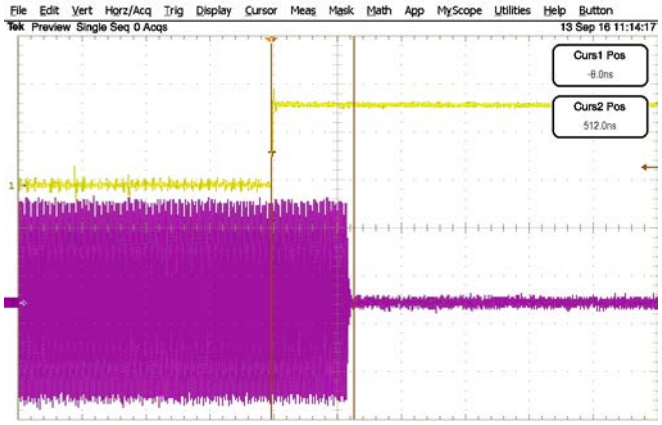


Figure 18. Step Error versus DSA (+3.3V)

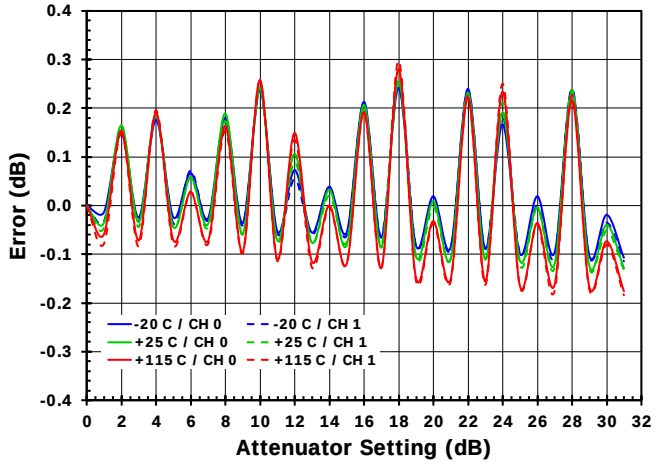
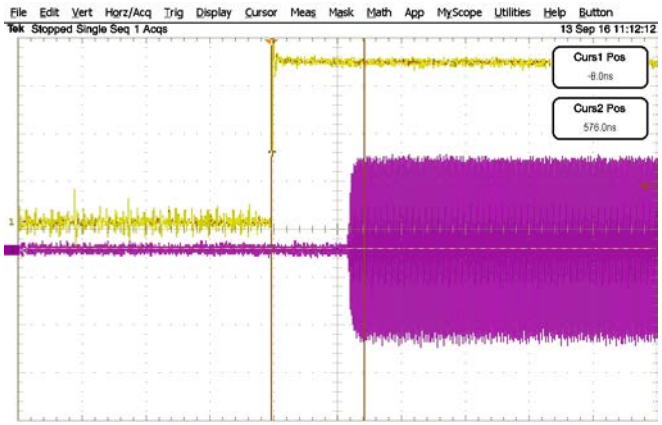


Figure 19. DSA Minimum to Maximum Switching (+3.3V, +25°C)



11. Typical Performance Characteristics - Cascaded Gain

Figure 20. Gain versus Frequency (+25°C)

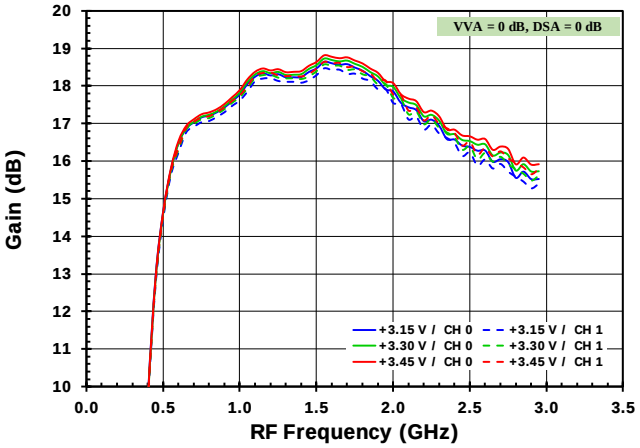


Figure 21. Gain versus Frequency (+3.3V)

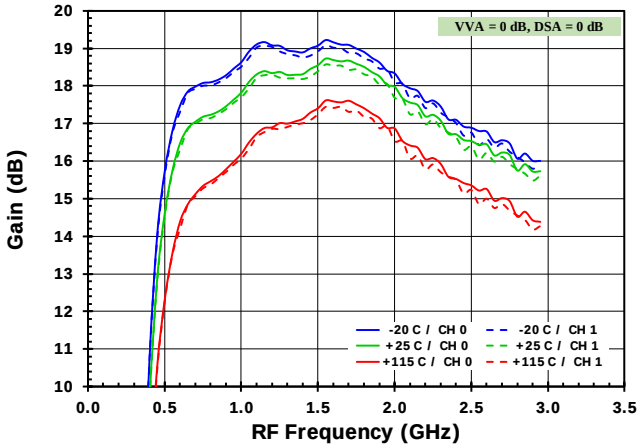


Figure 22. Gain versus Frequency (+3.3V)

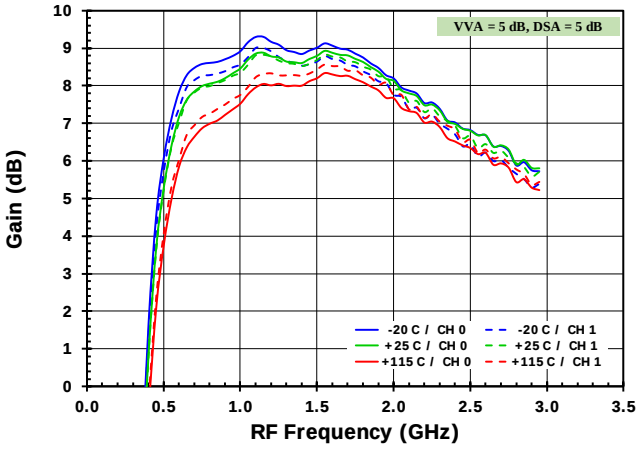


Figure 23. Gain versus Frequency (+3.3V)

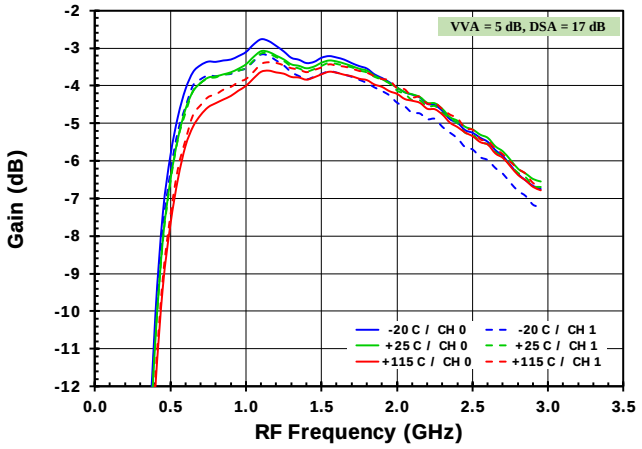


Figure 24. Gain versus Frequency (+3.3V)

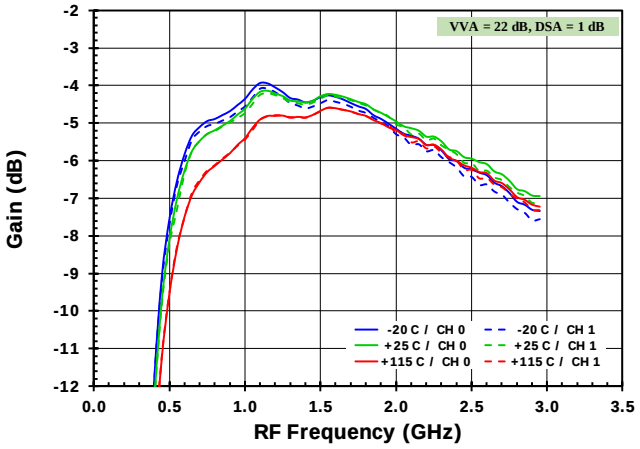
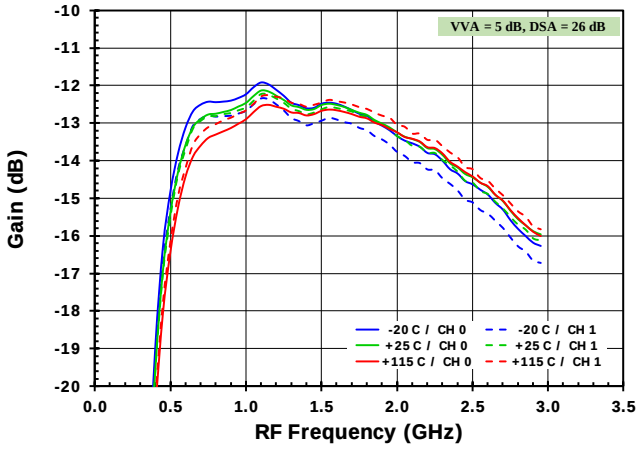


Figure 25. Gain versus Frequency (+3.3V)



12. Typical Performance Characteristics - Cascaded Gain (Cont.)

Figure 26. Gain versus Frequency (+3.3V)

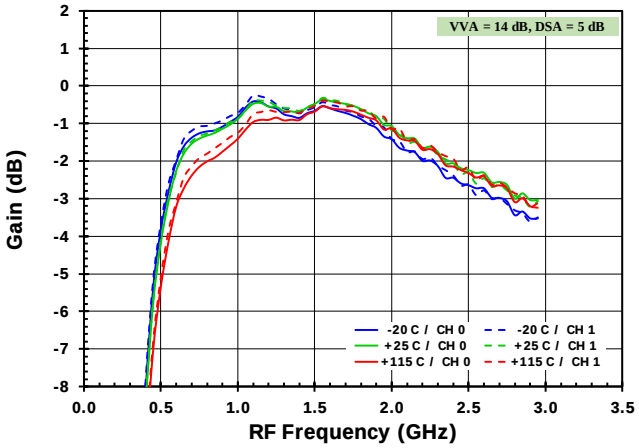


Figure 27. Gain versus Frequency (+3.3V)

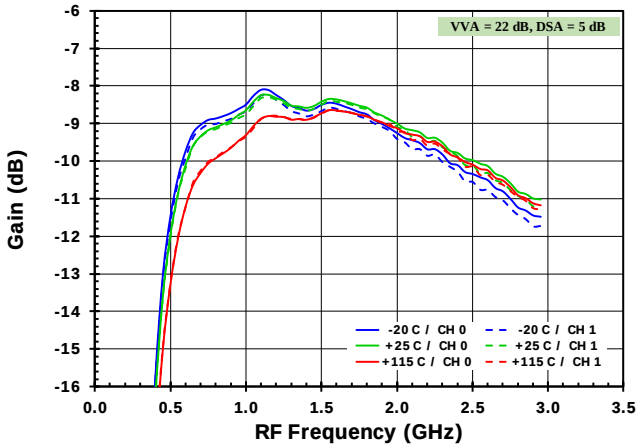


Figure 28. Gain versus Frequency (+3.3V)

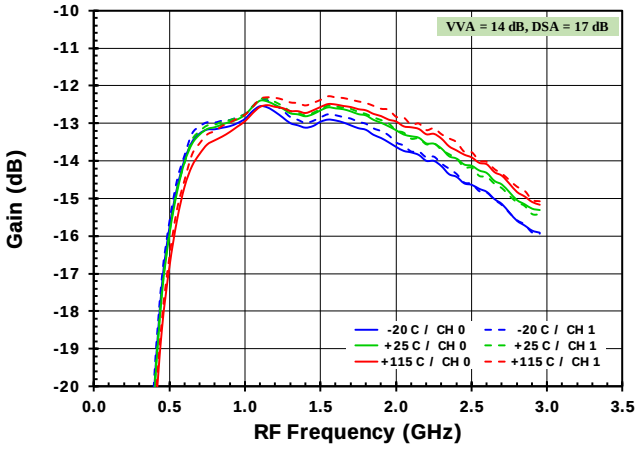


Figure 29. Gain versus Frequency (+3.3V)

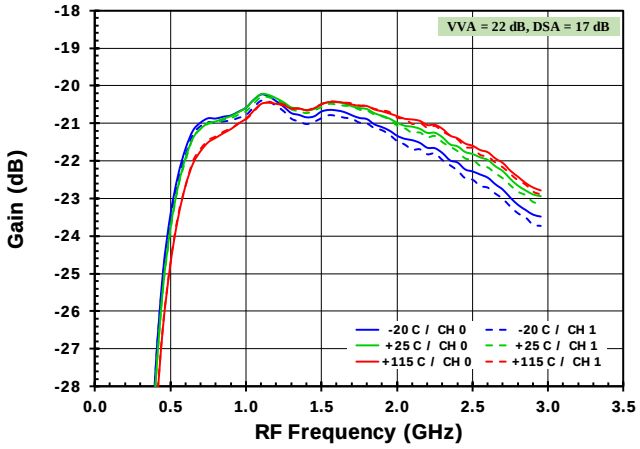


Figure 30. Gain versus Frequency (+3.3V)

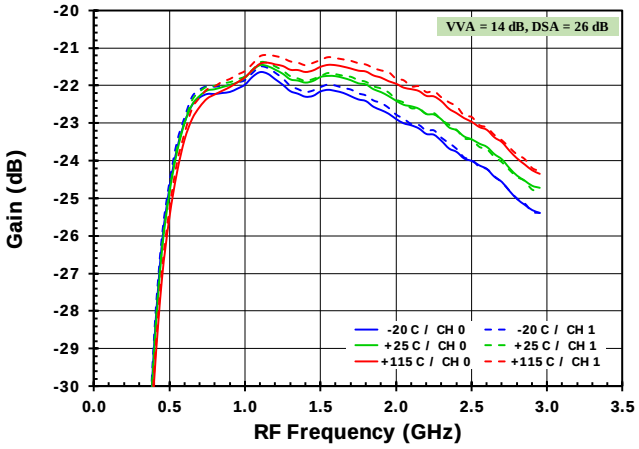
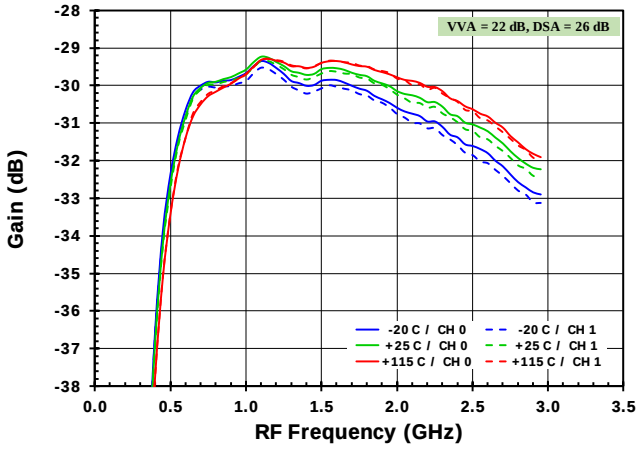


Figure 31. Gain versus Frequency (+3.3V)



13. Typical Performance Characteristics - Cascaded OIP3

Figure 32. OIP3 versus Frequency (+25°C)

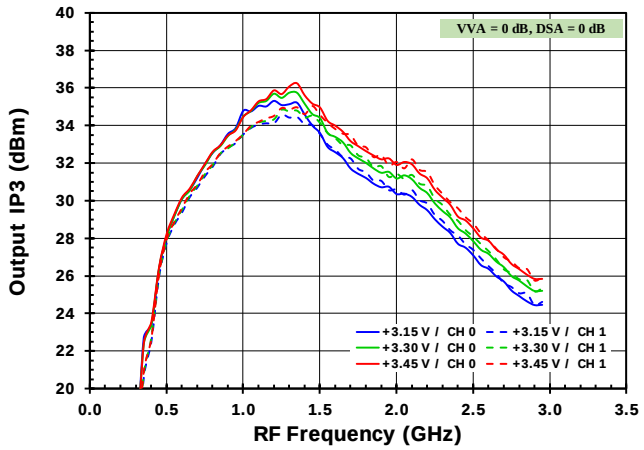


Figure 33. OIP3 versus Frequency (+3.3V)

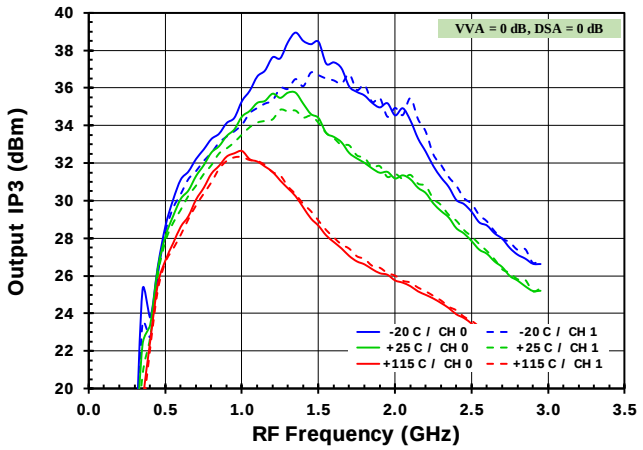


Figure 34. OIP3 versus Frequency (+3.3V)

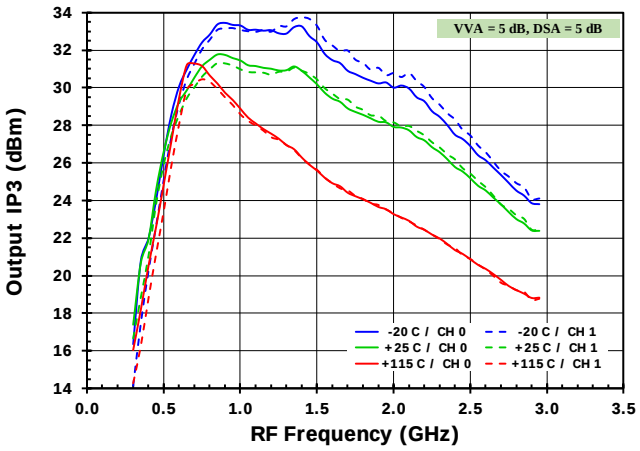


Figure 35. OIP3 versus Frequency (+3.3V)

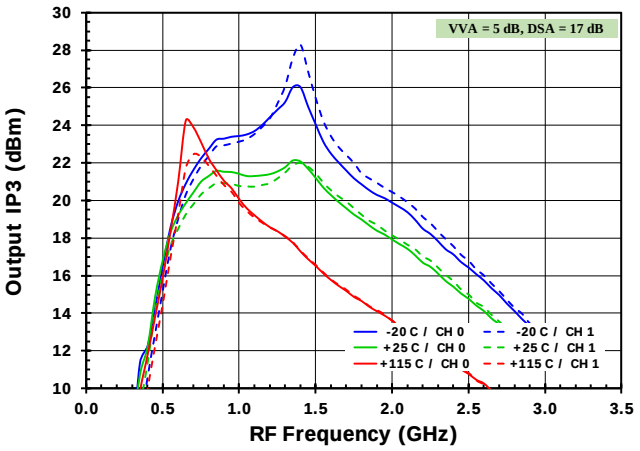


Figure 36. OIP3 versus Frequency (+3.3V)

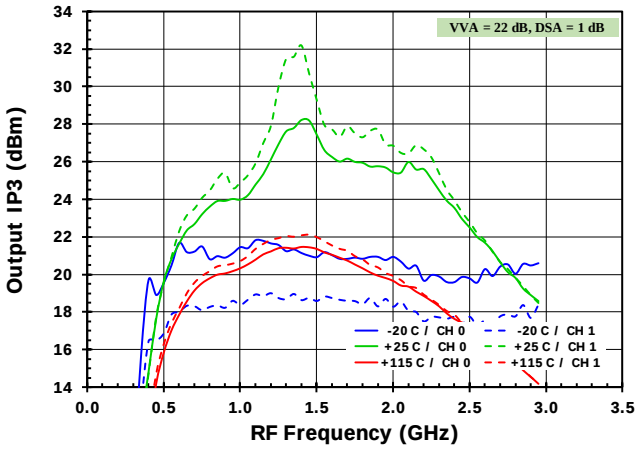
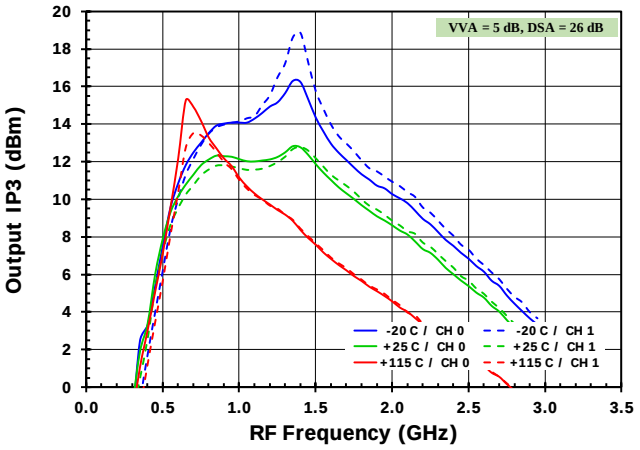


Figure 37. OIP3 versus Frequency (+3.3V)



14. Typical Performance Characteristics - Cascaded OIP3 (Cont.)

Figure 38. OIP3 versus Frequency (+3.3V)

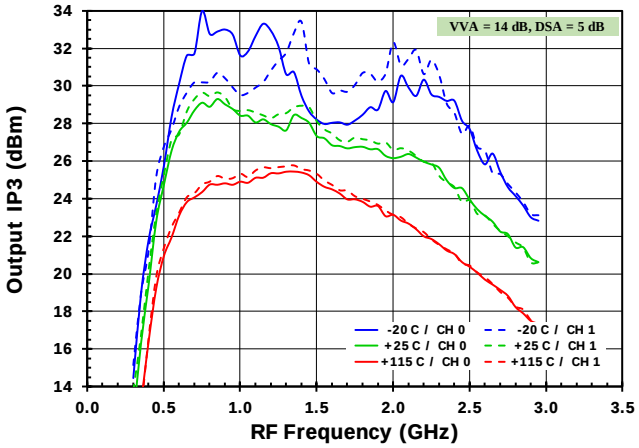


Figure 39. OIP3 versus Frequency (+3.3V)

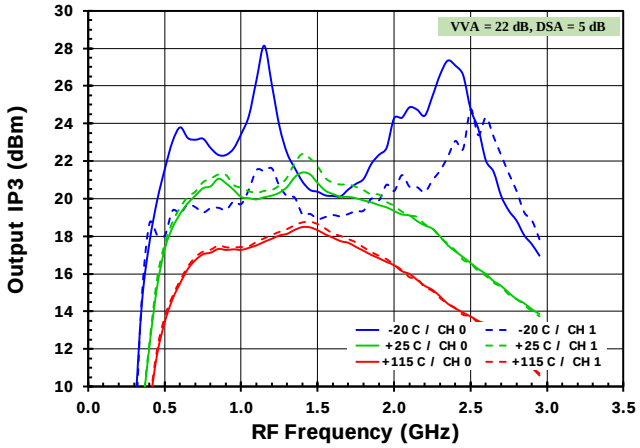


Figure 40. OIP3 versus Frequency (+3.3V)

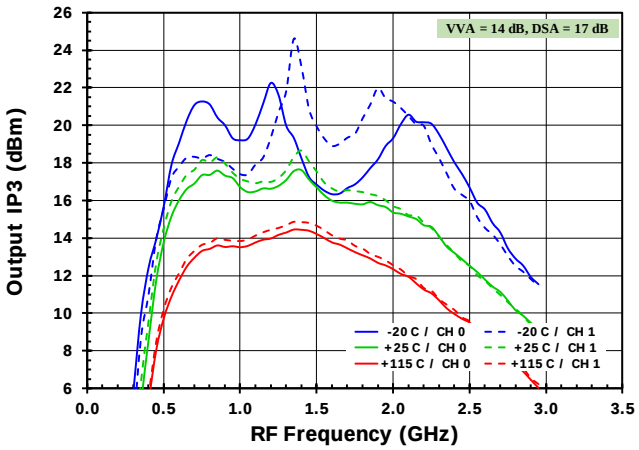


Figure 41. OIP3 versus Frequency (+3.3V)

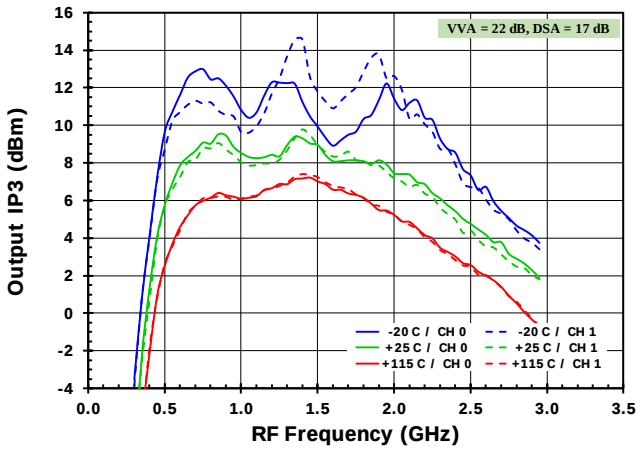


Figure 42. OIP3 versus Frequency (+3.3V)

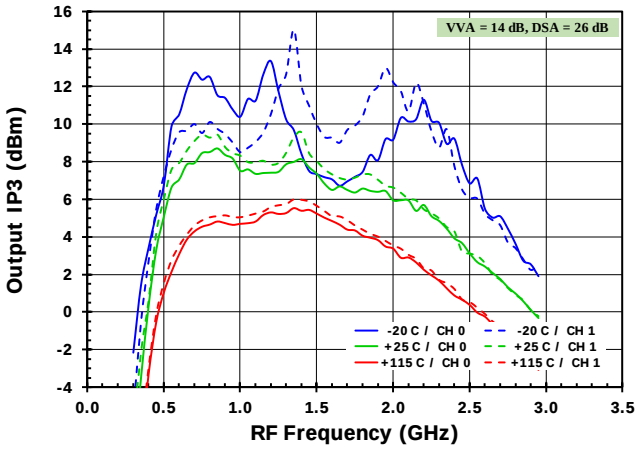
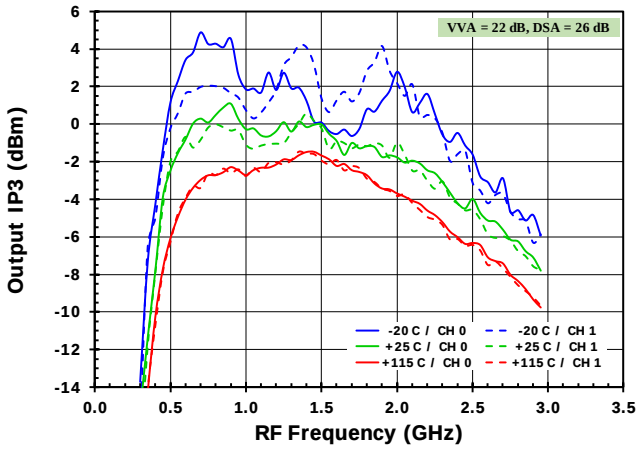


Figure 43. OIP3 versus Frequency (+3.3V)



15. Typical Performance Characteristics - Cascaded OIP2

Figure 44. OIP2 versus Frequency (+25°C)

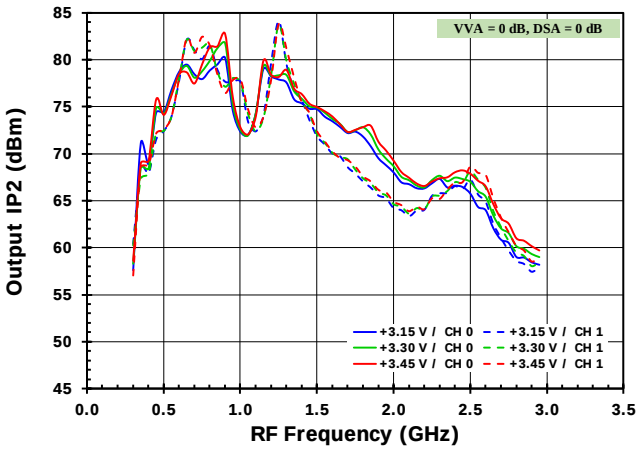


Figure 45. OIP2 versus Frequency (+3.3V)

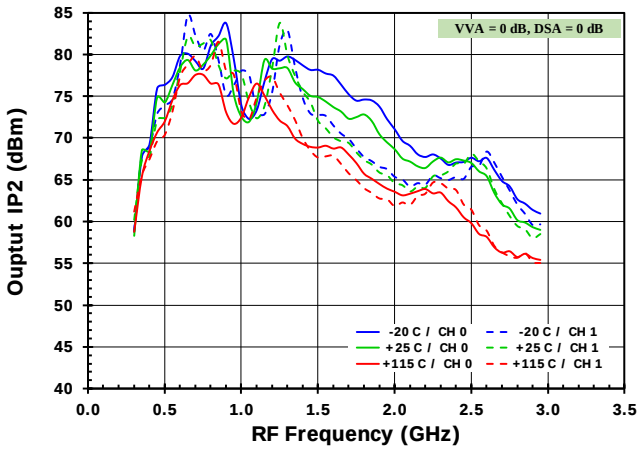


Figure 46. OIP2 versus Frequency (+3.3V)

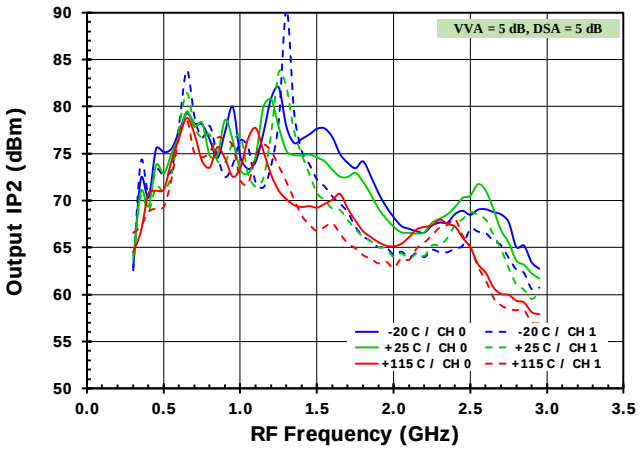


Figure 47. OIP2 versus Frequency (+3.3V)

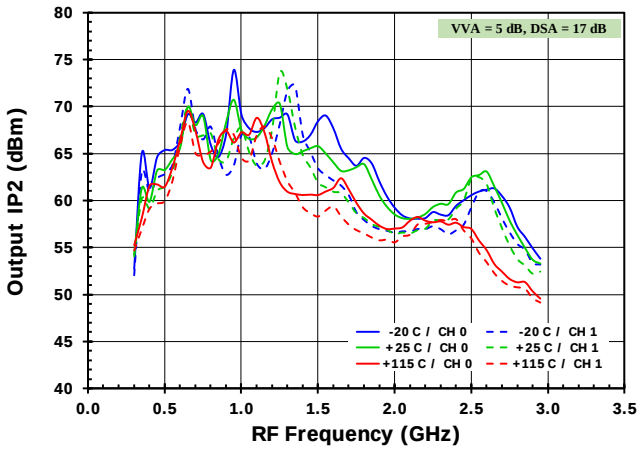


Figure 48. OIP2 versus Frequency (+3.3V)

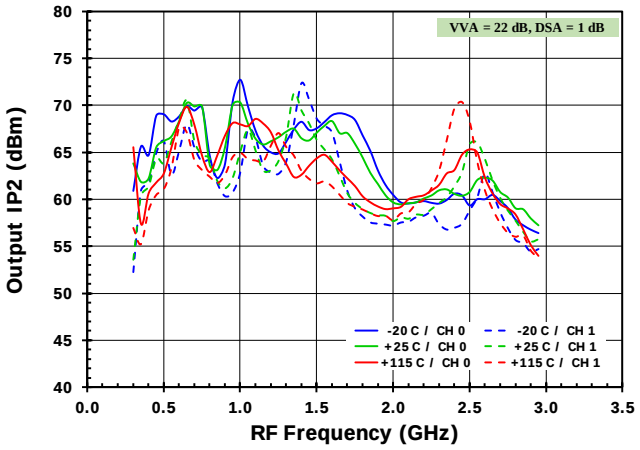
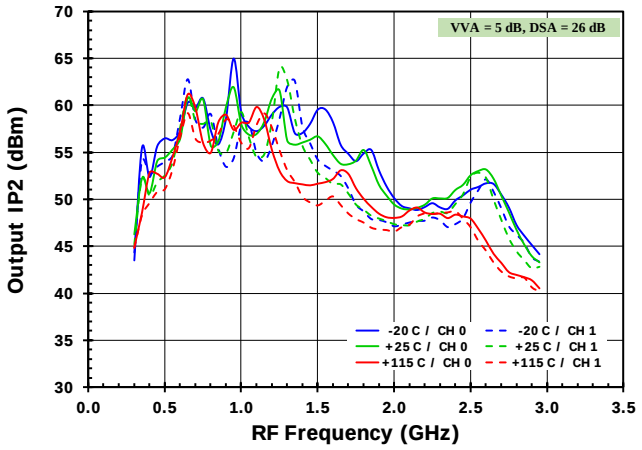


Figure 49. OIP2 versus Frequency (+3.3V)



16. Typical Performance Characteristics - Cascaded OIP2 (Cont.)

Figure 50. OIP2 versus Frequency (+3.3V)

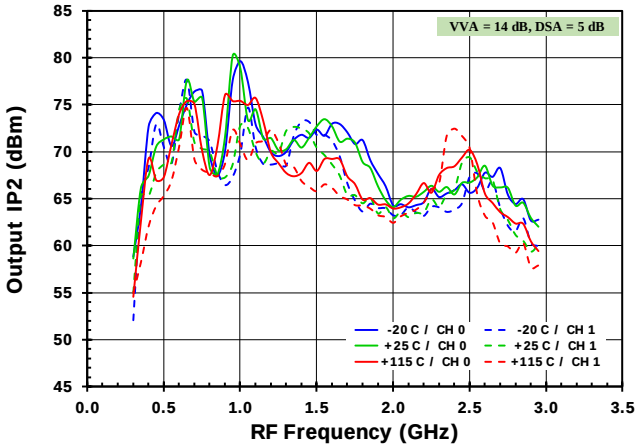


Figure 51. OIP2 versus Frequency (+3.3V)

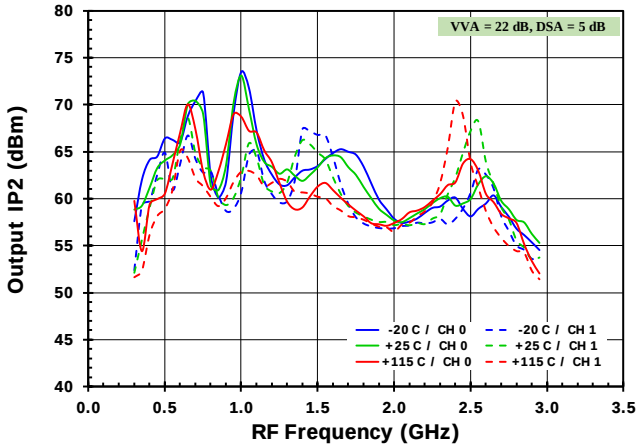


Figure 52. OIP2 versus Frequency (+3.3V)

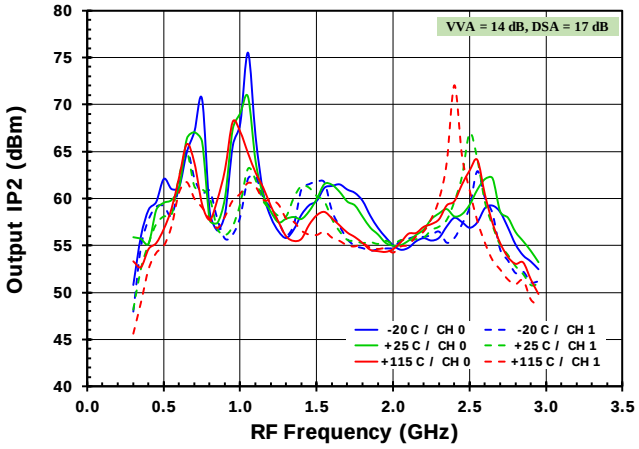


Figure 53. OIP2 versus Frequency (+3.3V)

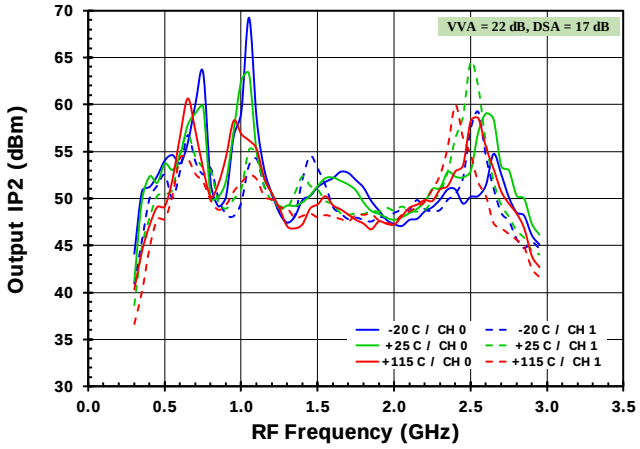


Figure 54. OIP2 versus Frequency (+3.3V)

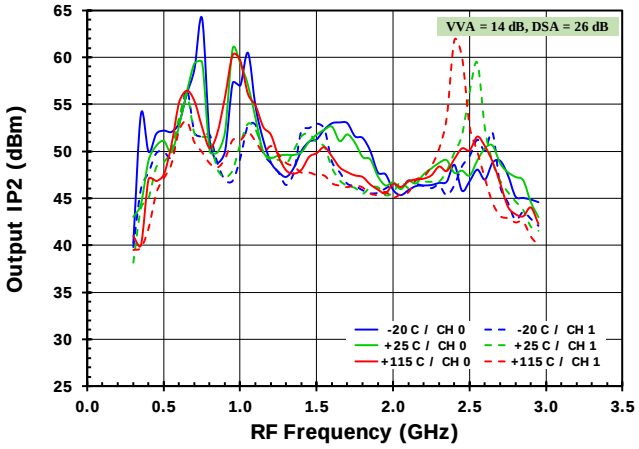
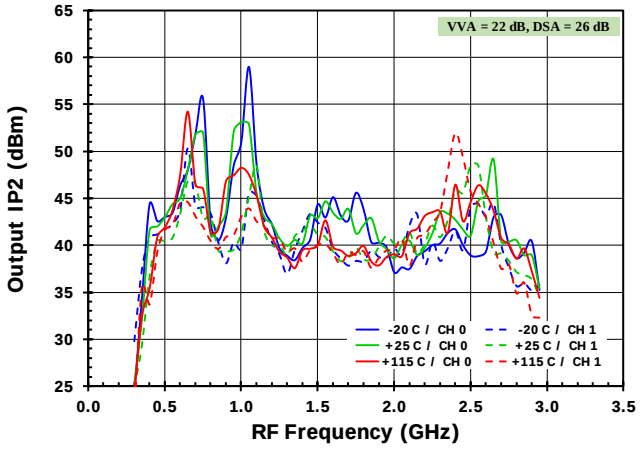


Figure 55. OIP2 versus Frequency (+3.3V)



17. Typical Performance Characteristics - Cascaded OP1dB

Figure 56. Output P1dB vs Frequency (+25°C)

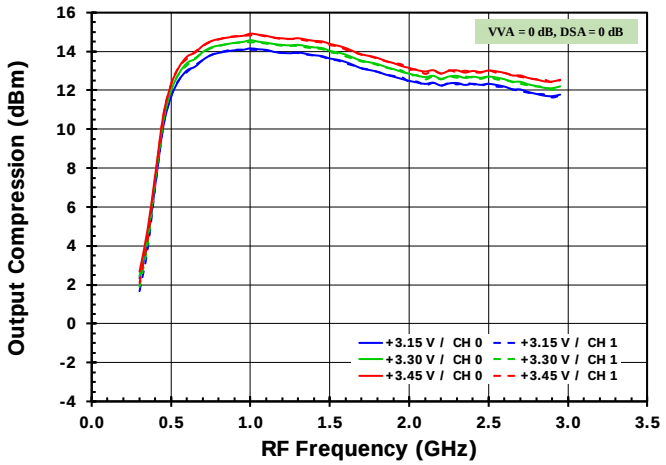


Figure 57. Output P1dB vs Frequency (+3.3V)

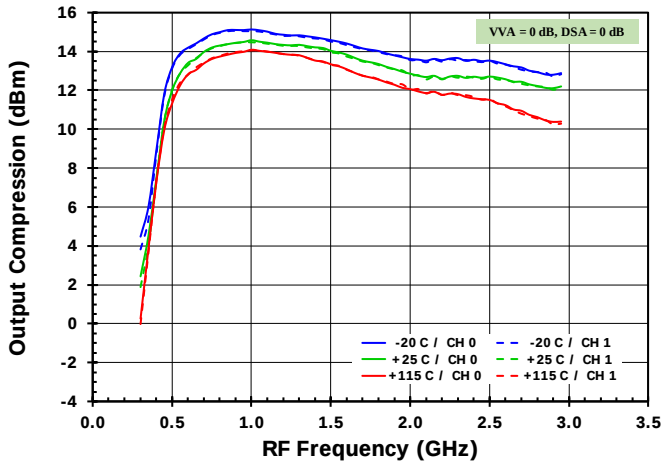


Figure 58. Output P1dB vs Frequency (+3.3V)

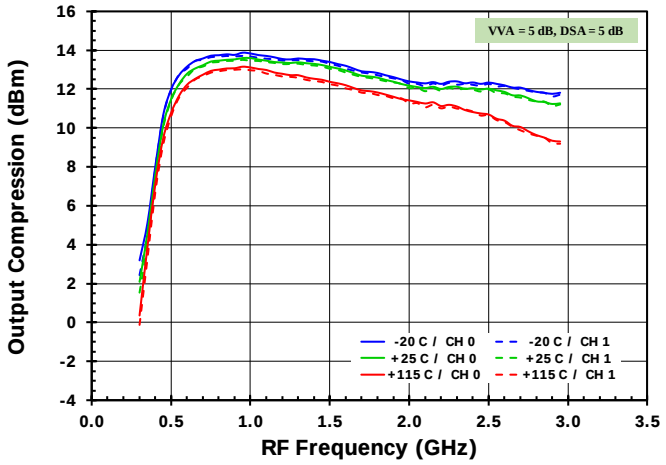


Figure 59. Output P1dB vs Frequency (+3.3V)

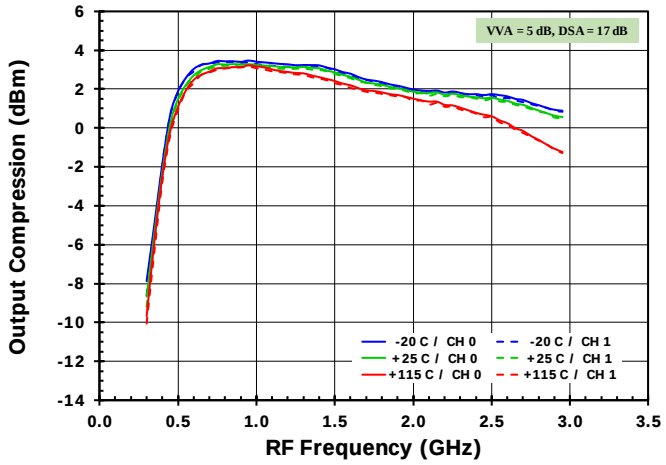


Figure 60. Output P1dB vs Frequency (+3.3V)

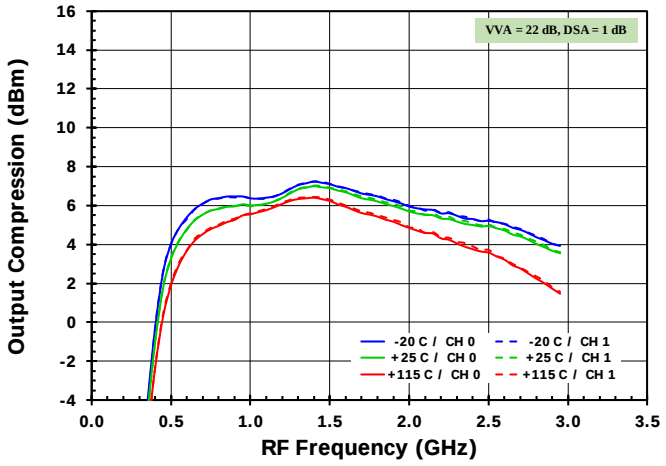
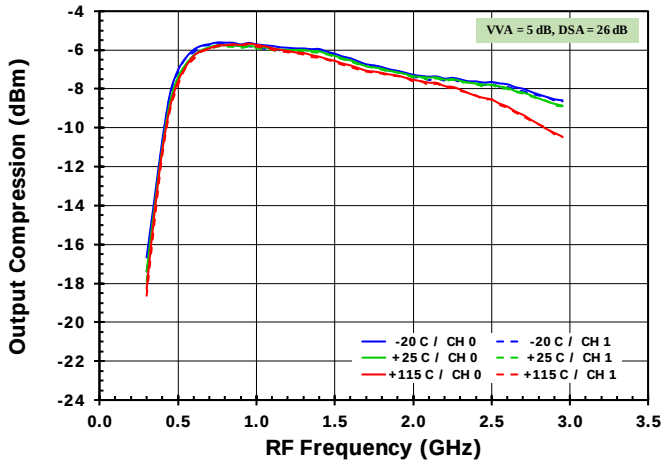


Figure 61. Output P1dB vs Frequency (+3.3V)



18. Typical Performance Characteristics - Cascaded OP1dB (Cont.)

Figure 62. Output P1dB vs Frequency (+3.3V)

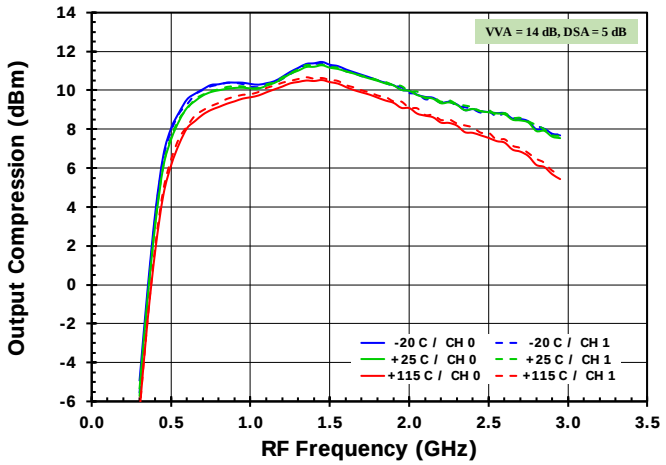


Figure 63. Output P1dB vs Frequency (+3.3V)

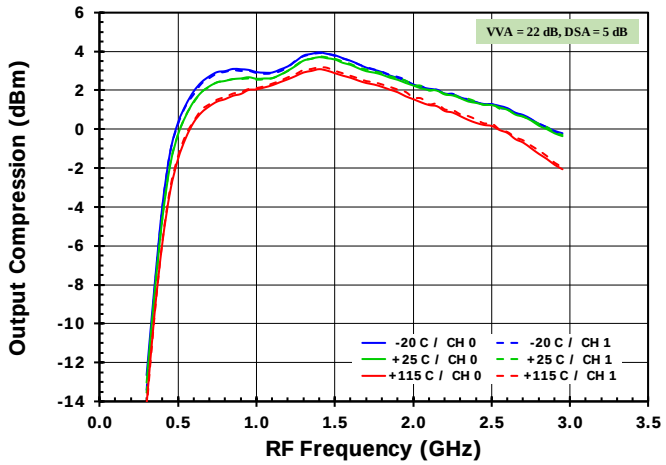


Figure 64. Output P1dB vs Frequency (+3.3V)

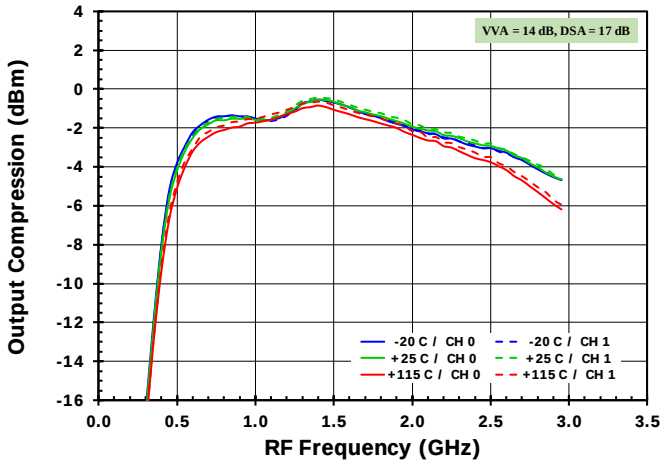


Figure 65. Output P1dB vs Frequency (+3.3V)

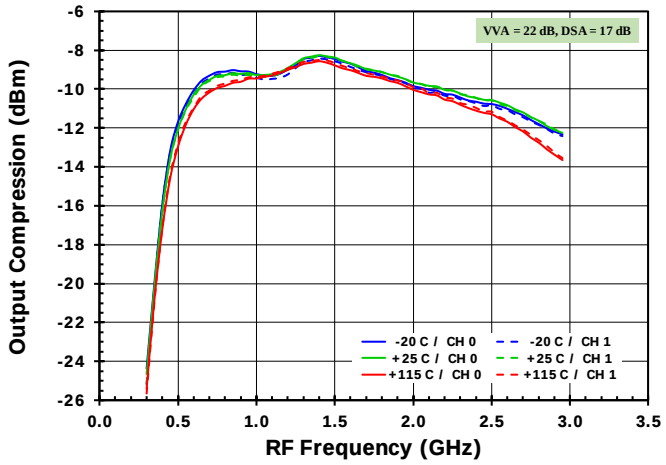


Figure 66. Output P1dB vs Frequency (+3.3V)

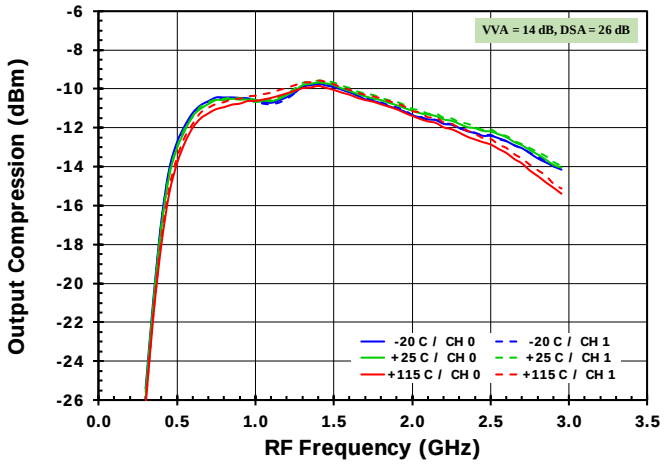
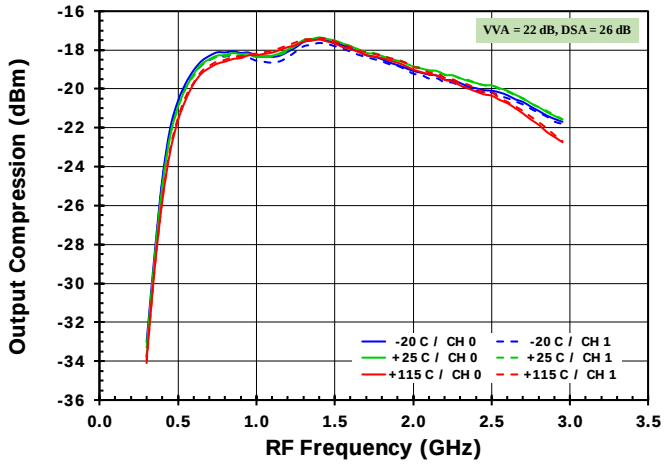


Figure 67. Output P1dB vs Frequency (+3.3V)



19. Typical Performance Characteristics - Harmonics, Current, Switching

Figure 68. Second Harmonic vs Frequency (+3.3V)

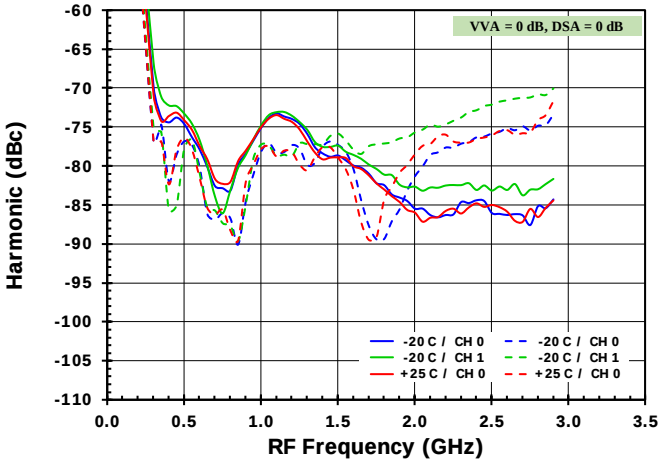


Figure 69. Current vs Frequency (+3.3V)

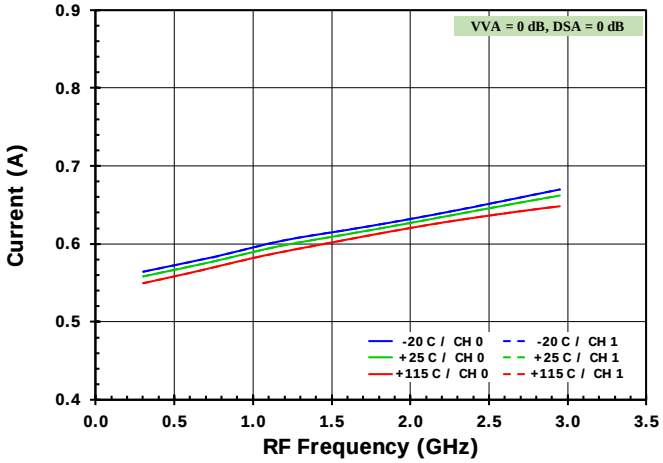


Figure 70. Third Harmonic vs Frequency (+3.3V)

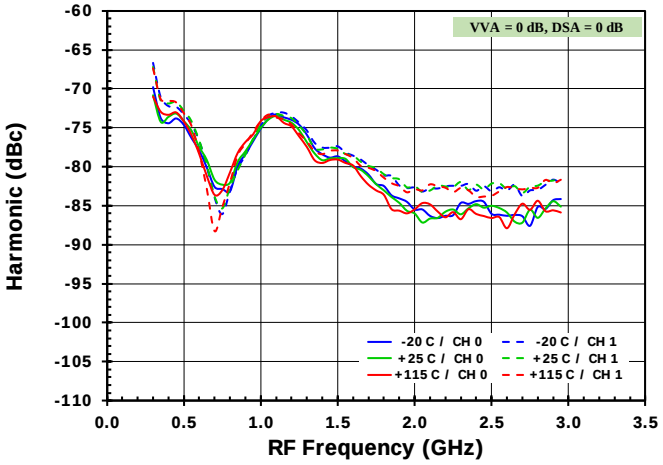


Figure 71. Amplifier Enable Pin Switched from LOW to HIGH

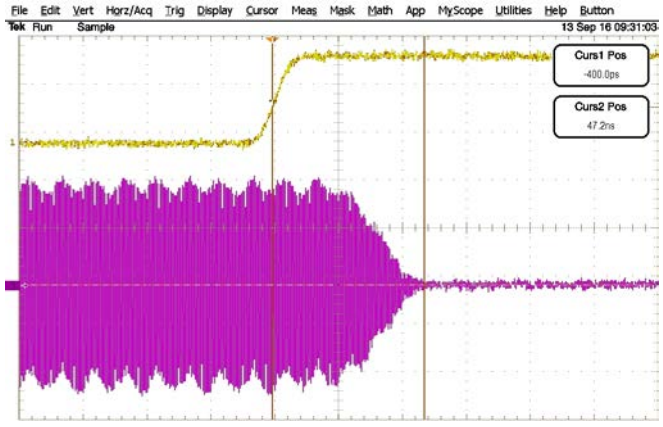


Figure 72. Fifth Harmonic vs Frequency (+3.3V)

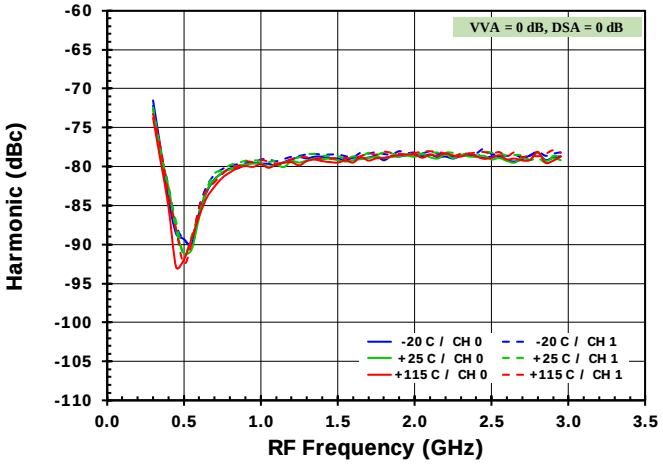
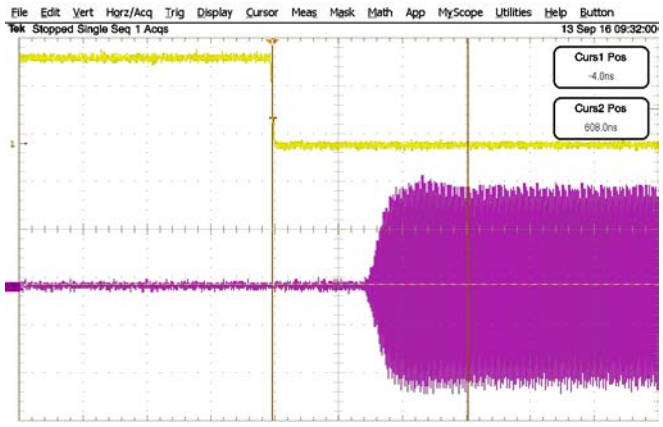


Figure 73. Amplifier Enable Pin Switched from HIGH to LOW



20. Typical Performance Characteristics - Modulator Coupled Output

Figure 74. Gain versus Frequency (+3.3V)

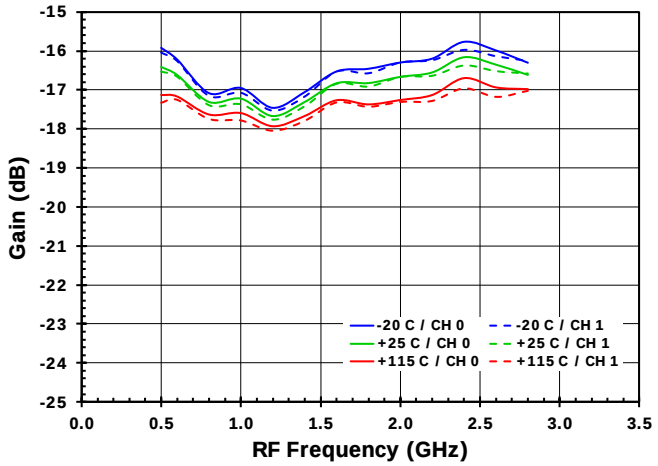


Figure 75. Output Power versus Frequency (+3.3V)

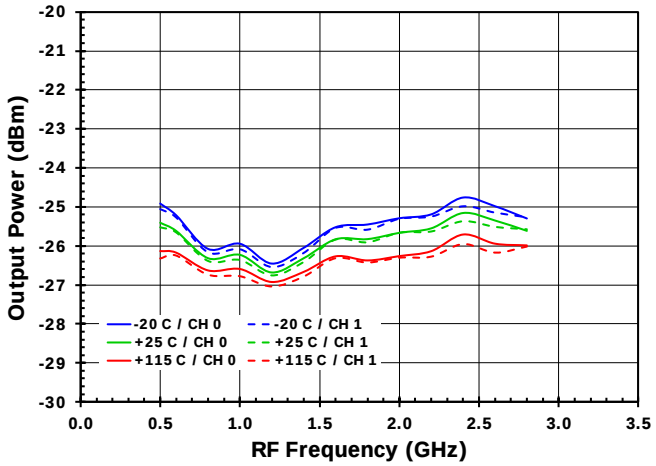


Figure 76. OIP3 versus Frequency (+3.3V)

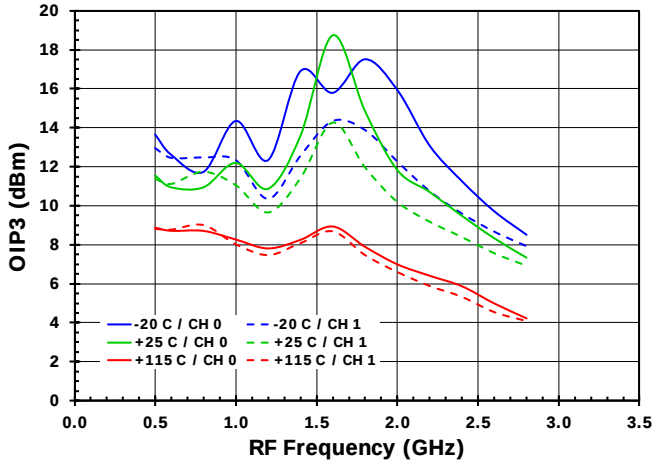


Figure 77. OIP2H versus Frequency (+3.3V)

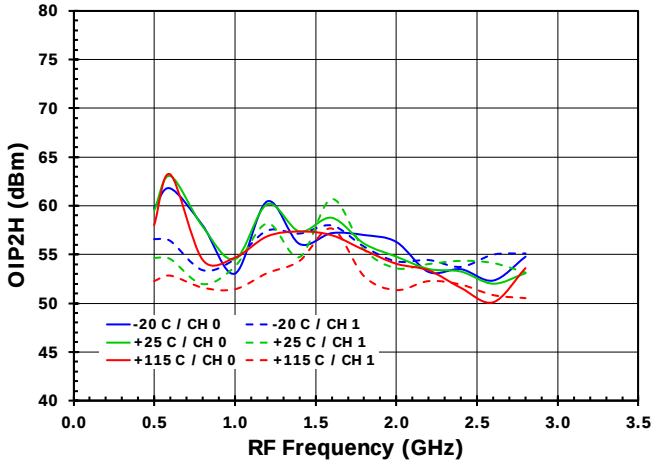
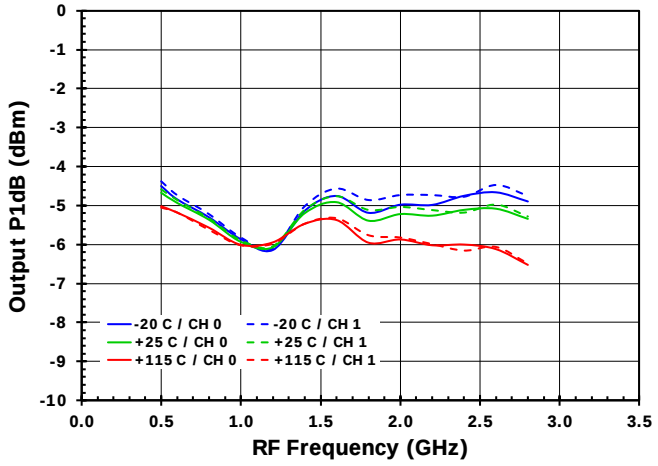


Figure 78. OP1dB versus Frequency (+3.3V)



21. Typical Performance Characteristics - Modulator Coupled Output

Figure 79. 2nd Baseband Harmonic versus Frequency (+3.3V, f_{LO} +/- $2f_{IF}$)

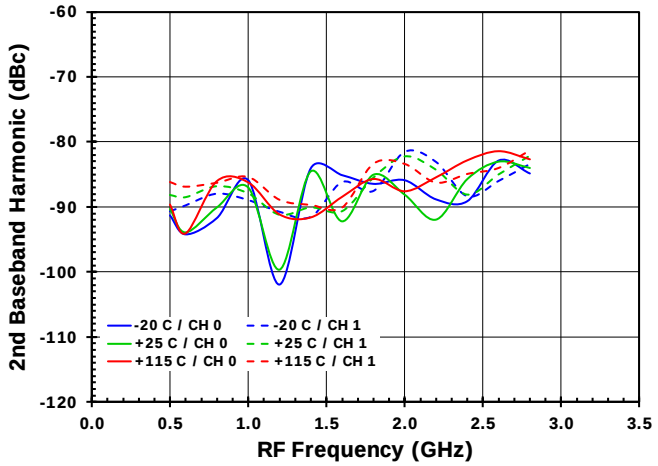


Figure 80. LO Leakage

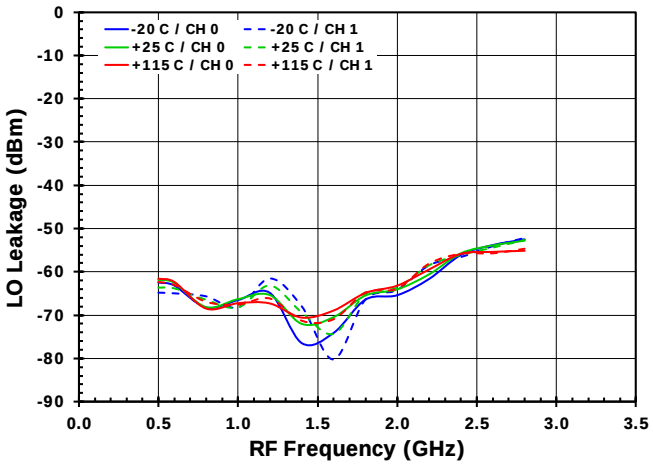


Figure 81. 3rd Baseband Harmonic versus Frequency (+3.3V, f_{LO} +/- $3f_{IF}$)

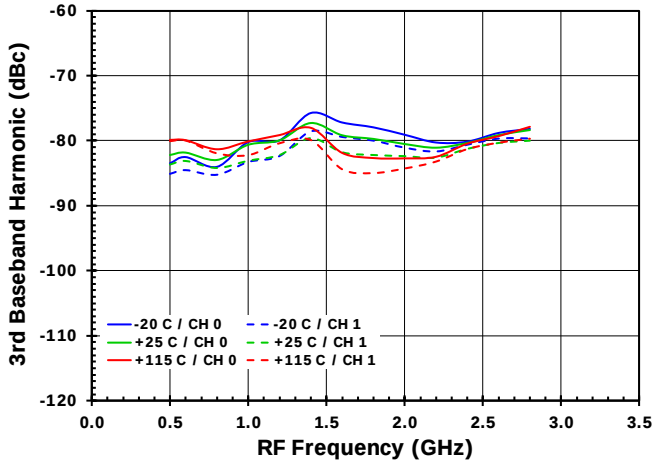


Figure 82. Switching Time ON to OFF

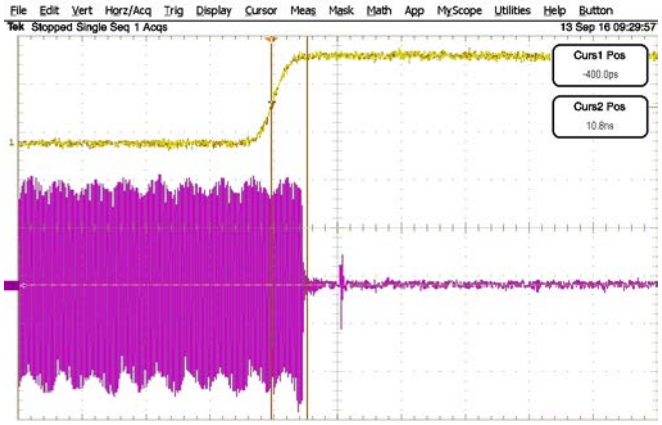


Figure 83. 5th Baseband Harmonic versus Frequency (+3.3V, f_{LO} +/- $5f_{IF}$)

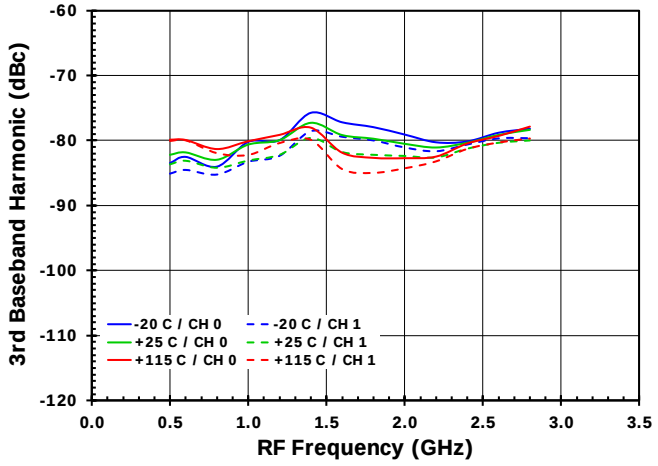
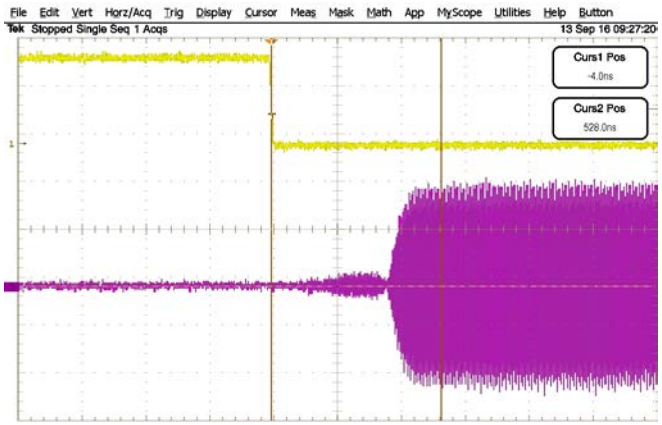


Figure 84. Switching Time OFF to ON



22. Typical Performance Characteristics - LO

Figure 85. LO Output Power versus Frequency (+3.3V)

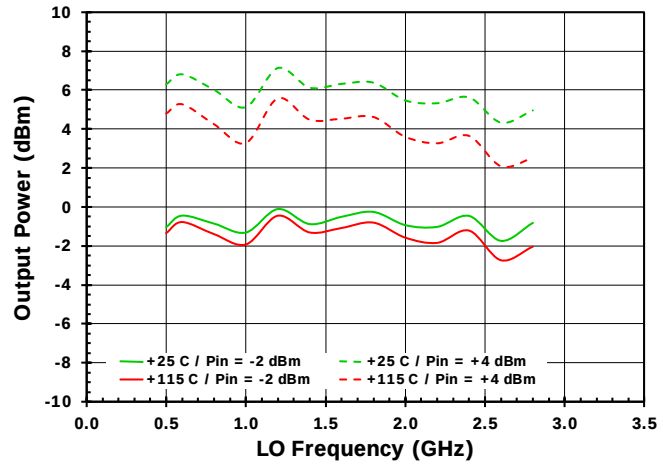


Figure 86. Lock Detect (f_{LO} = 1.8745GHz)

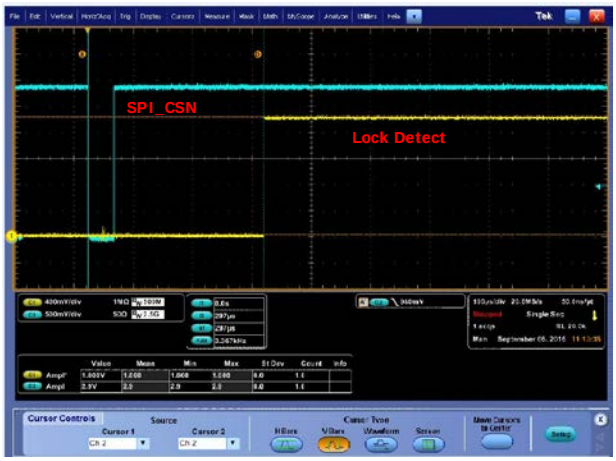


Figure 87. LO Output Phase Noise (0.9425GHz)

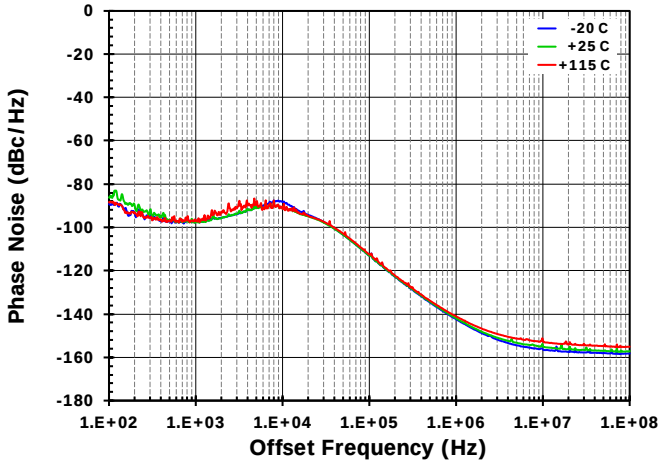


Figure 88. LO Output Phase Noise (1.8475GHz)

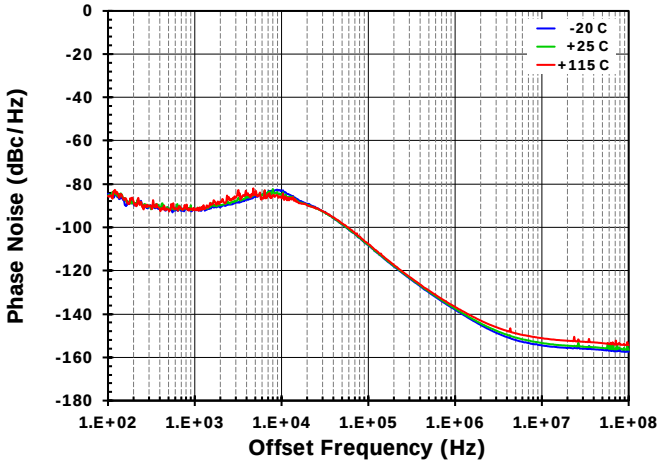


Figure 89. LO Output Phase Noise (2.1550GHz)

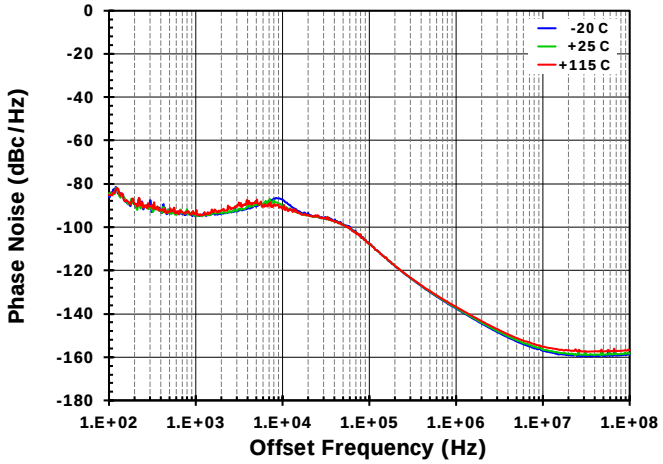
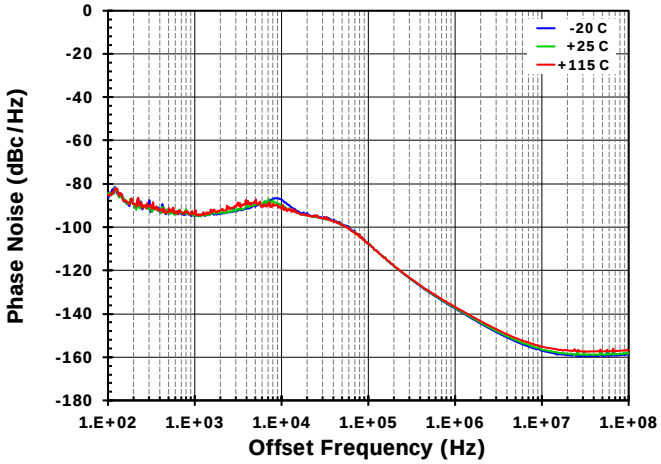


Figure 90. LO Output Phase Noise (2.6550GHz)



23. Theory of Operation

The F159V transmit chip can be defined as three separate functions:

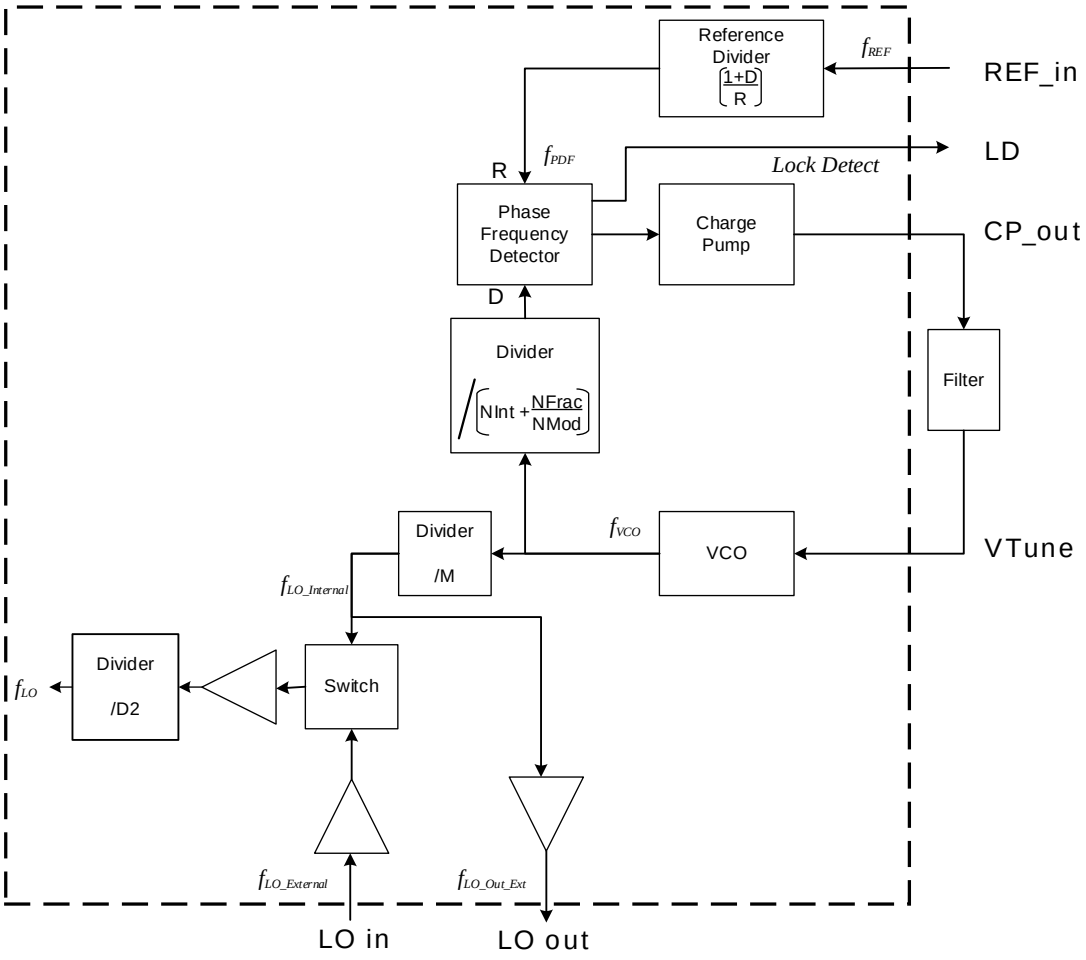
- Frequency Generator – The F159V uses either an internal voltage controlled oscillator (VCO) that is locked using a fractional-N phase lock loop (PLL) or an external frequency source. The internal VCO has a frequency range of 2GHz–4GHz. If an external frequency is used this must be supplied using a 100Ω differential signal. There is only one frequency generator per device but this signal is split into two different paths.
- Modulator – The baseband signals, which are 100Ω differential I/Q signals, are up-converted with the signal generated from the frequency generator. There are two modulators per device.
- Variable Gain Amplifier – After a signal is modulated for each of the paths, the signal is amplified and can be attenuated with both a digital step attenuator (DSA) and voltage variable attenuator (VVA). There are two variable gain amplifiers (VGA) per device.

Controlling the F159V is done using fifty 8-bit registers.

23.1. Frequency Generator

The signal used as the carrier for the modulator can be supplied via an external source or internally generated via a fractional-N phase lock loop (PLL). The block diagram is shown in Figure 91. Controlling the various switches, dividers, and PLL is done by serially programming registers to generate the required frequency. The registers are described in the following section.

Figure 91. Phase Lock Loop (PLL) Schematic



23.1.1. Internal (VCO) Frequency

The fractional-N architecture is implemented via a cascaded programmable dual modulus prescaler. The N divider offers a division ratio in the feedback path of the PLL, and is given by programming the values of NInt, NFrac, and NMod. The VCO frequency is determined by the following equation:

$$f_{VCO} = f_{PFD}\left[NInt + \frac{NFrac}{NMod}\right] \; or \; f_{PFD} = \frac{f_{VCO}}{\left[NInt + \frac{NFrac}{NMod}\right]}$$

Each of the values is a 16-bit word that requires the programming of two registers.

Table 18. Feedback Divider Values

Name	Register	Description	Register Name	Function
NInt	17 18	Feedback Divider Integer Value	NInt_0 NInt_1	This sets the integer value for feedback divider which is a 16-bit word. The value is limited between 7 and 65,535. NInt_0 is the lower 8 bits. NInt_1 is the upper 8 bits. The default value is 63 = 0000_0000_0011_1111b.
NFrac	19 20	Feedback Divider Fractional Value	NFrac_0 NFrac_1	This sets the fractional value for feedback divider which is a 16-bit word. There is no limit to the value and can be between 0 and 65,535. NFrac_0 is the lower 8 bits. NFrac_1 is the upper 8 bits. The default value is 31232 = 0111_1010_0000_0000b.
NMod	21 22	Feedback Divider Modulus Value	NMod_0 NMod_1	This sets the modulus value for feedback divider which is a 16-bit word. The value must be between 2 and 65,535. NMod_0 is the lower 8 bits. NMod_1 is the upper 8 bits. The default value is 65535 = 1111_1111_1111_1111b.

The Fractional-N PLL can be put into an integer N mode. This is accomplished by setting the fractional value, NFrac, to 0.

23.1.2. Reference Frequency

The Phase Frequency Detector also requires a reference frequency for proper operation. The externally applied reference signal can be either a sine or square wave. This signal can be translated for various performance enhancements.

$$f_{PFD} = f_{REF}\left[\frac{1 + \mathrm{D}}{R}\right]$$

When setting the frequency for the phase frequency detector, f_{PFD}, it is possible to double (D=1) the reference frequency before dividing the frequency (R). The phase frequency detector has an upper frequency limit of 250MHz in the Integer-N mode. When used in the Fractional-N mode, the upper frequency is limited to 105MHz.

Table 19. Reference Frequency Divider Values

Name	Register	Description	Register Name	Function
D	16	Reference Frequency Doubler	Ref_Doubler	This is a 1-bit control word that will double the externally applied reference frequency. This is the fifth bit on the word of the 8-bit word. The default value is 1 (doubler is on).
R	16	Reference Frequency Divider	Ref_Doubler	This is a 4-bit control word that sets the divider for the externally applied reference frequency. The value is between 1 and 15. If the value is 0 then the divider is set for 1. This is the first four bits of the word. The default value is 1 = 0000b.

23.1.3. Charge Pump

The charge pump current is programmable via the ICP register for maximum flexibility for PLL Bandwidth and performance. We recommend that default value be used.

Table 20. Charge Pump

Name	Register	Description	Register Name	Function
ICP	24	Charge Pump Current	ChrgPmp	This is a 4-bit control word that sets the output current of the charge pump. This is the first four bits of the word. The default value is 0.94mA = 0010b.

23.1.4. External Loop Filter

An external loop filter is required which is connected between CP_OUT and VTUNE. The design is application specific. See Application Note 849 for a general description for a loop filter design.

23.1.5. LO Frequency

The frequency that is used for the modulator is obtained from one of two paths. The first is from the internal VCO and PLL circuit. The output frequency of the VCO can be divided by up to a factor of 8 using a 3-bit control word.

$$f_{LO\_Internal} = \frac{f_{VCO}}{M}$$

There is a switch that allows this internal signal or an external signal to be used. There is another divider that can be used to further reduce the frequency by a factor of 2. This divider can be used on either the internal signal or the external frequency supplied.

$$f_{LO} = \frac{f_{LO\_Internal}}{D2} \; or \; \frac{f_{LO\_External}}{D2}$$

It is important to note that for the lower frequency LO signals (f_{LO}) lower than 1.15GHz, the quadrature divider must be enabled to generate the quadrature LO signal. At higher frequencies, an optimized filter is provided that properly splits the signal for the two paths, therefore the quadrature divider must be disabled.

Table 21. LO Frequency Divider Values

Name	Register	Description	Register Name	Function
MDiv	23	Output Divide Ratio	MDiv	This is a 3-bit control word that divides the VCO signal. This is first three bits of the word. The default value is 1 = 001b (divide by 2).
D2	23	Quadrature Divider	MDiv	This is a 1-bit control word that sets the divide by 2 option for signal used in the modulator. This can be applied to either the internal or external signal. This is the fourth bit of the word. The default value is to divide by 1.

23.1.6. Voltage Control Oscillator (VCO)

The VCO should be set for automatic calibration. If needed, the user can manually change the frequency. There are also different ways to set how the VCO is locked.

Table 22. VCO setting

Name	Register	Description	Register Name	Function
Force_Relock	36	VCO Locking	Force_Relock	This is a 1-bit control word that forces the PLL to recalibrate itself. The default value is to not relock (0b). When the value is enabled (1b), the PLL is recalibrated and then the bit is self-clearing (reset to 0b).
Band_Select_Disable	36	Band Selection	Force_Relock	This is a 1-bit control word that deals with the PLL recalibration. If any registers from 16 to 22 are written to, then the PLL is recalibrated with the default value of 0b. When the value is enabled (1b), the PLL is not recalibrated.
Auto_Recal_Enable	36	Recalibration	Force_Relock	This is a 1-bit control word that sets the PLL in the auto-recalibration mode. The default value of 0b will disable the auto recalibration. When the value is enabled (1b), the PLL will allow auto-recalibration mode.
BandSelDiv	38 39	Band Select Divider	BandSelect_0 BandSelect_1	This is a 12-bit word that will manually set the VCO band to be used. BandSelect_0 is the lower 8 bits. BandSelect_1 has the upper 4 bits. The default value is 256 = 0001_0000_0000b.

Table 23. LO Signal Power

Name	Register	Description	Register Name	Function
LO_BAND	33	Sets the LO frequency range	Freq_Band	This 1-bit word sets the operation of the LO frequency range. If set for logic LOW then frequency range is 1.50GHz to 2.00GHz. If set for logic HIGH, the frequency range is either 0.45GHz to 1.50GHz or 2.00GHz to 2.80GHz. The default value is the 1.50GHz to 2.00GHz frequency range = 0b.
RF_BAND	33	Sets the RF frequency range	Freq_Band	This 1-bit word sets the operation of the RF frequency range. If set for logic LOW then frequency range is 0.55GHz to 2.80GHz. If set for logic HIGH, the frequency range is either 0.45GHz to 0.55GHz. The default value is the 1.50GHz to 2.00GHz frequency range = 0b.
Dig_Out_Level	34	Sets the logic voltage	Logic	This 1-bit word sets the logic level for the device operation. If set for logic LOW, then JEDEC 1.8V logic is used. If set for logic HIGH, then JEDEC 3.3V logic is used The default value is JEDEC 1.8V logic = 0b.
LDP	35	Sets the lock time for the frequency	Freq_Lock	This 3-bit word sets the precision setting for the frequency lock detection. The default value is 11.5ns = 000b
LDPinMode	35	Set operation of the LOCK pin	Freq_Lock	This 2-bit word sets how the voltage on the Lock pin is set. The default value is for Normal lock detection = 00b

23.1.7. LO Switch Matrix

Through the LO Switch matrix, the F159V will route an LO signal from the internal PLL or from an external source. The device can also route the internal LO externally for use in other components. The external LO signals are differential signals and the impedance is 100Ω. In addition, the power can be modified to adjust the performance.

Table 24. LO Signal Power

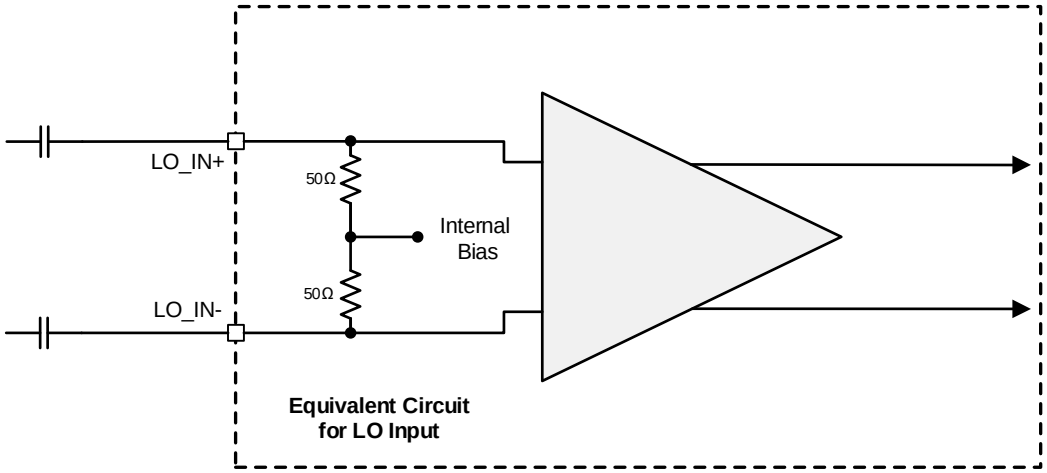
Name	Register	Description	Register Name	Function
LO_Out_Pwr	25	LO Power to Quadrature Divider	LO_Set_1	This is a 2-bit control word that sets the output power to the quadrature divider. The power can be adjusted from -2dBm to +4dBm in 2dB steps. The default value is 0dBm = 01b.
LO_SW_Out_Pwr	25	LO Power to External LO Port	LO_Set_1	This is a 2-bit control word that sets the output power to the external LO port. The power can be adjusted from -2dBm to +4dBm in 2dB steps. The default value is 0dBm = 01b.
LO_Out_Pwr_extra	25	Add extra power	LO_Set_1	This 1-bit word will increase the LO output power by adding 9.6mA of current to the pre-driver. The default value is no extra power= 0b.

Table 25. LO Signal Routing

Name	Register	Description	Register Name	Function
LO_In_Enable	26	LO Input Amplifier	LO_Set_2	This is a 1-bit control word that enables or disables the LO input amplifier. The default has this amplifier disabled (turned off).
LO_Out_Enable	26	LO Output Amplifier	LO_Set_2	This is a 1-bit control word that enables or disables the LO output amplifier. The default has this amplifier disabled (turned off).
LO_SW_Out_Enable	26	LO Output Switch	LO_Set_2	This is a 1-bit control word that enables or disables the switch to route the LO from the PLL to the output LO port. The default has switch enabled (turned on).
DAC_Enable	26	DAC Control	LO_Set_2	This is a 1-bit control word that enables or disables the DAC. The default has this enabled (turned on).
PLL_Enable	26	PLL Control	LO_Set_2	This is a 1-bit control word that enables or disables the PLL. The default has the PLL enabled (turned on or internal LO signal).
LO_SW_Out_Select	26	PLL Control	LO_Set_2	When this bit is set for logic LOW, the switch selects the output of the internal VCO. When this bit is set for logic HIGH, the switch selects the LO_IN (external) input. This is the control for the switch shown in Figure 92.

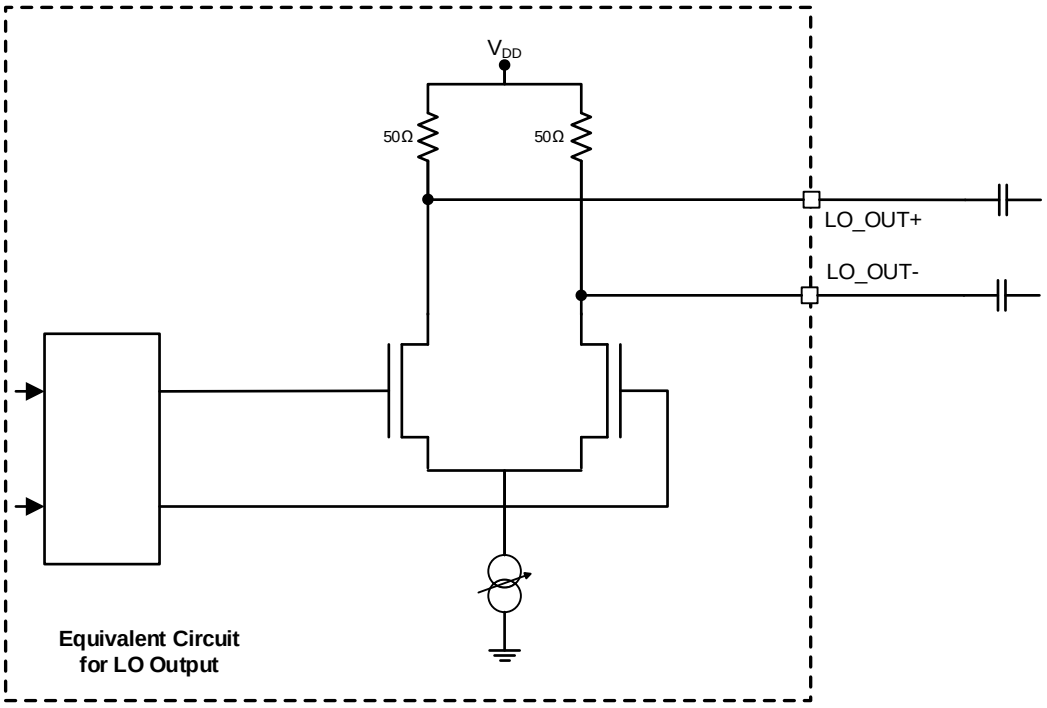
The LO_IN+/LO_IN- inputs are 100Ω differential inputs. The 100Ω termination is provided internal to the synthesizer die (as shown below). In addition, an internal bias ensures the proper DC operating level. For this input configuration, it is preferred that the inputs are AC coupled into LO_IN+/LO_IN-

Figure 92. LO Input Schematic



The LO_OUT+/LO_OUT- output pair is derived from the drain of an NMOS differential pair with on-chip termination resistors to V_{DD} (as shown below).

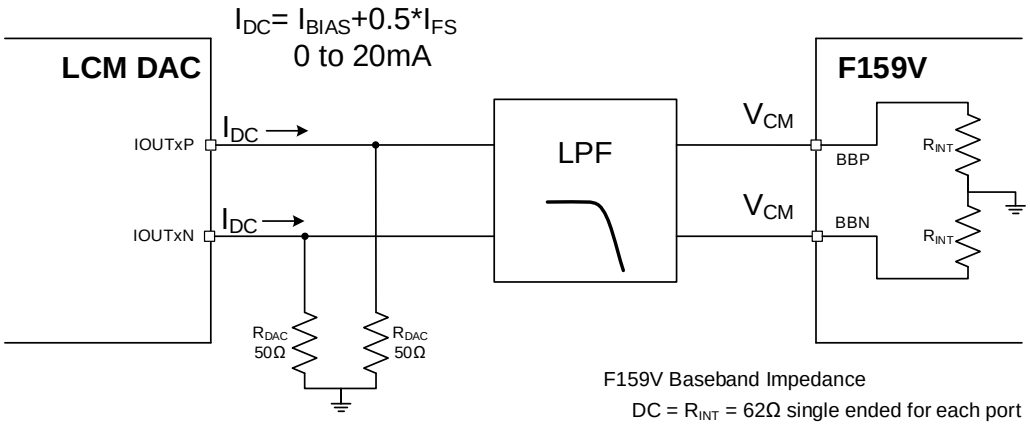
Figure 93. LO Output Schematic



23.2. Modulator

There are two modulators, one for each channel. The LO generated by the frequency generator is shared by both modulators. Each modulator has its own differential IF signal input. Figure 94 shows a general schematic to interface a Digital to Analog Converter (DAC) to the modulator input. There is a coupled output of the RF signal before the variable gain amplifier. There is no control of the modulator.

Figure 94. Generic DAC Interface



F159V Baseband Impedance
DC = R_{INT} = 62Ω single ended for each port
AC ~ 110Ω differential

LCM DAC: Low Current Mode Voltage DAC which usually has a high output impedance and will source an output current.

I_{BIAS}: Internal bias current of the DAC

I_{FS}: Full Scale current of the DAC

LPF: Differential Low Pass Filter for unwanted harmonics.

V_{CM}: Common Mode Voltage is determined by the DAC bias current and DC impedance of the IQ Modulator and DAC. It is given as

$$V_{CM} = I_{DC}\frac{R_{DAC}R_{INT}}{R_{DAC}+R_{INT}}$$

23.3. Variable Gain Amplifier

There are two variable gain amplifiers, one for each channel, which are used to adjust the output signal amplitude. There is both a digital step attenuator (DSA) which has 31dB of attenuation in 1dB steps and a voltage variable attenuator (VVA) that has 33dB of attenuation. The VVA can be set with a 12-bit word. Minimum attenuation is at the maximum digital word of 2047.

Table 26. Digital Step Attenuator Setting

Name	Register	Description	Register Name	Function
DSA0	27	Attenuator setting for DSA in Path 0	DSA0	This is a 5-bit control word that sets the attenuation setting for the DSA Channel 0. This is the first 5 bits of the word. The default value is 0dB = 0 0000b.
DSA1	28	Attenuator setting for DSA in Path 1	DSA1	This is a 5-bit control word that sets the attenuation setting for the DSA Channel 1. This is the first 5 bits of the word. The default value is 0dB = 0 0000b.

Table 27. Digital Step Attenuator Truth Table

DSA[4]	DSA[3]	DSA[2]	DSA[1]	DSA[0]	Attenuator Setting (dB)
LOW	LOW	LOW	LOW	LOW	0
LOW	LOW	LOW	LOW	HIGH	1
LOW	LOW	LOW	HIGH	LOW	2
LOW	LOW	HIGH	LOW	LOW	4
LOW	HIGH	LOW	LOW	LOW	8
HIGH	LOW	LOW	LOW	LOW	16
HIGH	HIGH	HIGH	HIGH	HIGH	31

Table 28. Voltage Variable Attenuator Setting

Name	Register	Description	Register Name	Function
VVA0	29 30	Voltage setting for VVA in Path 0	DAC0_0 DAC0_1	This is a 12-bit control word that sets the attenuation setting for the VVA in Channel 0. DAC0_0 is the lower 8 bits. DAC0_1 is the upper 4 bits. The default value is 2047 = 0111_1111_1111b.
DSA1	31 32	Voltage setting for VVA in Path 1	DAC1_0 DAC1_1	This is a 12-bit control word that sets the attenuation setting for the VVA in Channel 1. DAC1_0 is the lower 8 bits. DAC1_1 has the upper 4 bits. The default value is 2047 = 0111_1111_1111b.

23.4. General Settings

23.4.1. Initial Startup

When the F159V is initially powered up, power is applied to all the V_{DD} pins, or the RESET pin is set to logic LOW, the device is placed in the following state:

- Default logic is 1.8V.
- The reference frequency doubler is enabled.
- The PLL is set for integer mode with a divider of 63.
- The LO signal used for the modulator is set for half the frequency of the PLL frequency and 0dBm.
- The LO is set for the 1.50GHz to 2.00GHz range.
- The internal LO signal is used for the modulator.
- The PLL is enabled.
- Digital step attenuators are set for the minimum attenuation (0dB).
- Voltage variable attenuators are set for the minimum attenuation (state 2047) and the DAC used to control them is turned on.

23.4.2. Logic Pins

The following pins are individual pins to the F159V to reset the device, enable the channel modulator output ports, and enable the channel amplifiers.

Table 29. Amplifier Enable Pin Truth Table

Parameter	Logic Level	Function
CH0_AMPEN (pin 68) CH1_AMPEN (pin 18)	LOW	Amplifier in channel path has the DC power turned on.
	HIGH or No Connect	Amplifier in channel path has the DC power turned off.

Table 30. Coupled Modulator Output Enable Pin Truth Table

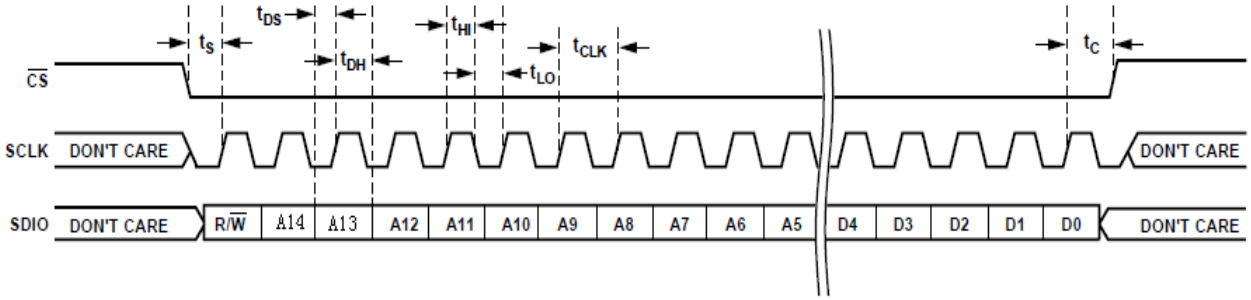
Parameter	Logic Level	Function
CH0_MODEN (pin 59) CH1_MODEN (pin 27)	LOW	Coupled modulator output path has the DC power turned on.
	HIGH or No Connect	Coupled modulator output path has the DC power turned off.

Table 31. RESET Pin Truth Table

Parameter	Logic Level	Function
RESET (pin 49)	LOW	Resets all registers to the default states.
	HIGH or No Connect	Normal operation.

24. Programming

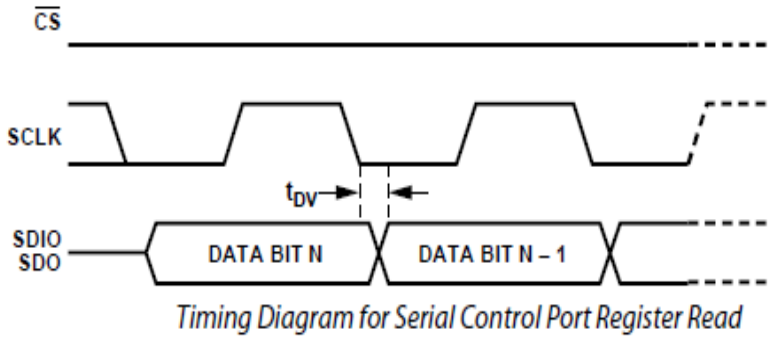
Figure 95. Serial Timing Diagram



Serial Control Port Write—MSB First, 16-Bit Instruction, Timing Measurements

Note: Falling edge of the last clock period is required in order to properly program the SPI.

Figure 96. Serial Timing Diagram for Multiple Bits



Timing Diagram for Serial Control Port Register Read

Table 32. SPI Timing Parameters

Parameter	Description	Minimum for SPI Timing (ns)	Maximum for SPI Timing (ns)
t_{ds}	SDIO to SCLK rising edge Setup	8	10
t_{dh}	SCLK rising edge to SDIO Hold	8	10
t_{clk}	Period of SCLK	50 (default)	
t_{hi}	High width of SPI clock	25	
t_{lo}	Low width of SPI clock	25	
t_s	CS falling edge to SCLK rising edge, setup time	10	
t_c	SCLK rising edge to CS rising edge, hold time	20	30
t_{dv}	SCLK falling edge to valid readback data, SDIO/SDO, t_{dv}		10

24.1. Special Programming Note

LD Mode must be programmed to be logic HIGH for proper operation of the lock detection circuit. This is set in Register 37 and the digital word to be used is 129 = 81h = 1000_0001b.

24.2. Register Definition

The F159V is programmed via a 3 or 4 wire SPI connection. There are 50 registers that can be programmed for various components of the device including the PLL, voltage variable attenuators, digital step attenuators, LO output power. Each register is 8-bits long. There are some parameters that require two registers to fulfill the functionality.

Note: The following numbering nomenclature is used. If the letter "h" is after characters, the number is a hexadecimal. If "b" follows characters, the number is binary. The binary number is also separated into groups of 4 bits (e.g., 1010_0011b). Otherwise, the number is decimal.

Table 33. Register Definition

Register	Hex Address	Type	Default Value	Description
0	00h	R/W	0000_0000b	This register configures the Reset and bit definition.
1	01h	R/W	0000_0000b	This register configures the Single instruction.
2	02h	R/W	0000_0000b	This register configures the data transfer.
3	03h	R	0000_0001b	Chip type.
4	04h	R	0000_0000b	Chip ID – lower 8 bits (total 16 bits).
5	05h	R	0000_0000b	Chip ID – higher 8 bits (total 16 bits).
6	06h	R	0000_0011b	Chip version.
7	07h	R/W	0000_0000b	Unused at this time.
8	08h	R/W	0000_0000b	Unused at this time.
9	09h	R/W	0000_0000b	Unused at this time.
10	0Ah	R/W	0000_0000b	Unused at this time.
11	0Bh	R/W	0000_0000b	Unused at this time.
12	0Ch	R	0010_0110b	Vendor ID – lower 8 bits (total of 16 bits).
13	0Dh	R	0000_0100b	Vendor ID – higher 8 bits (total of 16 bits).
14	0Eh	R/W	0000_0000b	Unused at this time.
15	0Fh	R/W	0000_0000b	Unused at this time.
16	10h	R/W	0001_0000b	5-bit word to control the Reference Divider and Reference Doubler.
17	11h	R/W	0011_1111b	FB divider integer part, lower 8 bits (total of 16 bits). Minimum divide ratio is 7.
18	12h	R/W	0000_0000b	FB divider integer part, higher 8 bits (total of 16-bits).
19	13h	R/W	0000_0000b	FB divider fractional numerator, lower 8 bits (total of 16 bits). Default = 31,232.
20	14h	R/W	0111_1010b	FB divider fractional numerator, higher 8 bits (total of 16-bits).
21	15h	R/W	1111_1111b	FB divider fractional denominator, lower 8 bits (total of 16 bits). Minimum modulus value is 2. Default = 65,535.
22	16h	R/W	1111_1111b	FB divider fractional denominator, higher 8 bits (total of 16 bits).
23	17h	R/W	0000_0001b	1-bit for the Quadrature Divider, 3-bit for the output divider.
24	18h	R/W	0000_0010b	Charge pump current setting, 4 bits.

Table 34. Register Definition–(Cont.)

Register	Hex Address	Type	Default Value	Description
25	19h	R/W	0000_0101b	Setting for LO output: 2 bits for Output Power, 2 bits for Switched Output Power, 1 bit for additional pre-driver current (output power).
26	1Ah	R/W	0001_1100b	Set the various LO switch parameters, and if the PLL and DAC are enabled.
27	1Bh	R/W	0000_0000b	5-bit word to control the DSA in Channel 0 (1dB LSB).
28	1Ch	R/W	0000_0000b	5-bit word to control the DSA in Channel 1 (1dB LSB).
29	1Dh	R/W	1111_1111b	Lower 8 bits of 11-bit word to control the VVA in Channel 0.
30	1Eh	R/W	0000_0111b	Higher 3 bits of 11-bit word to control the VVA in Channel 0.
31	1Fh	R/W	1111_1111b	Lower 8-bits of 11-bit word to control the VVA in Channel 1.
32	20h	R/W	0000_0111b	Higher 3-bits of 11-bit word to control the VVA in Channel 1.
33	21h	R/W	0000_0000b	1 bit for the RF Band, 1 bit for the LO Band.
34	22h	R/W	0000_0000b	1 bit for Digital Output Logic.
35	23h	R/W	0000_0000b	3 bits for Lock Detect Precision, 2 bits for Lock Detect.
36	24h	R/W	0000_0000b	1 bit for a force recalibration. 1 bit for Disabling the VCO recalibration, 1 bit for Automatic recalibration.
37	25h	R/W	0000_0001b	1 bit for Lock Detection.
38	26h	R/W	0000_0000b	Lower 8 bits of a 12-bit word for the Band Select Divider.
39	27h	R/W	0000_0001b	Higher 4 bits of a 12-bit word for the Band Select Divider.
40	28h	R/W	0000_0000b	Reserved for Vendor Use. Use only the default value.
41	29h	R/W	0000_0000b	Reserved for Vendor Use. Use only the default value.
42	2Ah	R/W	0000_0010b	Reserved for Vendor Use. Use only the default value.
43	2Bh	R/W	1100_1011b	Reserved for Vendor Use. Use only the default value.
44	2Ch	R/W	0000_0000b	Reserved for Vendor Use. Use only the default value.
45	2Dh	R/W	0000_0000b	Reserved for Vendor Use. Use only the default value.
46	2Eh	R	N/A	Reserved for Vendor Use. Use only the default value.
47	2Fh	R	N/A	Reserved for Vendor Use. Use only the default value.
48	30h	R	N/A	Reserved for Vendor Use. Use only the default value.
49	31h	R/W	N/A	Reserved for Vendor Use. Use only the default value.

24.2.1. Register 0 (00h)

This register sets how the entire serial communication functions. Since the device can use either the most significant bit (MSB) or least significant bit (LSB) order, only four parameters are set. By mirroring the bits, the parameters can be used properly in either mode. The default value is 0 = 00h = 0000_0000b.

Table 35. Register 0: Bit Definition

Bit	Bit Field Name	Default	Definition
0	SoftReset	0	Set to logic LOW is for normal operation. Set to logic HIGH to reset all registers above register 2 (02h), with write capability, to a default state. Registers 0 and 1 are not reset.
1	LSBFirst	0	Defines the bit transmitted first in SPIN transfers between the master and slave. If this bit is set to logic LOW, data is oriented as MSB first. If this bit is set to logic HIGH, data is oriented as LSB first.
2	AddressAscend	0	Defines how the addresses are incremented in streaming SPI mode. If this bit is set to logic LOW, addresses are auto-decremented. If this bit is set to logic HIGH, addresses are auto-incremented.
3	SDO Active	0	Selects the unidirectional or bidirectional data transfer mode for the SDIO pin. If this bit is cleared or set to logic LOW, then SPI 3-wire mode is used and: - SDIO is the SPI bidirectional data I/O pin - SDO pin is not used and is in high-impedance If this-bit is cleared or set to logic HIGH, then SPI 4-wire mode is used and: - SDIO is the SPI data input pin - SDO is the SPI data output pin
4	SDO Active	0	Must be equal to bit 3 (Mirror image to be independent of MSB or LSB).
5	AddressAscend	0	Must be equal to bit 2 (Mirror image to be independent of MSB or LSB).
6	LSBFirst	0	Must be equal to bit 1 (Mirror image to be independent of MSB or LSB).
7	SoftReset	0	Must be equal to bit 0 (Mirror image to be independent of MSB or LSB).

24.2.2. Register 1 (01h)

This register is used to determine how data is read back from the device. The default value is 0 = 00h = 0000_0000b.

Table 36. Register 1: Bit Definition

Bit	Bit Field Name	Default	Definition
0		0	Unused.
1		0	Unused.
2		0	Unused.
3		0	Unused.
4		0	Unused.
5	BufferReadMode	0	Double Buffer. Vendor can choose to design in a secondary buffer for reading. If set for logic HIGH, then when reading from the device the information is obtained for the second buffer. If set for logic LOW, then when reading from the device the information is obtained for the active register.
6		0	Unused.
7		0	Unused.

24.2.3. Register 2 (01h)

This register is unused and reserved for future use. The default value is 0 = 00h = 0000_0000b.

24.2.4. Register 3 (03h)

This register is used to define what type of Chip this is and is READ ONLY. It is 8 bits long. The default value is 1 = 01h = 0000_0001b.

Table 37. Register 3: Bit Definition

Bit	Bit Field Name	Default	Definition
0	ChipType[0]	1	Bit 0 of the value.
1	ChipType[1]	0	Bit 1 of the value.
2	ChipType[2]	0	Bit 2 of the value.
3	ChipType[3]	0	Bit 3 of the value.
4	ChipType[4]	0	Bit 4 of the value.
5	ChipType[5]	0	Bit 5 of the value.
6	ChipType[6]	0	Bit 6 of the value.
7	ChipType[7]	0	Bit 7 of the value.

24.2.5. Register 4 (04h)

Register 5 and 4 define the value for the ChipID. The ChipID is a 16-bit word with a default value of 0 = 0000h = 0000_0000_0000_0000b. Register 4 is the lower 8 bits of the word and the default value is 0 = 00h = 0000_0000b. This register is READ ONLY.

Table 38. Register 4: Bit Definition

Bit	Bit Field Name	Default	Definition
0	ChipID[0]	0	Bit 0 of the value.
1	ChipID[1]	0	Bit 1 of the value.
2	ChipID[2]	0	Bit 2 of the value.
3	ChipID[3]	0	Bit 3 of the value.
4	ChipID[4]	0	Bit 4 of the value.
5	ChipID[5]	0	Bit 5 of the value.
6	ChipID[6]	0	Bit 6 of the value.
7	ChipID[7]	0	Bit 7 of the value.

24.2.6. Register 5 (05h)

Register 5 and 4 define the value for the ChipID. The ChipID is a 16-bit word with a default value of 0 = 0000h = 0000_0000_0000_0000b. Register 5 is the higher 8 bits of the word and the default value is 0 = 00h = 0000_0000b. This register is READ ONLY.

Table 39. Register 5: Bit Definition

Bit	Bit Field Name	Default	Definition
0	ChipID[8]	0	Bit 8 of the value.
1	ChipID[9]	0	Bit 9 of the value.
2	ChipID[10]	0	Bit 10 of the value.
3	ChipID[11]	0	Bit 11 of the value.
4	ChipID[12]	0	Bit 12 of the value.
5	ChipID[13]	0	Bit 13 of the value.
6	ChipID[14]	0	Bit 14 of the value.
7	ChipID[15]	0	Bit 15 of the value.

24.2.7. Register 6 (06h)

This register is READ ONLY and contains the Chip Version value. The Chip Version is an 8-bit word. The default value is 3 = 03h= 0000_0011b.

Table 40. Register 6: Bit Definition

Bit	Bit Field Name	Default	Definition
0	ChipVersion[0]	1	Bit 0 of the value.
1	ChipVersion[1]	1	Bit 1 of the value.
2	ChipVersion[2]	0	Bit 2 of the value.
3	ChipVersion[3]	0	Bit 3 of the value.
4	ChipVersion[4]	0	Bit 4 of the value.
5	ChipVersion[5]	0	Bit 5 of the value.
6	ChipVersion[6]	0	Bit 6 of the value.
7	ChipVersion[7]	0	Bit 7 of the value.

24.2.8. Register 7 (07h)

This register is unused and reserved for future use. The default value is 0 = 00h = 0000_0000b.

24.2.9. Register 8 (08h)

This register is unused and reserved for future use. The default value is 0 = 00h = 0000_0000b.

24.2.10. Register 9 (09h)

This register is unused and reserved for future use. The default value is 0 = 00h = 0000_0000b.

24.2.11. Register 10 (0Ah)

This register is unused and reserved for future use. The default value is 0 = 00h = 0000_0000b.

24.2.12. Register 11 (0Bh)

This register is unused and reserved for future use. The default value is 0 = 00h = 0000_0000b.

24.2.13. Register 12 (0Ch)

Register 13 and 12 define the value of the Vendor ID. The Vendor ID is a 16-bit word. IDT's vendor code is 1062 = 0426h. Register 12 is the lower 8 bits of the word and the default value is 38 = 26h= 0010_0110b. This register is READ ONLY.

Table 41. Register 12: Bit Definition

Bit	Bit Field Name	Default	Definition
0	VendorID[0]	0	Bit 0 of the value.
1	VendorID[1]	1	Bit 1 of the value.
2	VendorID[2]	1	Bit 2 of the value.
3	VendorID[3]	0	Bit 3 of the value.
4	VendorID[4]	0	Bit 4 of the value.
5	VendorID[5]	1	Bit 5 of the value.
6	VendorID[6]	0	Bit 6 of the value.
7	VendorID[7]	0	Bit 7 of the value.

24.2.14. Register 13 (0Dh)

Register 13 and 12 define the value of the Vendor ID. The Vendor ID is a 16-bit word. IDT's vendor code is 1062 = 0426h. Register 13 is the higher 8 bits of the word and the default value is 4 = 04h= 0000_0100b. This register is READ ONLY.

Table 42. Register 13: Bit Definition

Bit	Bit Field Name	Default	Definition
0	VendorID[8]	0	Bit 8 of the value.
1	VendorID[9]	0	Bit 9 of the value.
2	VendorID[10]	1	Bit 10 of the value.
3	VendorID[11]	0	Bit 11 of the value.
4	VendorID[12]	0	Bit 12 of the value.
5	VendorID[13]	0	Bit 13 of the value.
6	VendorID[14]	0	Bit 14 of the value.
7	VendorID[15]	0	Bit 15 of the value.

24.2.15. Register 14 (0Eh)

This register is unused and reserved for future use. The default value is 0 = 00h = 0000_0000b.

24.2.16. Register 15 (0Fh)

This register determines how the data in transferred from the buffers in the active register when a multi-byte word is sent. The default value is 0 = 00h= 0000_0000b.

Table 43. Register 15: Bit Definition

Bit	Bit Field Name	Default	Definition
0	TransferOn	0	This device implements double-buffered registers for various parameters that are larger than one byte (8 bits). If this is set to logic LOW, then there is no transfer. If this is set to logic HIGH, then the data (multiple bytes) into the device is synchronized so as to not affect the operation of the device. This bit is always reset to logic LOW 0 after the operation, and this is called Auto-Clear.
1		0	Unused.
2		0	Unused.
3		0	Unused.
4		0	Unused.
5		0	Unused.
6		0	Unused.
7		0	Unused.

24.2.17. Register 16 (10h)

This register controls the Reference Frequency Divider within the PLL. The reference frequency can be first be doubled, then divided. The default value is 16 = 10h = 0001_0000b.

Table 44. Register 16: Bit Definition

Bit	Bit Field Name	Default	Definition
0	R[0]	0	Bit 0 of a 4-bit word to determine the divider ratio (R) of the reference frequency (Table 45).
1	R[1]	0	Bit 1 of a 4-bit word to determine the divider ratio (R) of the reference frequency (Table 45).
2	R[2]	0	Bit 2 of a 4-bit word to determine the divider ratio (R) of the reference frequency (Table 45).
3	R[3]	0	Bit 3 of a 4-bit word to determine the divider ratio (R) of the reference frequency (Table 45).
4	RefDoub	1	If this is set to logic LOW, then the reference frequency doubler (D) is disabled (multiplier is set for 1). If this is set to logic HIGH, then the reference frequency doubler (D) is enable (multiplier is set for 2). This is the default value.
5		0	Unused.
6		0	Unused.
7		0	Unused.

Table 45. 4-bit Pre Divider Value (R) Description

Decimal	Bit 3	Bit 2	Bit 1	Bit 0	Definition
0	0	0	0	0	Divide by 1 (default)
1	0	0	0	1	Divide by 1
2	0	0	1	0	Divide by 2
3	0	0	1	1	Divide by 3
4	0	1	0	0	Divide by 4
5	0	1	0	1	Divide by 5
6	0	1	1	0	Divide by 6
7	0	1	1	1	Divide by 7
8	1	0	0	0	Divide by 8
9	1	0	0	1	Divide by 9
10	1	0	1	0	Divide by 10
11	1	0	1	1	Divide by 11
12	1	1	0	0	Divide by 12
13	1	1	0	1	Divide by 13
14	1	1	1	0	Divide by 14
15	1	1	1	1	Divide by 15

24.2.18. Register 17 (11h)

Registers 18 and 17 control the Feedback Frequency Divider within the PLL. This is a 16-bit word that gives the integer value of the divider. The integer can vary from 7 to 65,535. The default value is 63 = 003Fh = 0000_0000_0011_1111b. Register 17 is the lower 8 bits of the word and has a default value 63 = 3Fh = 0011_1111b.

Table 46. Register 17: Bit Definition

Bit	Bit Field Name	Default	Definition
0	NInt[0]	1	Bit 0 of a 16-bit word to determine Integer value for the feedback divider.
1	NInt[1]	1	Bit 1 of a 16-bit word to determine Integer value for the feedback divider.
2	NInt[2]	1	Bit 2 of a 16-bit word to determine Integer value for the feedback divider.
3	NInt[3]	1	Bit 3 of a 16-bit word to determine Integer value for the feedback divider.
4	NInt[4]	1	Bit 4 of a 16-bit word to determine Integer value for the feedback divider.
5	NInt[5]	1	Bit 5 of a 16-bit word to determine Integer value for the feedback divider.
6	NInt[6]	0	Bit 6 of a 16-bit word to determine Integer value for the feedback divider.
7	NInt[7]	0	Bit 7 of a 16-bit word to determine Integer value for the feedback divider.

24.2.19. Register 18 (12h)

Registers 18 and 17 control the Feedback Frequency Divider within the PLL. This is a 16-bit word that gives the integer value of the divider. The integer can vary from 7 to 65,535. The default value is 63 = 003Fh = 0000_0000_0011_1111b. Register 18 is the higher 8 bits of the word and has a default value of 0 = 00h = 0000_0000b.

Table 47. Register 18: Bit Definition

Bit	Bit Field Name	Default	Definition
0	NInt[8]	0	Bit 8 of a 16-bit word to determine integer value for the feedback divider.
1	NInt[9]	0	Bit 9 of a 16-bit word to determine integer value for the feedback divider.
2	NInt[10]	0	Bit 10 of a 16-bit word to determine integer value for the feedback divider.
3	NInt[11]	0	Bit 11 of a 16-bit word to determine integer value for the feedback divider.
4	NInt[12]	0	Bit 12 of a 16-bit word to determine integer value for the feedback divider.
5	NInt[13]	0	Bit 13 of a 16-bit word to determine integer value for the feedback divider.
6	NInt[14]	0	Bit 14 of a 16-bit word to determine integer value for the feedback divider.
7	NInt[15]	0	Bit 15 of a 16-bit word to determine integer value for the feedback divider.

24.2.20. Register 19 (13h)

Registers 20 and 19 control the NFrac term, which is the numerator in the fractional part of the equation for the PLL's Feedback Frequency Divider: NInt + (NFrac / NMod). NFrac is a 16-bit word that can vary from 0 to 65,535. There is a restriction that NFrac must be less than the denominator value NMod (see registers 21 and 22). The default value for NFrac is 31232 = 7A00h = 0111_1010_0000_0000b. Register 19 is the lower 8 bits of NFrac, and its default value is 0 = 00h = 0000_0000b.

Table 48. Register 19: Bit Definition

Bit	Bit Field Name	Default	Definition
0	NFrac[0]	0	Bit 0 in the 16-bit NFrac numerator in the fraction term in the feedback divider equation.
1	NFrac[1]	0	Bit 1 in the 16-bit NFrac numerator in the fraction term in the feedback divider equation.
2	NFrac[2]	0	Bit 2 in the 16-bit NFrac numerator in the fraction term in the feedback divider equation.
3	NFrac[3]	0	Bit 3 in the 16-bit NFrac numerator in the fraction term in the feedback divider equation.
4	NFrac[4]	0	Bit 4 in the 16-bit NFrac numerator in the fraction term in the feedback divider equation.
5	NFrac[5]	0	Bit 5 in the 16-bit NFrac numerator in the fraction term in the feedback divider equation.
6	NFrac[6]	0	Bit 6 in the 16-bit NFrac numerator in the fraction term in the feedback divider equation.
7	NFrac[7]	0	Bit 7 in the 16-bit NFrac numerator in the fraction term in the feedback divider equation.

24.2.21. Register 20 (14h)

Registers 20 and 19 control the NFrac term, which is the numerator in the fractional part of the equation for the PLL's Feedback Frequency Divider: NInt + (NFrac / NMod). NFrac is a 16-bit word that can vary from 0 to 65,535. There is a restriction that NFrac must be less than the denominator value NMod (see registers 21 and 22). The default value for NFrac is 31232 = 7A00h = 0111_1010_0000_0000b. Register 20 is the upper 8 bits of NFrac, and its default value is 122 = 7Ah = 0111_1010b.

Table 49. Register 20: Bit Definition

Bit	Bit Field Name	Default	Definition
0	NFrac[8]	0	Bit 8 in the 16-bit NFrac numerator in the fraction term in the feedback divider equation.
1	NFrac[9]	1	Bit 9 in the 16-bit NFrac numerator in the fraction term in the feedback divider equation.
2	NFrac[10]	0	Bit 10 in the 16-bit NFrac numerator in the fraction term in the feedback divider equation.
3	NFrac[11]	1	Bit 11 in the 16-bit NFrac numerator in the fraction term in the feedback divider equation.
4	NFrac[12]	1	Bit 12 in the 16-bit NFrac numerator in the fraction term in the feedback divider equation.
5	NFrac[13]	1	Bit 13 in the 16-bit NFrac numerator in the fraction term in the feedback divider equation.
6	NFrac[14]	1	Bit 14 in the 16-bit NFrac numerator in the fraction term in the feedback divider equation.
7	NFrac[15]	0	Bit 15 in the 16-bit NFrac numerator in the fraction term in the feedback divider equation.

24.2.22. Register 21 (15h)

Registers 22 and 21 control the NMod term, which is the denominator in the fractional part of the equation for the PLL's Feedback Frequency Divider: NInt + (NFrac / NMod). NMod is a 16-bit word that can vary from 2 to 65,535. There is a restriction that NMod must be greater than the numerator NFrac value (see registers 19 and 20). The default value for NMod is 65535 = FFFFh = 1111_1111_1111_1111b. Register 21 is the lower 8 bits of NMod, and its default value is 255 = FFh = 1111_1111b.

Table 50. Register 21: Bit Definition

Bit	Bit Field Name	Default	Definition
0	NMod[0]	1	Bit 0 in the 16-bit NMod denominator in the fraction term in the feedback divider equation.
1	NMod[1]	1	Bit 1 in the 16-bit NMod denominator in the fraction term in the feedback divider equation.
2	NMod[2]	1	Bit 2 in the 16-bit NMod denominator in the fraction term in the feedback divider equation.
3	NMod[3]	1	Bit 3 in the 16-bit NMod denominator in the fraction term in the feedback divider equation.
4	NMod[4]	1	Bit 4 in the 16-bit NMod denominator in the fraction term in the feedback divider equation.
5	NMod[5]	1	Bit 5 in the 16-bit NMod denominator in the fraction term in the feedback divider equation.
6	NMod[6]	1	Bit 6 in the 16-bit NMod denominator in the fraction term in the feedback divider equation.
7	NMod[7]	1	Bit 7 in the 16-bit NMod denominator in the fraction term in the feedback divider equation.

24.2.23. Register 22 (16h)

Registers 22 and 21 control the NMod term, which is the denominator in the fractional part of the equation for the PLL's Feedback Frequency Divider: NInt + (NFrac / NMod). NMod is a 16-bit word that can vary from 2 to 65,535. There is a restriction that NMod must be greater than the numerator NFrac value (see registers 19 and 20). The default value for NMod is 65535 = FFFFh = 1111_1111_1111_1111b. Register 22 is the upper 8 bits of NMod, and its default value is 255 = FFh = 1111_1111b.

Table 51. Register 22: Bit Definition

Bit	Bit Field Name	Default	Definition
0	NMod[8]	1	Bit 8 in the 16-bit NMod denominator in the fraction term in the feedback divider equation.
1	NMod[9]	1	Bit 9 in the 16-bit NMod denominator in the fraction term in the feedback divider equation.
2	NMod[10]	1	Bit 10 in the 16-bit NMod denominator in the fraction term in the feedback divider equation.
3	NMod[11]	1	Bit 11 in the 16-bit NMod denominator in the fraction term in the feedback divider equation.
4	NMod[12]	1	Bit 12 in the 16-bit NMod denominator in the fraction term in the feedback divider equation.
5	NMod[13]	1	Bit 13 in the 16-bit NMod denominator in the fraction term in the feedback divider equation.
6	NMod[14]	1	Bit 14 in the 16-bit NMod denominator in the fraction term in the feedback divider equation.
7	NMod[15]	1	Bit 15 in the 16-bit NMod denominator in the fraction term in the feedback divider equation.

24.2.24. Register 23 (17h)

Register 23 creates the proper frequency that is used by the modulator. There are two separate dividers. The Quad Divider is a divide by 2 and will work with both the internal frequency generator and an external frequency generator. The other divider, MDiv, only works on the internal frequency generator and is 3-bit word that allows values of 1 to 8. The Quad Divider default is 0 and the other divider, MDiv, is 1. Bits 4 to 7 are not used. The default value is 1 = 01h = 0000_0001b.

Table 52. Register 23: Bit Definition

Bit	Bit Field Name	Default	Definition
0	MDiv[0]	1	Bit 0 of 3-bit word for divider (see Table 53).
1	MDiv[1]	0	Bit 1 of 3-bit word for divider (see Table 53).
2	MDiv[2]	0	Bit 2 of 3-bit word for divider (see Table 53).
3	Quad_Divider	0	Quadrature Divider. Set for logic LOW for divide by 1. This is the default value. Set for logic HIGH for divide by 2.
4		0	Unused.
5		0	Unused.
6		0	Unused.
7		0	Unused.

Table 53. 3-Bit Divider Value (MDiv) Description

Decimal	Bit 2	Bit 1	Bit 0	Definition
0	0	0	0	Divide by 1
1	0	0	1	Divide by 2 (default)
2	0	1	0	Divide by 4
3	0	1	1	Divide by 8
4	1	0	0	Unused
5	1	0	1	Unused
6	1	1	0	Unused
7	1	1	1	Unused

24.2.25. Register 24 (18h)

This register changes the characteristics of the charge pump. This is a 4-bit word that will adjust the current of the charge pump. The default current is 0.94mA. Bits 4 to 7 are not used. The default value is 2 = 02h = 0000_0010b.

Table 54. Register 24: Bit Definition

Bit	Bit Field Name	Default	Definition
0	ChrgPmp[0]	0	Bit 0 of 4-bit word for charge pump current (see Table 55).
1	ChrgPmp[1]	1	Bit 1 of 4-bit word for charge pump current (see Table 55).
2	ChrgPmp[2]	0	Bit 2 of 4-bit word for charge pump current (see Table 55).
3	ChrgPmp[3]	0	Bit 3 of 4-bit word for charge pump current (see Table 55).
4		0	Unused.
5		0	Unused.
6		0	Unused.
7		0	Unused.

Table 55. 4-Bit Charge Pump Current

Decimal	Bit 3	Bit 2	Bit 1	Bit 0	Definition
0	0	0	0	0	Set current for 0.31mA
1	0	0	0	1	Set current for 0.63mA
2	0	0	1	0	Set current for 0.94mA (default)
3	0	0	1	1	Set current for 1.25mA
4	0	1	0	0	Set current for 1.56mA
5	0	1	0	1	Set current for 1.88mA
6	0	1	1	0	Set current for 2.19mA
7	0	1	1	1	Set current for 2.50mA
8	1	0	0	0	Set current for 2.81mA
9	1	0	0	1	Set current for 3.13mA
10	1	0	1	0	Set current for 3.44mA
11	1	0	1	1	Set current for 3.75mA
12	1	1	0	0	Set current for 4.06mA
13	1	1	0	1	Set current for 4.38mA
14	1	1	1	0	Set current for 4.69mA
15	1	1	1	1	Set current for 5.00mA

24.2.26. Register 25 (19h)

This register controls the LO power levels for the modulator and external LO port. Each power level defaults to 0dBm. If needed, the modulator LO power can be increased by setting a 1 bit word. Bits 5 to 7 are unused. The register default is 5 = 05h = 0000_0101b.

Table 56. Register 25: Bit Definition

Bit	Bit Field Name	Default	Definition
0	LO_Out_Pwr[0]	1	Bit 0 of a 2-bit word to set the LO power to the modulator (see Table 57).
1	LO_Out_Pwr[1]	0	Bit 1 of a 2-bit word to set the LO power to the modulator (see Table 57).
2	LO_SW_Out_Pwr[0]	1	Bit 0 of a 2-bit word to set LO power to the external port (see Table 58).
3	LO_SW_Out_Pwr[1]	0	Bit 1 of a 2-bit word to set LO power to the external port (see Table 58).
4	LO_Out_Pwr_extra	0	If this bit is set for logic HIGH, then the LO predriver increases the output power to the modulator. The addition power is different for each of the LO_Out_Pwr settings. If this bit is set for logic LOW (default), then the LO predriver will not increase the output power.
5		0	Unused.
6		0	Unused.
7		0	Unused.

Table 57. 2-Bit Power Setting for the Modulator Signal

Decimal	Bit 1	Bit 0	Definition
0	0	0	Set for -2dBm
1	0	1	Set for 0dBm (default)
2	1	0	Set for +2dBm
3	1	1	Set for +4dBm

Table 58. 2-Bit LO Power for the External LO Port (LO_OUT)

Decimal	Bit 1	Bit 0	Definition
0	0	0	Set for -2dBm
1	0	1	Set for 0dBm (default)
2	1	0	Set for +2dBm
3	1	1	Set for +4dBm

24.2.27. Register 26 (1Ah)

This register controls the LO Switch matrix. There are five single-bit words for various configurations. Bits 6 and 7 are unused. The default value is 28 = 1Ch = 0001_1100b.

Table 59. Register 26: Bit Definition

Bit	Bit Field Name	Default	Definition
0	LO_IN_Enable	0	This bit turns on the signal buffer that allows an external LO signal to be used as the signal for the modulator. If this bit is set for logic LOW (default), then the buffer is turned off. If this bit is set for logic HIGH, then the buffer is turned on. This bit works with bit LO_SW_Out_Select to use an external signal for the LO.
1	LO_Out_Enable	0	This bit turns on the signal buffer that allows the LO signal to be sent to other devices. If this bit is set for logic LOW (default), then the buffer is turned off. If this bit is set for logic HIGH, then the buffer is turned on.
2	LO_SW_Out_Enable	1	This bit turns on the switch buffer that controls which signal to use for modulator. If this bit is set for logic LOW then the buffer is turned off. If this bit is set for logic HIGH (default), then the buffer is turned on.
3	DAC_Enable	1	This bit allows the DAC to control the VVAs. If this bit is set for logic LOW, then the DAC is disabled. If this bit is set for logic HIGH (default), then the DAC is enabled.
4	PLL_Enable	1	This bit controls power to the PLL. If this bit is set for logic LOW, then the power to the PLL is disabled for minimum current. If this bit is set for logic HIGH (default), then the power to the PLL is enabled.
5	LO_SW_Out_Select	0	This bit selects which signal is used for the modulator. If this bit is set for logic LOW (default), then the internal signal from the PLL is used. If this bit is set for logic HIGH, then the external signal from LO_IN is used.
6		0	Unused.
7		0	Unused.

24.2.28. Register 27 (1Bh)

This register controls the Digital Step Attenuator in Channel 0. This is a 5-bit word. Bits 5 to 7 are unused. The default is 0dB, 0 = 00h = 0000_0000b.

Table 60. Register 27: Bit Definition

Bit	Bit Field Name	Default	Definition
0	DSA0[0]	0	Bit 0 of a 5-bit word to set the DSA for Channel 0 (see Table 61).
1	DSA0[1]	0	Bit 1 of a 5-bit word to set the DSA for Channel 0 (see Table 61).
2	DSA0[2]	0	Bit 2 of a 5-bit word to set the DSA for Channel 0 (see Table 61).
3	DSA0[3]	0	Bit 3 of a 5-bit word to set the DSA for Channel 0 (see Table 61).
4	DSA0[4]	0	Bit 4 of a 5-bit word to set the DSA for Channel 0 (see Table 61).
5		0	Unused.
6		0	Unused.
7		0	Unused.

Table 61. 5-Bit Digital Attenuator Setting used for both DSA0 and DSA1

Decimal	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Definition
0	0	0	0	0	0	0dB (default)
1	0	0	0	0	1	1dB
2	0	0	0	1	0	2dB
4	0	0	1	0	0	4dB
8	0	1	0	0	0	8dB
16	1	0	0	0	0	16dB
31	1	1	1	1	1	31dB

24.2.29. Register 28 (1Ch)

This register controls the Digital Step Attenuator in Channel 1. This is a 5-bit word. Bits 5 to 7 are unused. The default is 0dB, 0 = 0h = 0000_0000b.

Table 62. Register 28: Bit Definition

Bit	Bit Field Name	Default	Definition
0	DSA1[0]	0	Bit 0 of a 5-bit word to set the DSA for Channel 1 (see Table 61).
1	DSA1[1]	0	Bit 1 of a 5-bit word to set the DSA for Channel 1 (see Table 61).
2	DSA1[2]	0	Bit 2 of a 5-bit word to set the DSA for Channel 1 (see Table 61).
3	DSA1[3]	0	Bit 3 of a 5-bit word to set the DSA for Channel 1 (see Table 61).
4	DSA1[4]	0	Bit 4 of a 5-bit word to set the DSA for Channel 1 (see Table 61).
5		0	Unused.
6		0	Unused.
7		0	Unused.

24.2.30. Register 29 (1Dh)

Registers 30 and 29 control the Voltage Variable Attenuator in Channel 0, and is an 11-bit word. The minimum attenuation (0dB) is at the maximum DAC setting (2047). The default is 2047 = 7FFh = 111_1111_1111b. Register 29 is the lower 8 bits of the word and the default is 255 = FFh = 1111_1111b.

Table 63. Register 29: Bit Definition

Bit	Bit Field Name	Default	Definition
0	DAC0[0]	1	Bit 0 of an 11-bit word to set the VVA for Channel 0.
1	DAC0[1]	1	Bit 1 of an 11-bit word to set the VVA for Channel 0.
2	DAC0[2]	1	Bit 2 of an 11-bit word to set the VVA for Channel 0.
3	DAC0[3]	1	Bit 3 of an 11-bit word to set the VVA for Channel 0.
4	DAC0[4]	1	Bit 4 of an 11-bit word to set the VVA for Channel 0.
5	DAC0[5]	1	Bit 5 of an 11-bit word to set the VVA for Channel 0.
6	DAC0[6]	1	Bit 6 of an 11-bit word to set the VVA for Channel 0.
7	DAC0[7]	1	Bit 7 of an 11-bit word to set the VVA for Channel 0.

24.2.31. Register 30 (1Eh)

Registers 30 and 29 control the Voltage Variable Attenuator in Channel 0, and is an 11-bit word. The minimum attenuation (0dB) is at the maximum DAC setting (2047). The default is 2047 = 7FFh = 111_1111_1111b. Bits 3 to 7 of this register are unused. Register 30 is the higher 3 bits of the word and the default is 7 = 7h = 0000_0111b.

Table 64. Register 30: Bit Definition

Bit	Bit Field Name	Default	Definition
0	DAC0[8]	1	Bit 8 of an 11-bit word to set the VVA for Channel 0.
1	DAC0[9]	1	Bit 9 of an 11-bit word to set the VVA for Channel 0.
2	DAC0[10]	1	Bit 10 of an 11-bit word to set the VVA for Channel 0.
3	Unused	0	Unused.
4	Unused	0	Unused.
5	Unused	0	Unused.
6	Unused	0	Unused.
7	Unused	0	Unused.

24.2.32. Register 31 (1Fh)

Registers 32 and 31 control the Voltage Variable Attenuator in Channel 1, and is an 11-bit word. The minimum attenuation (0dB) is at the maximum DAC setting (2047). The default is 2047 = 7FFh = 111_1111_1111b. . Register 31 is the lower 8 bits of the word and the default is 255 = FFh = 1111_1111b.

Table 65. Register 31: Bit Definition

Bit	Bit Field Name	Default	Definition
0	DAC1[0]	1	Bit 0 of an 11-bit word to set the VVA for Channel 1.
1	DAC1[1]	1	Bit 1 of an 11-bit word to set the VVA for Channel 1.
2	DAC1[2]	1	Bit 2 of an 11-bit word to set the VVA for Channel 1.
3	DAC1[3]	1	Bit 3 of an 11-bit word to set the VVA for Channel 1.
4	DAC1[4]	1	Bit 4 of an 11-bit word to set the VVA for Channel 1.
5	DAC1[5]	1	Bit 5 of an 11-bit word to set the VVA for Channel 1.
6	DAC1[6]	1	Bit 6 of an 11-bit word to set the VVA for Channel 1.
7	DAC1[7]	1	Bit 7 of an 11-bit word to set the VVA for Channel 1.

24.2.33. Register 32 (20h)

Registers 32 and 31 control the Voltage Variable Attenuator in Channel 1, and is an 11-bit word. The minimum attenuation (0dB) is at the maximum DAC setting (2047). The default is 2047 = 7FFh = 111_1111_1111b. Bits 3 to 7 of this register are unused. Register 30 is the higher 3 bits of the word and the default is 7 = 7h = 0000_0111b.

Table 66. Register 32: Bit Definition

Bit	Bit Field Name	Default	Definition
0	DAC1[8]	1	Bit 8 of an 11-bit word to set the VVA for Channel 1.
1	DAC1[9]	1	Bit 9 of an 11-bit word to set the VVA for Channel 1.
2	DAC1[10]	1	Bit 10 of an 11-bit word to set the VVA for Channel 1.
3	Unused	0	Unused.
4	Unused	0	Unused.
5	Unused	0	Unused.
6	Unused	0	Unused.
7	Unused	0	Unused.

24.2.34. Register 33 (21h)

This register selects the RF and LO bands used for the device. Bits 2 to 7 are unused. The default is 0 = 0h = 0000_0000b.

Table 67. Register 33: Bit Definition

Bit	Bit Field Name	Default	Definition
0	LO_BAND	0	Set the LO band of operation. Set to logic LOW to select the 1.50GHz to 2.00GHz range for the LO band. This is the default. Set to logic HIGH to select the either the 0.45GHz to 1.50GHz range or the 2.00GHz to 2.80GHz range for the LO band.
1	RF_BAND	0	Set the RF band of operation. Set to logic LOW to select the 0.55GHz to 2.80GHz range for the RF band. This is the default. Set to logic HIGH to select the 0.45GHz to 0.55GHz range for the RF band.
2	Unused	0	Unused.
3	Unused	0	Unused.
4	Unused	0	Unused.
5	Unused	0	Unused.
6	Unused	0	Unused.
7	Unused	0	Unused.

24.2.35. Register 34 (22h)

This register selects the logic levels used for the digital output. Default is JEDEC 1.8 V logic and the default value is 0 = 00h = 0000_0000b. Bits 1 to 7 are unused.

Table 68. Register 34: Bit Definition

Bit	Bit Field Name	Default	Definition
0	Dig_Out_Level	0	Set for logic LOW for JEDEC 1.8 Volt logic (default). Set for logic HIGH for JEDEC 3.3 V logic.
1	Unused	0	Unused.
2	Unused	0	Unused.
3	Unused	0	Unused.
4	Unused	0	Unused.
5	Unused	0	Unused.
6	Unused	0	Unused.
7	Unused	0	Unused.

24.2.36. Register 35 (23h)

This register selects the precision of the Lock Detection and how the LO Lock Detection pin (56) is used. Bit 3, 6, and 7 are unused. The default is 0 = 0h = 0000_0000b.

Table 69. Register 35: Bit Definition

Bit	Bit Field Name	Default	Definition
0	LDP[0]	0	Bit 0 of a 3-bit word to set when the VCO precision lock detection is set (see Table 70).
1	LDP[1]	0	Bit 1 of a 3-bit word to set when the VCO precision lock detection is set (see Table 70).
2	LDP[2]	0	Bit 2 of a 3-bit word to set when the VCO precision lock detection is set (see Table 70).
3	Unused	0	Unused.
4	LDPinMode[0]	0	Bit 0 of a 2-bit word to set the LD pin operation (see Table 71).
5	LDPinMode[1]	0	Bit 1 of a 2-bit word to set the LD pin operation (see Table 71).
6	Unused	0	Unused.
7	Unused	0	Unused.

Table 70. 3-bit VCO Lock Precision Detection Description

Decimal	Bit 2	Bit 1	Bit 0	Definition
0	0	0	0	Set for lock detection to within 11.5ns (default).
1	0	0	1	Set for lock detection to within 6.5ns.
2	0	1	0	Set for lock detection to within 6.5ns.
3	0	1	1	Set for lock detection to within 3.0ns.
4	1	0	0	Set for lock detection to within 5.0ns.
5	1	0	1	Set for lock detection to within 5.0ns.
6	1	1	0	Set for lock detection to within 1.5ns.
7	1	1	1	Set for lock detection to within 1.5ns.

Table 71. 2-bit Lock Detection Pin Description

Decimal	Bit 1	Bit 0	Definition
0	0	0	Digital Lock (normal operation) (default).
1	0	1	VCO calibration is done.
2	1	0	Set for logic LOW.
3	1	1	Set for logic HIGH.

24.2.37. Register 36 (24h)

This register controls how the PLL locks the VCO frequency. The default value is 0 = 00h = 0000_0000b. Bits 3 to 7 are unused.

Table 72. Register 36: Bit Definition

Bit	Bit Field Name	Default	Definition
0	Force_Relock	0	0 = No VCO relocking (default). 1 = Force the VCO to recalibrate. This-bit is self-clearing.
1	Band_Sel_Disable	0	0 = If registers16-22 are written, then the VCO will recalibrate (default). 1 = No VCO recalibration is done.
2	Auto_Recal_Enable	0	0 = Disable Auto Recalibration (default). 1 = Enable Auto Recalibration.
3	Unused	0	Unused.
4	Unused	0	Unused.
5	Unused	0	Unused.
6	Unused	0	Unused.
7	Unused	0	Unused.

24.2.38. Register 37 (25h)

This register controls the lock detection of the PLL. The default value is 1 = 01h = 0000_0001b.

Note: LD Mode must be programmed to be logic HIGH for proper operation of the lock detection circuit. IDT requires the following digital word to be used 129 = 81h = 1000_0001b.

Table 73. Register 37: Bit Definition

Bit	Bit Field Name	Default	Definition
0	Vendor Supplied	1	Reserved for vendor use. Use only the default value.
1	Vendor Supplied	0	Reserved for vendor use. Use only the default value.
2	Vendor Supplied	0	Reserved for vendor use. Use only the default value.
3	Vendor Supplied	0	Reserved for vendor use. Use only the default value.
4	Vendor Supplied	0	Reserved for vendor use. Use only the default value.
5	Vendor Supplied	0	Reserved for vendor use. Use only the default value.
6	Vendor Supplied	0	Reserved for vendor use. Use only the default value.
7	LD Mode	0	Changes the lock timing loop. The default is logic LOW. *This pin is required to be programmed to logic HIGH.*

24.2.39. Register 38 (26h)

Register 39 and 38 select the VCO Band within the PLL. This is a 12-bit word that can vary from 1 to 4095. The default value is 256 = 100h = 0001_0000_0000b. Register 38 is the lower 8 bits of the word and the default value is 0 = 00h = 0000_0000b.

Table 74. Register 38: Bit Definition

Bit	Bit Field Name	Default	Definition
0	BndSelDiv[0]	0	Bit 0 of a 12-bit word to select the VCO Band.
1	BndSelDiv[1]	0	Bit 1 of a 12-bit word to select the VCO Band.
2	BndSelDiv[2]	0	Bit 2 of a 12-bit word to select the VCO Band.
3	BndSelDiv[3]	0	Bit 3 of a 12-bit word to select the VCO Band.
4	BndSelDiv[4]	0	Bit 4 of a 12-bit word to select the VCO Band.
5	BndSelDiv[5]	0	Bit 5 of a 12-bit word to select the VCO Band.
6	BndSelDiv[6]	0	Bit 6 of a 12-bit word to select the VCO Band.
7	BndSelDiv[7]	0	Bit 7 of a 12-bit word to select the VCO Band.

24.2.40. Register 39 (27h)

Register 39 and 38 select the VCO Band within the PLL. This is a 12-bit word that can vary from 1 to 4095. The default value is 256 = 100h = 0001_0000_0000b. Register 39 is the higher 4 bits of the word and the default value is 1 = 01h = 0000_0001b.

Table 75. Register 39: Bit Definition

Bit	Bit Field Name	Default	Definition
0	BndSelDiv[8]	1	Bit 8 of a 12-bit word to select the VCO Band.
1	BndSelDiv[9]	0	Bit 9 of a 12-bit word to select the VCO Band.
2	BndSelDiv[10]	0	Bit 10 of a 12-bit word to select the VCO Band.
3	BndSelDiv[11]	0	Bit 11 of a 12-bit word to select the VCO Band.
4	Unused	0	Unused.
5	Unused	0	Unused.
6	Unused	0	Unused.
7	Unused	0	Unused.

24.2.41. Register 40 (28h)

This register is reserved for internal use. The default value is 0 = 00h = 0000_0000b.

24.2.42. Register 41 (29h)

This register is reserved for internal use. The default value is 0 = 00h = 0000_0000b.

24.2.43. Register 42 (2Ah)

This register is reserved for internal use. The default value is 2 = 02h = 0000_0010b.

24.2.44. Register 43 (2Bh)

This register is reserved for internal use. The default value is 203 = CBh = 1100_1011b.

24.2.45. Register 44 (2Ch)

This register is reserved for internal use. The default value is 0 = 00h = 0000_0000b.

24.2.46. Register 45 (2Dh)

This register is reserved for internal use. The default value is 0 = 00h = 0000_0000b.

24.2.47. Register 46 (2Eh)

This register is reserved for internal use and is READ ONLY. The default value does not apply.

24.2.48. Register 47 (2Fh)

This register is reserved for internal use and is READ ONLY. The default value does not apply.

24.2.49. Register 48 (30h)

This register is reserved for internal use and is READ ONLY. The default value does not apply.

24.2.50. Register 49 (31h)

This register is reserved for internal use. The default value does not apply.

25. Evaluation Kit Picture

Figure 97. Top View – Differential Board

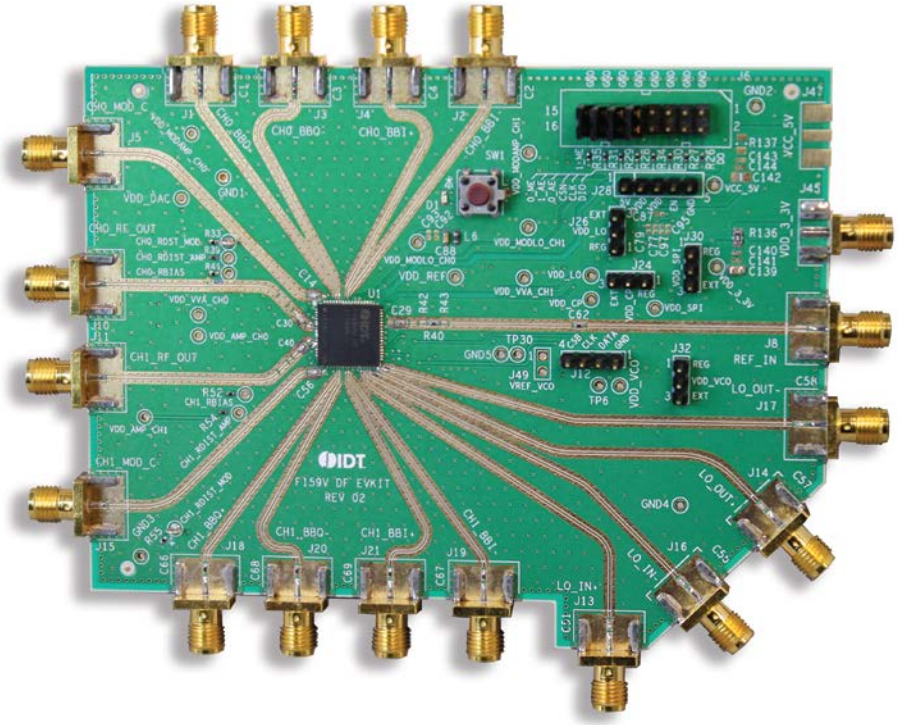
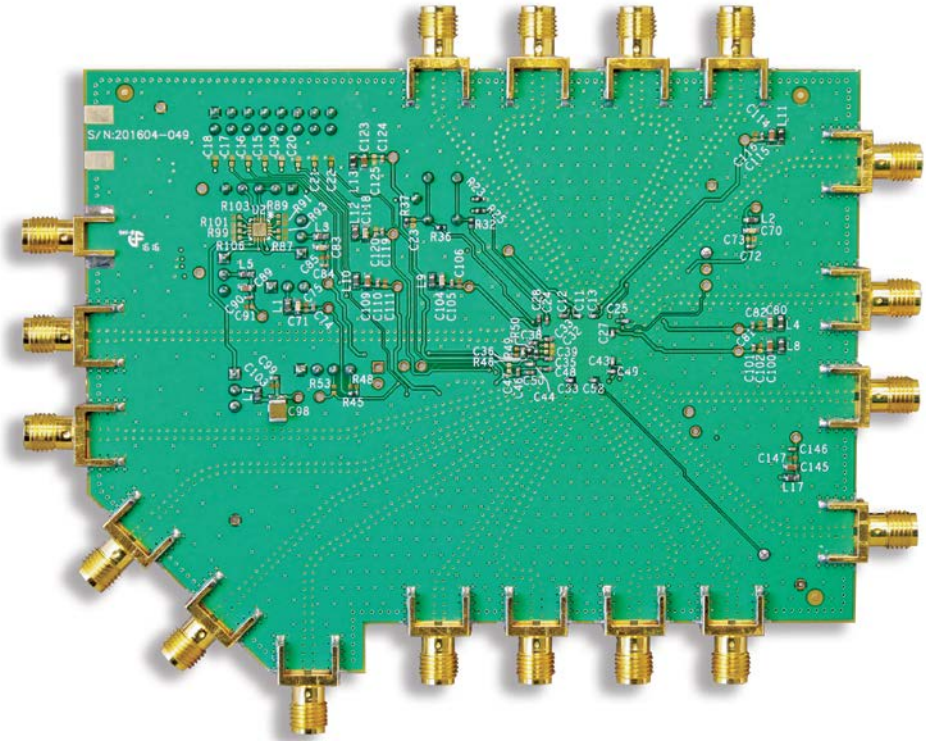


Figure 98. Bottom View – Differential Board



26. Evaluation Kit / Applications Circuit

Figure 99. Electrical Schematic for the Differential Evaluation Board

All differential ports have transmission lines of equal length.

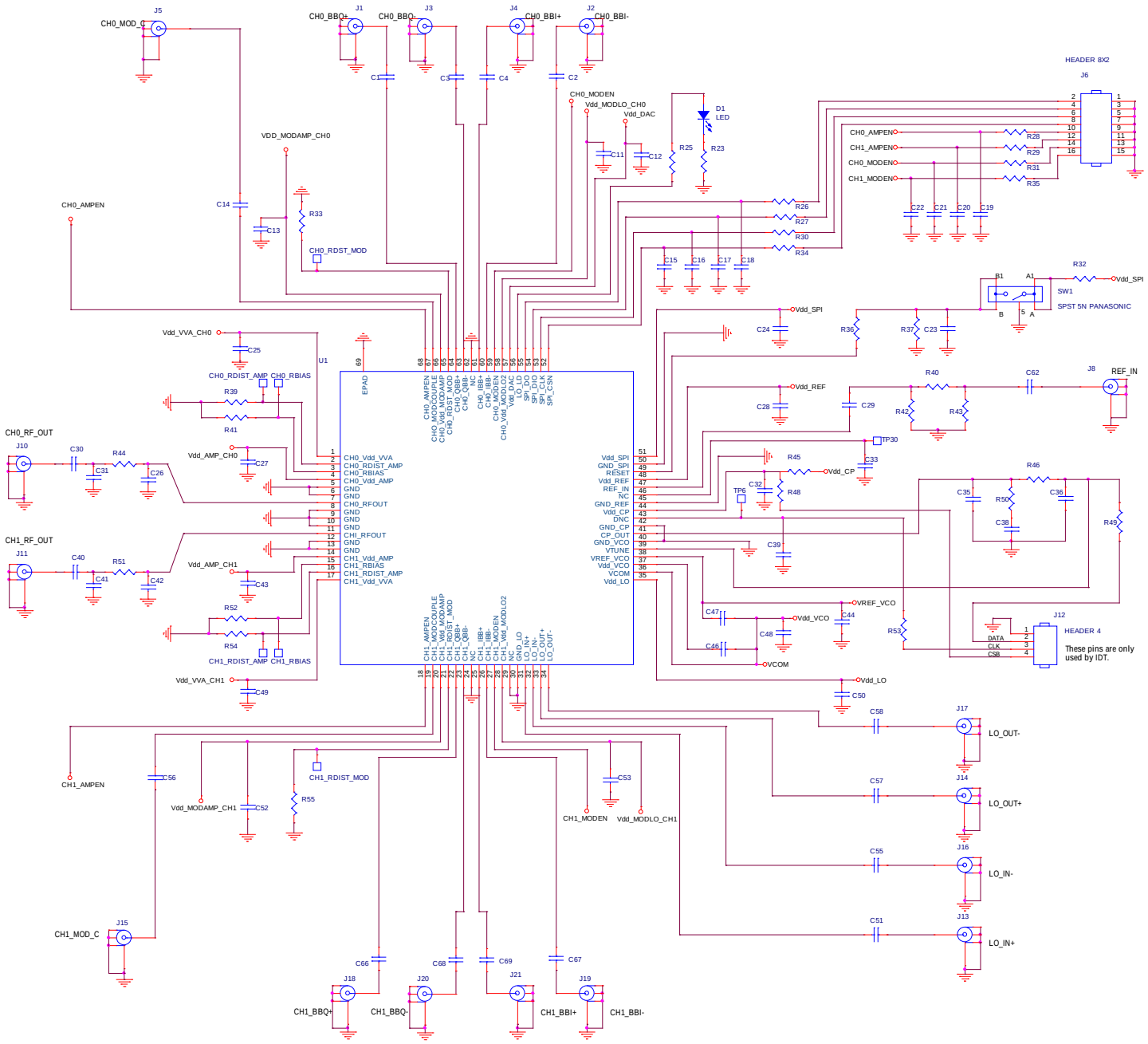


Figure 100. DC Electrical Schematic for the Differential Evaluation Board

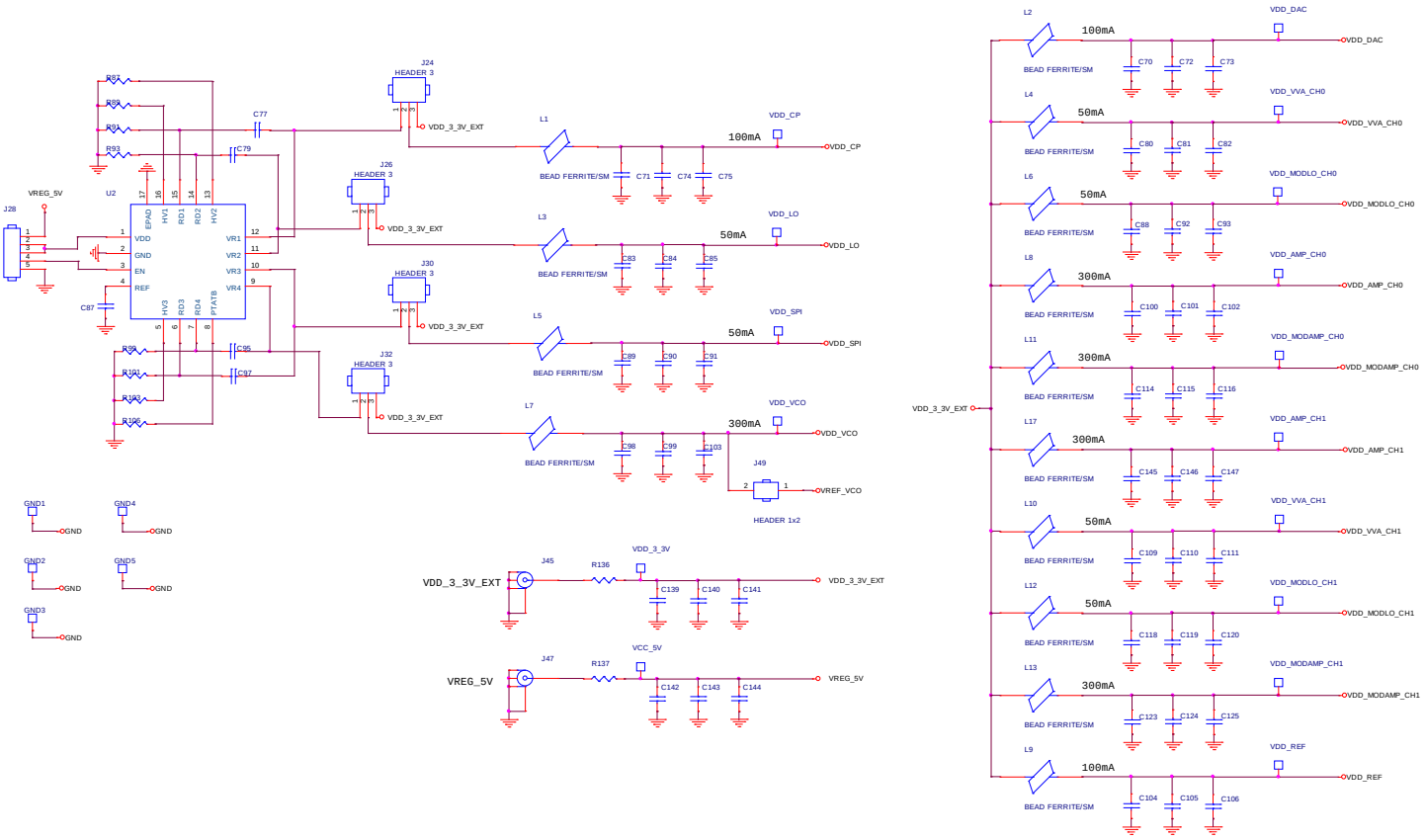


Table 76. Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C14, C30, C40, C51, C55, C56, C57, C58	8	100pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H101J	Murata
C11, C13, C25, C27, C43, C49, C52, C53	8	1000pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H102J	Murata
C72, C74, C81, C84, C90, C92, C99, C101, C105, C110, C115, C119, C124, C140, C146	15	10nF ±5%, 50V, X7R Ceramic Capacitor (0402)	GRM155R71H103J	Murata
C12, C24, C28, C29, C32, C48, C50	7	100nF ±10%, 16V, X7R Ceramic Capacitor (0402)	GRM155R71C104K	Murata
C70, C71, C80, C83, C88, C89, C100, C104, C109, C114, C118, C123, C145	13	10µF ±20%, 16V, X6S Ceramic Capacitor (0603)	GRM188C81C106M	Murata
C139	1	10µF ±10%, 16V, X6S Ceramic Capacitor (0805)	GRM21BC81C106K	Murata
C35	1	2700pF ±10%, 50V, X7R Ceramic Capacitor (0402)	GRM155R71H272K	Murata
C38	1	47nF ±10%, 50V, X7R Ceramic Capacitor (0402)	GRM155R71H473K	Murata
C36	1	680pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H681	Murata
C44	1	2.2µF ±10%, 10V, X5R Ceramic Capacitor (0402)	GRM155R61A225K	Murata
C46	1	33nF ±10%, 50V, X7R Ceramic Capacitor (0402)	GRM155R71H333K	Murata
C98	1	150µF ±20%, 6.3V, X5R Ceramic Capacitor (1210)	JMK325ABJ157M	Taiyo Yuden
R25, R36, R40, R45, C1, C2, C3, C4, C62, C66, C67, C68, C69	13	0Ω Resistor (0402)	ERJ-2GE0R00X	Panasonic
R136	1	0Ω Resistor (0805)	ERJ-6GEY0R00	Panasonic
R23	1	33Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF33R0X	Panasonic
R28, R29, R31, R32, R35	5	100Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1000X	Panasonic
R50	1	360Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF3600X	Panasonic
R39, R46, R54	3	1kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1001X	Panasonic
R26, R27, R30, R34, R33, R55, C15, C16, C17, C18	10	2kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF2001X	Panasonic
R41, R52	2	3.9kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF3901X	Panasonic
R37	1	5.11kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF5111X	Panasonic

Table 77. Bill of Material (BOM) (Cont.)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
L1- L13, L17	14	EMI Filter Beads Chips 220 Ohm 450mA (0603)	BLM18BB221SN1D	Murata
D1	1	LED GREEN CLEAR SMD (0603)	LTST-C191KGKT	LITE-ON
SW1	1	SWITCH TACTILE SPST-NO 0.02A 15V	EVQ-PBG05R	Panasonic
J24, J26, J30, J32	4	CONN HEADER VERT SGL 3 X 1 POS GOLD	961103-6404-AR	3M
J12	1	CONN HEADER VERT SGL 4 X 1 POS GOLD	961104-6404-AR	3M
J28	1	CONN HEADER VERT SGL 5 X 1 POS GOLD	961105-6404-AR	3M
J6	1	CONN HEADER VERT DBL 8 X 2 POS GOLD	67997-116HLF	FCI
J1, J2, J3, J4, J5, J8, J10, J11, J13, J14, J15, J16, J17,J18, J19, J20, J21	17	Edge Launch SMA (0.375 inch pitch ground, tab)	142-0701-851	Emerson Johnson
J45	1	Edge Launch SMA (0.250 inch pitch ground, round)	142-0711-821	Emerson Johnson
U1	1	RF Transmitter 2 Channels	F159VNLGN	IDT
	1	Printed Circuit Board	F159V EVKIT REV 02	IDT

Note: All other parts noted in the schematic that are not contained in this Bill of Material are not installed.

27. Application Information

The F159V is optimized for use in high-performance RF applications from 450MHz to 2800MHz.

27.1. Power Supplies

A common V_{DD} power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20µS. In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps or while it returns to zero. For multiple devices driven by a single control line, values will need to be adjusted so as to not load the control line.

27.2. Power Supply Sequencing

All power supply pins must be turned on simultaneously.

27.3. Digital Pin Voltage and Resistance Values

The following table provides open-circuit DC voltage referenced to ground and resistance values for each of the control pins listed.

Table 78. Digital Pin Voltages and Resistance

Pin	Name	DC Voltage (volts)	Pull-up or Pull-down Resistance Value (kΩ)
18	CH1_AMPEN	3.3	50
27	CH1_MODEN	3.3	50
49	RESET	0	51
52	SPI_CSN	0	51
53	SPI_CLK	0	51
54	SPI_DIO	1.8	51
59	CH0_MODEN	3.3	50
68	CH0_AMPEN	3.3	50

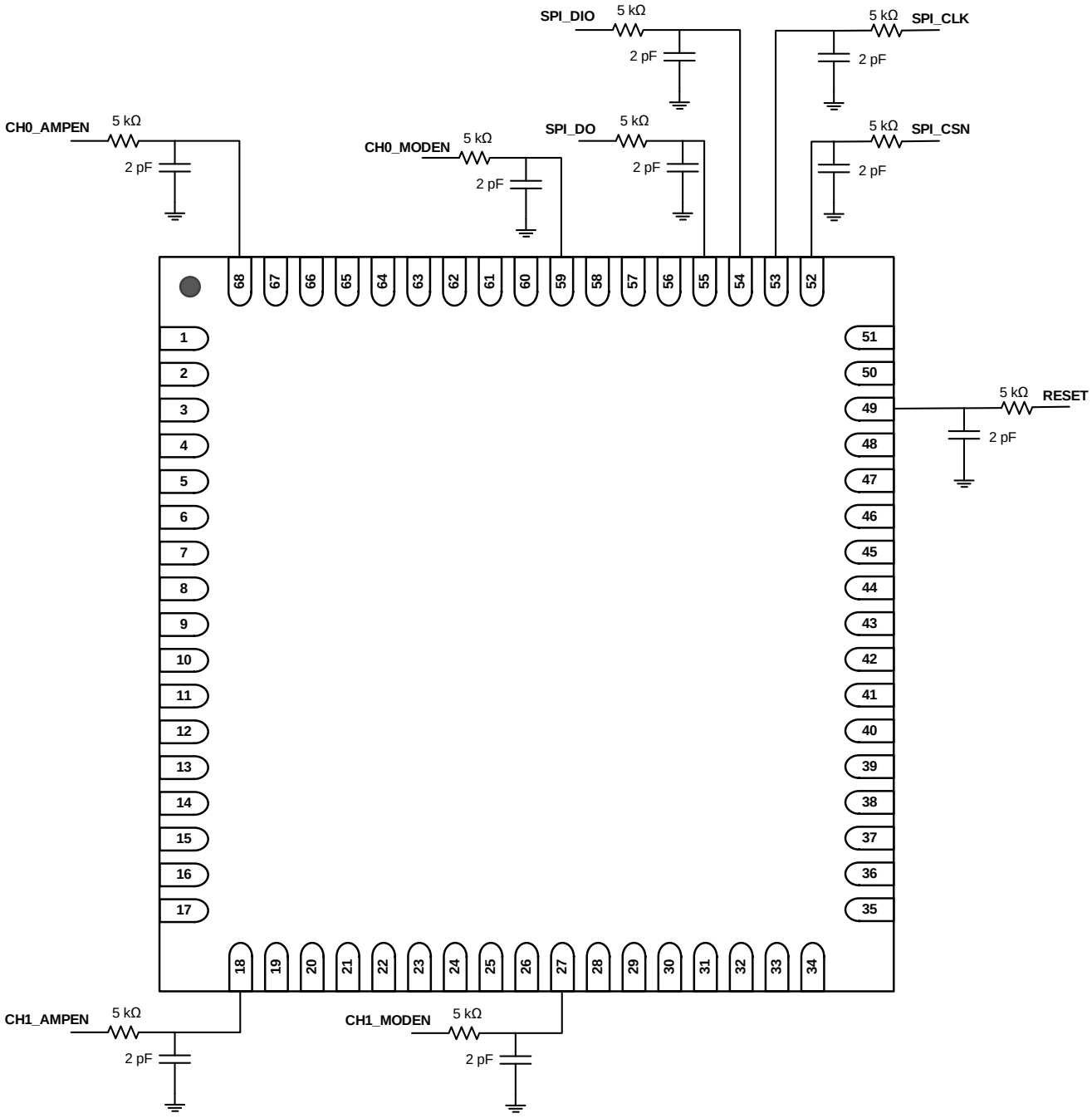
27.4. Phase Relation between the Quadrature Input Signals: I and Q

When BBI leads BBQ by 90 degrees, HS LO injection is used. When BBQ leads BBI by 90 degrees, LS LO injection is used.

27.5. Signal Integrity

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to all SPI and control pins as shown below. Note that the recommended resistor and capacitor values do not necessarily match the EVKit BOM for the case of poor control signal integrity.

Figure 101. Control Pin Interface



28. Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/us/en/document/psc/nlnlg68-package-outline-100-x-100-mm-epad-770-mm-sq-vfqfp-n

29. Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
F159VNLGN	10 x 10 x 0.9 mm 68-VFQFPN	3	Tray	-20° to +115°C
F159VNLGN8	10 x 10 x 0.9 mm 68-VFQFPN	3	Reel	-20° to +115°C
F159VEVBN	Evaluation Board			

30. Marking Diagram

- Line 1 and 2 are the part number.
- Line 3 “ZK” is for die version.
- Line 3 “yyww” = 1729 has two digits for the year and week that the part was assembled.
- Line 3 “L” denotes assembly site.
- Line 4 “Q57BO12PY THA” is the assembly lot number.

Revision History

Revision Date	Description of Change
May 15, 2020	Rebranded/reformatted document.
November 10, 2017	Updated for format, theory of operation, and register definition.
December 23, 2016	Initial release.

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