MAX20459

Automotive High-Current Step-Down Converter with USB-C Dedicated Charging Port

General Description

The MAX20459 combines a 3A high-efficiency, automotive-grade, step-down converter, a USB Type-C DFP controller, and automatic BC1.2 DCP, Apple®, and Samsung® dedicated charger-detection circuitry. The device also includes a USB load current-sense amplifier and configurable feedback-adjustment circuit designed to provide automatic USB voltage compensation. The device limits the USB load current using both a fixed internal peak-current threshold and a user-configurable external current-sense USB load threshold.

The MAX20459 is optimized for high-frequency operation and includes programmable frequency selection from 310kHz to 2.2MHz, allowing optimization of efficiency, noise, and board space based on application requirements. The fully synchronous DC-DC converter integrates high-side and low-side MOSFETs along with an external SYNC input/output, and can be configured for spread-spectrum operation. Additionally, thermal foldback is implemented to avoid excessive heating of the module while charging at high ambient temperature.

The MAX20459 allows flexible configuration and advanced diagnostic options for both standalone and supervised applications. The device can operate as a true one-chip solution that offers advanced fault autorecovery and can be programmed using external programming resistors and/or internal I^2C registers.

The MAX20459 is available in a small 5mm x 5mm 32-pin TQFN package and is designed to minimize required external components and layout area.

Applications

- Dedicated USB Charging Port (DCP)
  - Host and Hub Module Dedicated Charging Ports
  - Dedicated Charging Modules

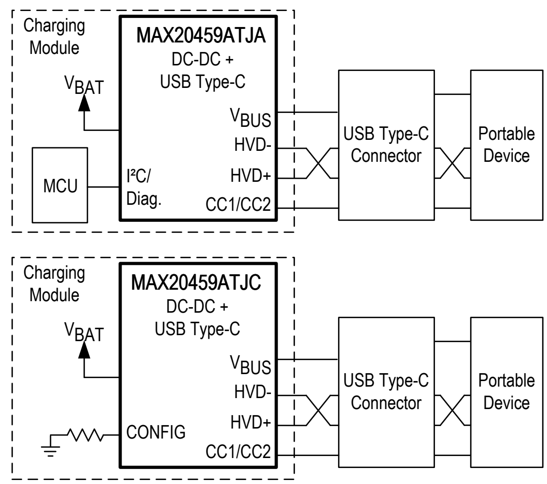
Benefits and Features

- One-Chip Type-C Solution Directly from Car Battery to Portable Device
  - USB Type-C-Compliant DFP Controller
  - Integrated iPhone®/iPad®, Samsung® and BC1.2 DCP Charger Detection
  - 4.5V to 28V Input (40V Load Dump), Synchronous Buck Converter
  - 5V to 7V, 3A Output Capability
  - Standalone Device or I^2C Configuration Options and Fault Autorecovery
- Optimal USB Charging and Communication for Portable Devices
  - User-Programmable Voltage Gain Adjusts Output for up to 474mΩ Cable Resistance
  - User-Programmable USB Current Limit
- Low-Noise Features Prevent Interference with AM Band and Portable Devices
  - Fixed-Frequency 310kHz to 2.2MHz Operation
  - Fixed-PWM Option at No Load
  - Spread Spectrum for EMI Reduction
  - SYNC Input/Output for Frequency Parking
- Robust Design Keeps Vehicle System and Portable Device Safe in an Automotive Environment
  - Short-to-Battery Protection on V_{BUS}, HVD± Pins
  - ±15kV Air/±8kV Contact ISO 10605 (330pF, 330Ω)*
  - ±15kV Air/±8kV Contact ISO 10605 (330pF, 2kΩ)*
  - ±15kV Air/±8kV Contact IEC 61000-4-2 (150pF, 330Ω)*
  - Overtemperature Protection, Warning, and Intelligent Current Foldback
  - AEC-Q100 Qualified
  - -40ºC to +125ºC Operating Temperature Range

Tested in Typical Application Circuit as used on the MAX20459 Evaluation Kit

Ordering Information appears at end of datasheet.

Simplified Block Diagram



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Absolute Maximum Ratings

SUPSW to PGND .... -0.3V to +40V
HVEN to PGND .... -0.3V to V_{SUPSW} + 0.3V
LX to PGND (Note 1)............................ -0.3V to V_{SUPSW} + 0.3V
BIAS to AGND .... -0.3V to +6V
SYNC to AGND ....-0.3V to V_{BIAS} + 0.3V
SENSN, SENSP, VBMON to AGND .... -0.3V to V_{SUPSW} + 0.3V
AGND to PGND... -0.3V to +0.3V
BST to PGND .... -0.3V to +46V
BST to LX .... -0.3V to +6V
IN, CONFIG1, ENBUCK, SDA (CONFIG2), SCL (CONFIG3), BIAS, DCP_MODE, FAULT, INT(ATTACH), SHIELD, CC1, CC2 to AGND .... -0.3V to +6V
HVDP, HVDM to AGND.. -0.3V to +18V
G_DMOS to AGND... -0.3V to +16V

LX Continuous RMS Current 3.5A
Output Short-Circuit Duration....................................Continuous
Thermal Characteristics
Continuous Power Dissipation, Single-Layer Board (T_A = +70°C, 32-TQFN (derate 21.3mW/°C above +70°C)).... mW to 1702.10mW
Continuous Power Dissipation, Multilayer Board (T_A = +70°C, 32-TQFN (derate 34.5mW/°C above +70°C)) ....2758.6 mW
Operating Temperature Range ....-40°C to 125°C
Junction Temperature ....+150°C
Storage Temperature Range..........................-40°C to +150°C
Lead Temperature (soldering, 10s) ....300°C
Soldering Temperature (reflow)...................................+260°C

Note 1: Self-protected from transient voltages exceeding these limits for ≤ 50ns in circuit under normal operation.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

32 Pin TQFN 5x5x0.75mm

Package Code	T3255+4C
Outline Number	21-0140
Land Pattern Number	90-0012
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	47 °C/W
Junction to Case (θ_{JC})	1.70 °C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	29 °C/W
Junction to Case (θ_{JC})	1.70 °C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{SUPSW} = 14V, V_{IN} = 3.3V, V_{ENBUCK} = 3.3V, Temperature = $T_A = T_J$ = -40°C to +125°C, unless otherwise noted, actual typical values may vary and are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply and Enable						
Supply Voltage Range	V_{SUPSW}	(*Note 2*)	4.5		28	V
Load Dump Event Supply Voltage Range	V_{SUPSW_LD}	< 1s			40	V
Supply Current - Off State	I_{SUPSW}	V_{SUPSW} = 18V; V_{HVEN} = 0V; V_{ENBUCK} = 0V; V_{IN} = 0V; off state		10	20	µA

Electrical Characteristics (continued)

(V_{SUPSW} = 14V, V_{IN} = 3.3V, V_{ENBUCK} = 3.3V, Temperature = $T_A = T_J$ = -40°C to +125°C, unless otherwise noted, actual typical values may vary and are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current - Buck Off	I_{SUPSW}	V_{HVEN} = 14V; V_{ENBUCK} = 0V		1.1		mA
Supply Current - Skip Mode	I_{SUPSW}	V_{HVEN} = 14V; buck switching; no load		1.8		mA
Supply Current - FPWM	I_{SUPSW}	V_{HVEN} = 14V; buck switching; no load		28		mA
BIAS Voltage	V_{BIAS}	5.75V ≤ V_{SUPSW} ≤ 28V	4.5	4.7	5.25	V
BIAS Current Limit			50	150		mA
BIAS Undervoltage Lockout	V_{UV_BIAS}	V_{BIAS} rising	3.0	3.3	3.6	V
BIAS Undervoltage Lockout Hysteresis				0.2		V
SUPSW Undervoltage Lockout		V_{SUPSW} rising	3.9		4.42	V
SUPSW Undervoltage Lockout Hysteresis				0.2		V
IN Voltage Range	V_{IN}		3		3.6	V
IN Overvoltage Lockout	V_{IN_OVLO}	V_{IN} rising	3.8	4	4.3	V
IN Input Current	I_{IN}				10	µA
HVEN Rising Threshold	V_{HVEN_R}		0.6	1.5	2.4	V
HVEN Falling Threshold	V_{HVEN_F}				0.4	V
HVEN Hysteresis	V_{HVEN}			0.2		V
HVEN Delay Rising	t_{HVEN_R}		2.5		15	µs
HVEN Delay Falling	t_{HVEN_F}		5	12	25	µs
HVEN Input Leakage		V_{HVEN} = V_{SUPSW} = 18V, V_{HVEN} = 0V			10	µA
G_DMOS Pin						
G_DMOS Unloaded Output Voltage	$V_{G\_DMOS\_OC}$	V_{G_DMOS} to V_{BIAS}, internal discharge path 2MΩ to GND	7	10	13.0	V
G_DMOS Output Impedance	$R_{G\_DMOS\_OC}$			100	250	kΩ
G_DMOS DC Output Current	$I_{G\_DMOS\_SC}$	G_DMOS to BIAS		20		µA
USB Type C / Current Level Characteristics						
CC DFP Default Current Source	$I_{DFP0.5\_CC}$	4.0V < V_{BIAS} < 5.5V, ±20%	64	80	96	µA
CC DFP 1.5A Current Source	$I_{DFP1.5\_CC}$	4.0V < V_{BIAS} < 5.5V, ±8%	166	180	194	µA
CC DFP 3.0A Current Source	$I_{DFP3.0\_CC}$	4.0V < V_{BIAS} < 5.5V, ±8%	304	330	356	µA
USB Type C / Timing Characteristics						
Type-C CC Pin Detection Debounce	$t_{CCDEBOUNCE}$	Final transition to Attached state		160		ms

Electrical Characteristics (continued)

(V_{SUPSW} = 14V, V_{IN} = 3.3V, V_{ENBUCK} = 3.3V, Temperature = $T_A = T_J$ = -40°C to +125°C, unless otherwise noted, actual typical values may vary and are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HVD+, HVD- Pins						
Protection Trip Threshold	V_{OV_D}		3.65	3.85	4.1	V
On-Resistance of HVD+/HVD- short	R_{SHORT}	V_{HVDP} = 1V, I_{HVDM} = 500µA		90	180	Ω
HVD+/HVD- On-Leakage Current	I_{HVD_ON}	$V_{HVD\pm}$ = 3.6V or 0V	-7		7	µA
HVD+/HVD- Off-Leakage Current	I_{HVD_OFF}	V_{HVD+} = 18V or V_{HVD-} = 18V, $V_{D\pm}$ = 0V			150	µA
Current-Sense Amplifier (SENSP, SENSN) and Analog Inputs (VBMON)						
Gain		10mV < V_{SENSP} - V_{SENSN} < 110mV, GAIN[4:0] = 0b11111		19.4		V/V
Cable Compensation LSB	R_{LSB}			18		mΩ
Overcurrent Threshold	ILIM_SET	ILIM[2:0] = 0b111, R_{SENSE} = 33mΩ	3.04	3.14	3.30	A
		ILIM[2:0] = 0b110, R_{SENSE} = 33mΩ	2.6	2.75	2.9	
		ILIM[2:0] = 0b101, R_{SENSE} = 33mΩ	2.1	2.25	2.4	
		ILIM[2:0] = 0b100, R_{SENSE} = 33mΩ	1.62	1.7	1.78	
		ILIM[2:0] = 0b011, R_{SENSE} = 33mΩ	1.05	1.13	1.21	
		ILIM[2:0] = 0b010, R_{SENSE} = 33mΩ	0.8	0.86	0.92	
		ILIM[2:0] = 0b001, R_{SENSE} = 33mΩ	0.55	0.6	0.65	
		ILIM[2:0] = 0b000, R_{SENSE} = 33mΩ	0.3	0.33	0.36	
SENSN / VBMON Discharge Current	I_{SENSN_DIS}		11	18	32	mA
Startup Wait Time	t_{BUCK_WAIT}			100		ms
SENSN / VBMON Discharge Time	t_{DIS_POR}	Discharge after POR		1		s
	t_{DIS_CD}	DCDC_ON toggle		2		
	t_{DIS_DET}	Type-C detach		100		ms
Forced Buck Off-Time	$t_{BUCKOFF\_CD}$	DCDC_ON toggle; see reset criteria		2		s
	$t_{BUCKOFF\_DET}$	Type-C detach		100		ms
Attach Comparator Load Current Rising Threshold		Common mode input = 5.15V	5	16	28	mA
Attach Comparator Hysteresis		Common mode input = 5.15V		2.5		mA
SENSN Undervoltage Threshold (Falling)	V_{UV_SENSN}		4	4.375	4.75	V
SENSN Overvoltage Threshold (Rising)	V_{OV_SENSN}		7	7.46	7.9	V

Electrical Characteristics (continued)

(V_{SUPSW} = 14V, V_{IN} = 3.3V, V_{ENBUCK} = 3.3V, Temperature = $T_A = T_J$ = -40°C to +125°C, unless otherwise noted, actual typical values may vary and are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SENSN Short-Circuit Threshold (Falling)	V_{SHT_SENSN}		1.75	2	2.25	V
SENSN Undervoltage Fault Blanking Time				16		ms
SENSN Overvoltage Fault Blanking Time	t_{B,OV_SENSN}	From overvoltage condition to $\overline{\text{FAULT}}$ asserted		3	6	µs
SENSN Discharge Threshold Falling		V_{SENSN} Falling	0.47	0.51	0.57	V
Remote Feedback Adjustment						
SHIELD Input Voltage Range			0.1		0.75	V
Gain			1.935	2	2.065	V/V
Input-Referred Offset Voltage				±2.0		mV
Digital Inputs (SDA, SCL, ENBUCK, DCP_MODE)						
Input Leakage Current		V_{PIN} = 5.5V, 0V	-5		+5	µA
Logic-High	V_{IH}		1.6			V
Logic-Low	V_{IL}				0.5	V
Synchronous Step-Down DC-DC Converter						
PWM Output Voltage	V_{SENSP}	7V ≤ V_{SUPSW} ≤ 28V, no load		5.15		V
Skip Mode Output Voltage	V_{SENSP_SKIP}	7V ≤ V_{SUPSW} ≤ 18V, no load (Note 2)		5.25		V
Load Regulation	R_{LR}	7V ≤ V_{SUPSW} ≤ 18V, for 5V nominal output setting		51		mΩ
Output Voltage Accuracy		8V ≤ V_{SUPSW} ≤ 18V, 2.4A, V_{SENSP} - V_{SENSN} = 79.2mV , GAIN[4:0] = 0b11111 cable compensation.	6.33		6.68	V
Spread-Spectrum Range		SS Enabled		±3.4		%
SYNC Switching Threshold High	V_{SYNC_HI}	Rising	1.4			V
SYNC Switching Threshold Low	V_{SYNC_LO}	Falling			0.4	V
SYNC Internal Pulldown				200		kΩ
SYNC Input Clock Acquisition time	t_{SYNC}	(Note 3)		1		Cycles
High-Side Switch On-Resistance	R_{ONH}	I_{LX} = 1A		54	95	mΩ
Low-Side Switch On-Resistance	R_{ONL}	I_{LX} = 1A		72	135	mΩ
BST Input Current	I_{BST}	$V_{BST} – V_{LX}$ = 5V, high-side on		2.2		mA

Electrical Characteristics (continued)

(V_{SUPSW} = 14V, V_{IN} = 3.3V, V_{ENBUCK} = 3.3V, Temperature = $T_A = T_J$ = -40°C to +125°C, unless otherwise noted, actual typical values may vary and are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LX Current-Limit Threshold				5		A
Skip Mode Peak-Current Threshold	I_{SKIP_TH}			1		A
Negative Current Limit				1.2		A
Soft-Start Ramp Time	t_{SS}			8		ms
LX Rise Time	t_{LXR}	(*Note 3*)		3		ns
LX Fall Time	t_{LXF}	(*Note 3*)		4		ns
BST Refresh Algorithm Low-Side Minimum On-Time				60		ns
$\overline{\text{FAULT}}$, $\overline{\text{INT}}$ ($\overline{\text{ATTACH}}$), SYNC Outputs						
Output-High Leakage Current		$\overline{\text{FAULT}}$, $\overline{\text{INT}}$($\overline{\text{ATTACH}}$) = 5.5V	-10		+10	µA
Output Low Level		Sinking 1mA			0.4	V
SYNC Output High Level		Sourcing 1mA, SYNC configured as output	V_{BIAS} -0.4			V
Configuration Resistors Converter						
CONFIG1-3 Current Leakage		V_{CONFIG} = 0V to 4V			±5	µA
Minimum Window Amplitude			-4		4	%
ADC						
Resolution				8		Bits
ADC Gain Error				±2		LSBs
Offset Error	Offset_ADC			±1		LSB
Oscillators						
Internal High Frequency Oscillator	HFOSC		7	8	9	MHz
Buck Oscillator Frequency	f_{SW}	FSW[2:0] = 0b000	1.95	2.2	2.45	MHz
Buck Oscillator Frequency	f_{SW}	FSW[2:0] = 0b101	340	410	480	KHz
Thermal Overload						
Thermal Warning Temperature				130		°C
Thermal Warning Hysteresis				10		°C
Thermal Shutdown Temperature				165		°C

Electrical Characteristics (continued)

(V_{SUPSW} = 14V, V_{IN} = 3.3V, V_{ENBUCK} = 3.3V, Temperature = $T_A = T_J$ = -40°C to +125°C, unless otherwise noted, actual typical values may vary and are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Shutdown Hysteresis				10		°C
I²C						
Serial-Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
START Condition Setup Time	$t_{SU:STA}$		0.6			µs
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
STOP Condition Hold Time	$t_{SU:STO}$		0.6			µs
Clock-Low Period	t_{LOW}		1.3			µs
Clock-High Period	t_{HIGH}		0.6			µs
Data-Setup Time	$t_{SU:DAT}$		100			ns
Data-Hold Time	$t_{HD:DAT}$	From 50% SCL falling to SDA change	0.3		0.6	µs
Pulse Width of Spike Suppressed	t_{SP}			50		ns
ESD Protection (All Pins)						
ESD Protection Level	V_{ESD}	Human Body Model		±2		kV
ESD Protection (HVDP, HVDM, CC1, CC2)						
ESD Protection Level	V_{ESD}	ISO 10605 Air Gap (330pF, 330Ω)		±15		kV
		ISO 10605 Air Gap (330pF, 2kΩ)		±15		
		ISO 10605 Contact (330pF, 330Ω)		±8		
		ISO 10605 Contact (330pF, 2kΩ)		±8		
		IEC 61000-4-2 Air Gap (150pF, 330Ω)		±15		
		IEC 61000-4-2 Contact (150pF, 330Ω)		±8		

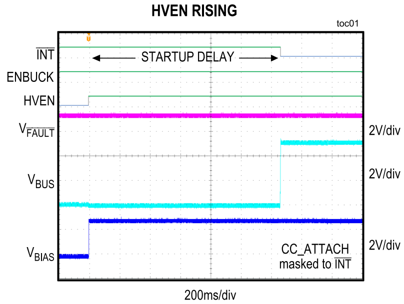
Note 2: Device is designed for use in applications with continuous operation of 14V. Device meets electrical table up to maximum supply voltage.

Note 3: Guaranteed by design and bench characterization; not production tested.

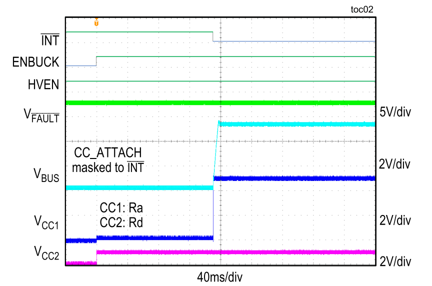
Typical Operating Characteristics

(TA = +25°C, unless otherwise noted.)

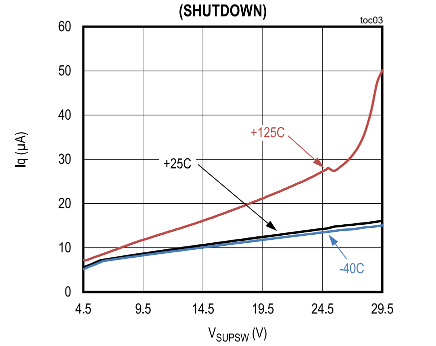
STARTUP INTO ATTACHMENT
HVEN RISING



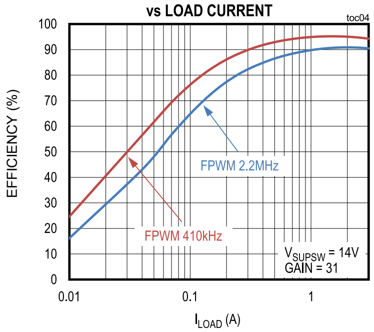
STARTUP INTO ATTACHMENT
ENBUCK RISING



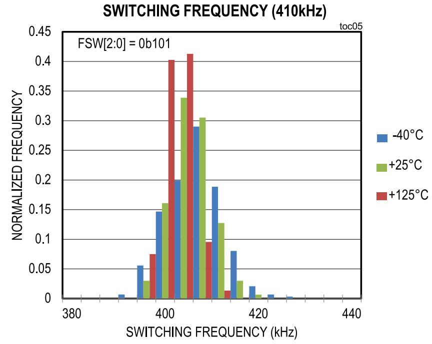
SUPPLY CURRENT vs VOLTAGE
(SHUTDOWN)



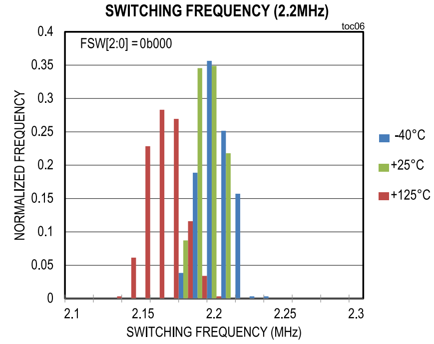
BUCK EFFICIENCY
vs LOAD CURRENT



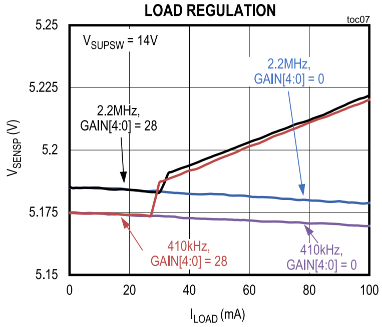
SWITCHING FREQUENCY (410kHz)



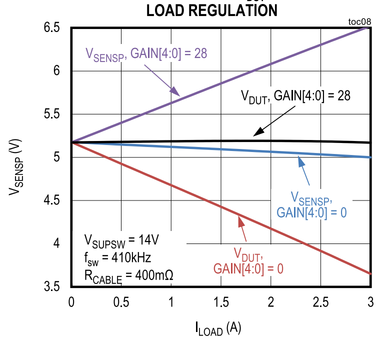
SWITCHING FREQUENCY (2.2MHz)



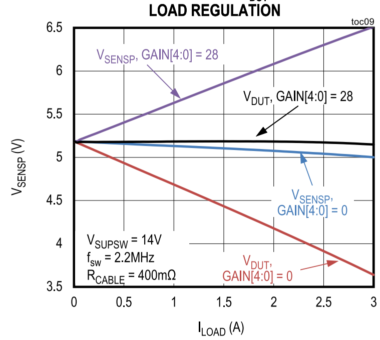
SENSP
LOAD REGULATION



SENSP AND V_{DUT}
LOAD REGULATION

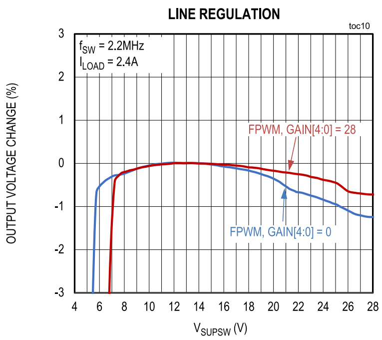


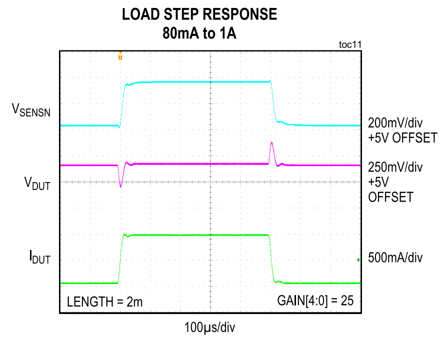
SENSP AND V_{DUT}
LOAD REGULATION

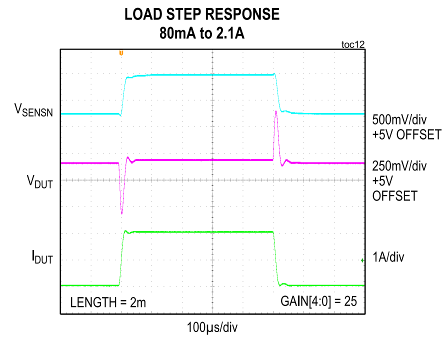


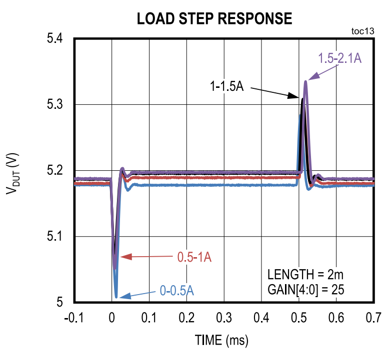
Typical Operating Characteristics (continued)

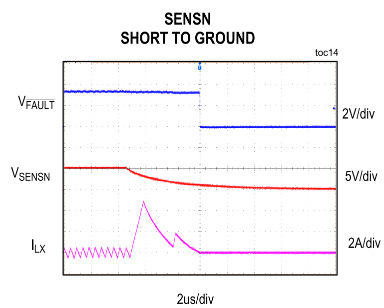
(T_A = +25°C, unless otherwise noted.)

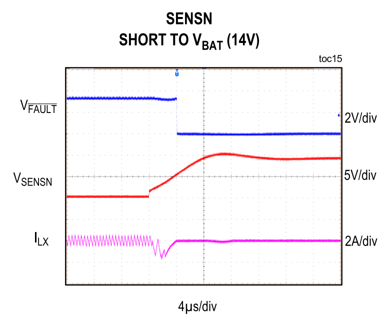


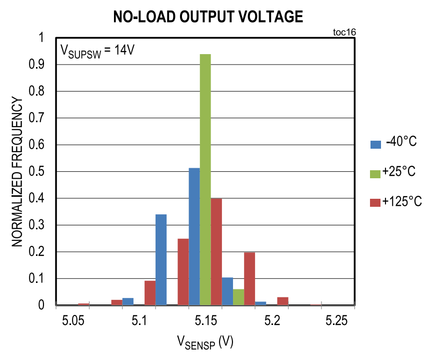


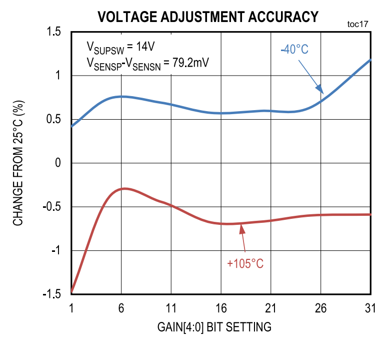


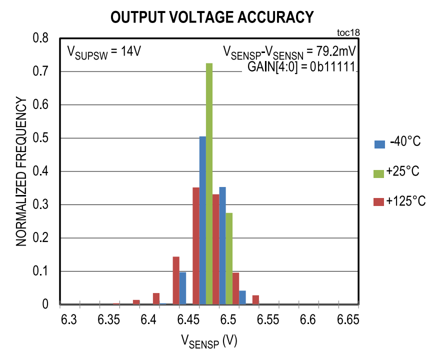








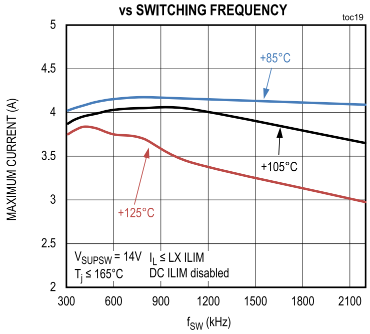




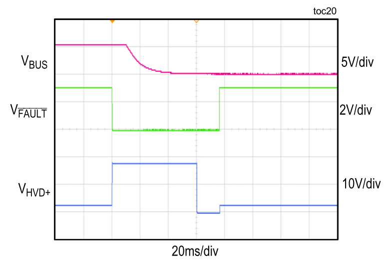
Typical Operating Characteristics (continued)

(TA = +25°C, unless otherwise noted.)

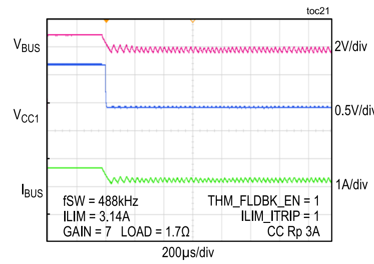
MAXIMUM USB LOAD CURRENT vs SWITCHING FREQUENCY



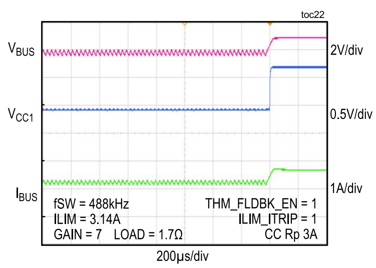
HVD+/- SHORT TO V_{BAT} (18V) POWERED AND ENABLED



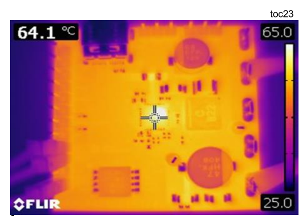
THERMAL FOLDBACK ENTRY



THERMAL FOLDBACK EXIT



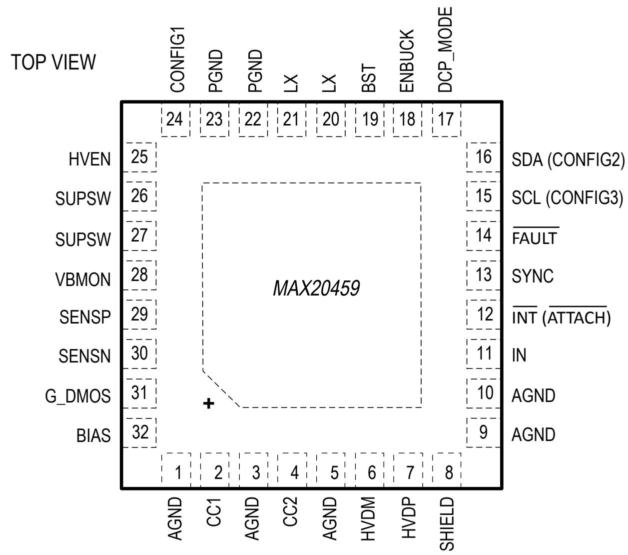
THERMAL IMAGE



f_{SW} = 488kHz, V_{IN} = 14V, I_{OUT} = 3.0A
4-layer PCB, 40 x 40mm, TA = +25° C

Pin Configuration

MAX20459



TQFN
5mm x 5mm

Pin Description

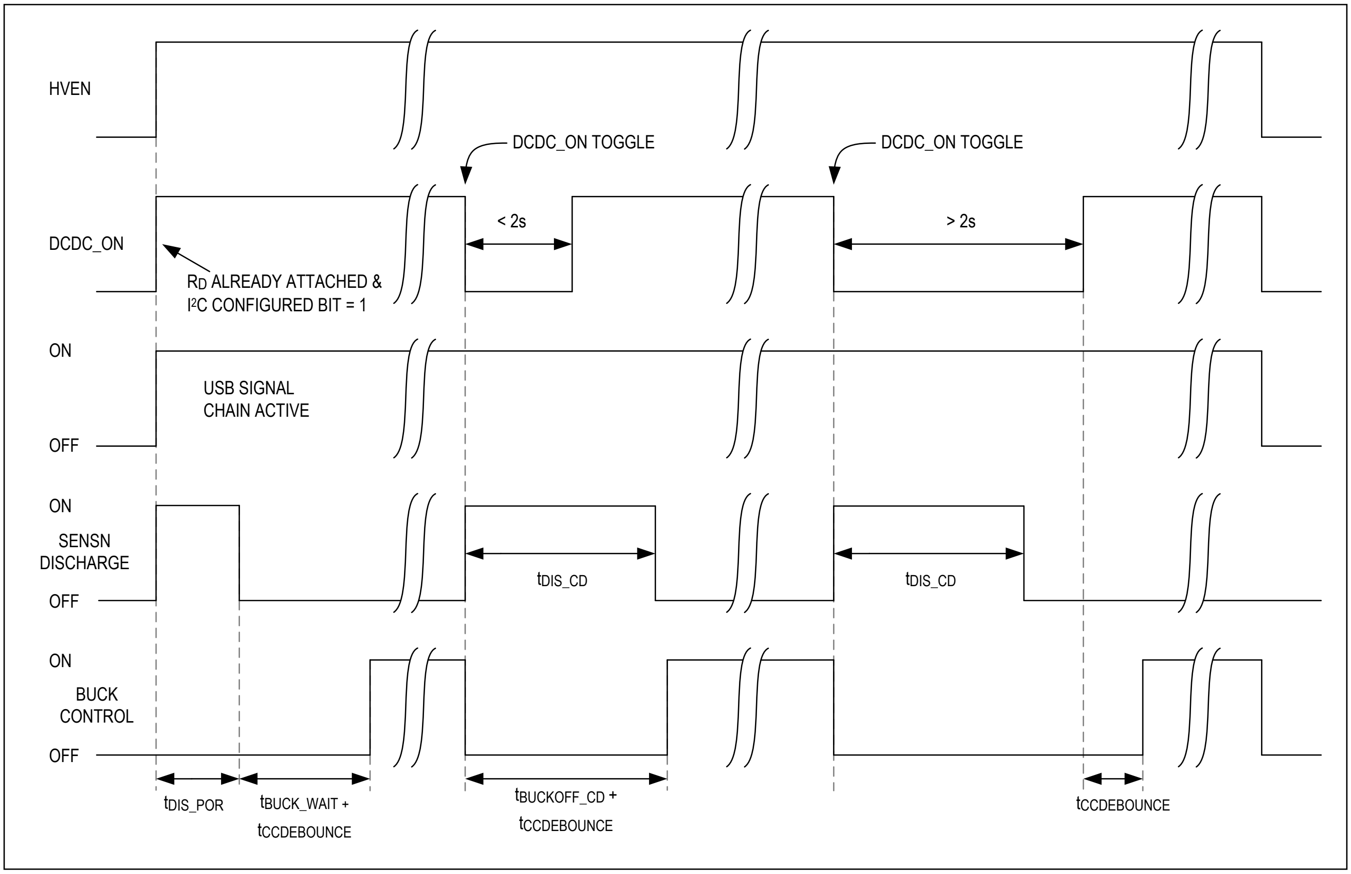
PIN	NAME	FUNCTION
1, 3, 5, 9, 10	AGND	Analog Ground.
2	CC1	Type-C Configuration Channel (CC).
4	CC2	Type-C Configuration Channel (CC).
6	HVDM	High-Voltage-Protected USB D- Interface. Connect HVD- to the downstream USB connector D- pin for charge detection.
7	HVDP	High-Voltage-Protected USB D+ Interface. Connect HVD+ to the downstream USB connector D+ pin for charge detection.
8	SHIELD	Optional Remote-Feedback Input. Tie to AGND if not used.
11	IN	Logic Enable Input. Connect to 3.3V. If no 3.3V rail is available in the system, use a 1kΩ/2kΩ resistor-divider from BIAS to generate 3.3V on IN. See *Typical Application Circuits*. IN is also used for clamping during overvoltage events on HVD+ or HVD-. Connect a 1µF ceramic capacitor from IN to GND.

Pin Description (continued)

PIN	NAME	FUNCTION
12	$\overline{\text{INT}}$ ($\overline{\text{ATTACH}}$)	Interrupt/Attach. On the I²C variant, functions as an active-low interrupt pin. On the standalone variant, functions as an active-low attach indicator. Connect a 100kΩ pullup resistor to IN. Tie to AGND if not used.
13	SYNC	Switching Frequency Input/Output for Synchronization with Other Supplies. Configure Sync as an input and tie to AGND if not used. See Applications Information section.
14	$\overline{\text{FAULT}}$	Active-Low, Open-Drain, Fault Indicator Output. Connect a 100kΩ pullup resistor to IN. Tie to AGND if not used.
15	SCL (CONFIG3)	SCL/Configuration 3. For the I²C variant, this serves as the SCL pin. For the standalone variant, this serves as CONFIG3 pin. Connect a resistor to AGND to configure thermal foldback, gain, current limit, and USB type-C source current.
16	SDA (CONFIG2)	SDA/Configuration 2. For the I²C variant, this serves as the SDA pin. For the standalone variant, this serves as the CONFIG2 pin. Connect a resistor to AGND to configure cable compensation.
17	DCP_MODE	DCP Mode Select. Tie low for Apple 2.4A mode, tie high for Apple 1A mode.
18	ENBUCK	DC-DC Enable Input. Drive high/low to enable/disable the buck converter. Connect to BIAS for always-on operation.
19	BST	High-Side Driver Supply. Connect a 0.1µF capacitor from BST to LX.
20, 21	LX	Inductor Connection Pin. Connect an inductor from LX to the DC-DC converter output (SENSP).
22, 23	PGND	Power Ground.
24	CONFIG1	Configuration 1. Connect a resistor to AGND to configure spread spectrum, sync direction, and switching frequency (standalone) or I^2C address.
25	HVEN	Active-High System Enable Pin. HVEN is battery-voltage tolerant. Connect to SUPSW for always-on operation.
26, 27	SUPSW	Internal High-Side Switch Supply Input. SUPSW provides power to the internal buck converter and LDO. Connect a 100nF and 10µF ceramic capacitor in parallel with a 47µF electrolytic capacitor from SUPSW to PGND. See *DC-DC Input Capacitor Selection*.
28	VBMON	USB V_{BUS} Monitor Pin
29	SENSP	DC-DC Converter Feedback Input and Current-Sense Amplifier Positive Input. Place the DC-DC bulk capacitance on this net. Connect to the positive terminal of the current-sense resistor and the main output of the converter. Used for internal voltage regulation loop.
30	SENSN	Current-Sense Amplifier Negative Input. Connect to the negative terminal of the current-sense resistor.
31	G_DMOS	Gate-Drive Output. Optionally connect to the gate of an external n-channel FET. Otherwise, terminate with a 2.7MΩ resistor or a 10pF capacitor to AGND.
32	BIAS	5V Linear-Regulator Output. Connect a 2.2µF ceramic capacitor from BIAS to GND. BIAS powers the internal circuitry.
EP	EP	Exposed Pad. Connect EP to multiple GND planes with 3 x 3 via grid (minimum).

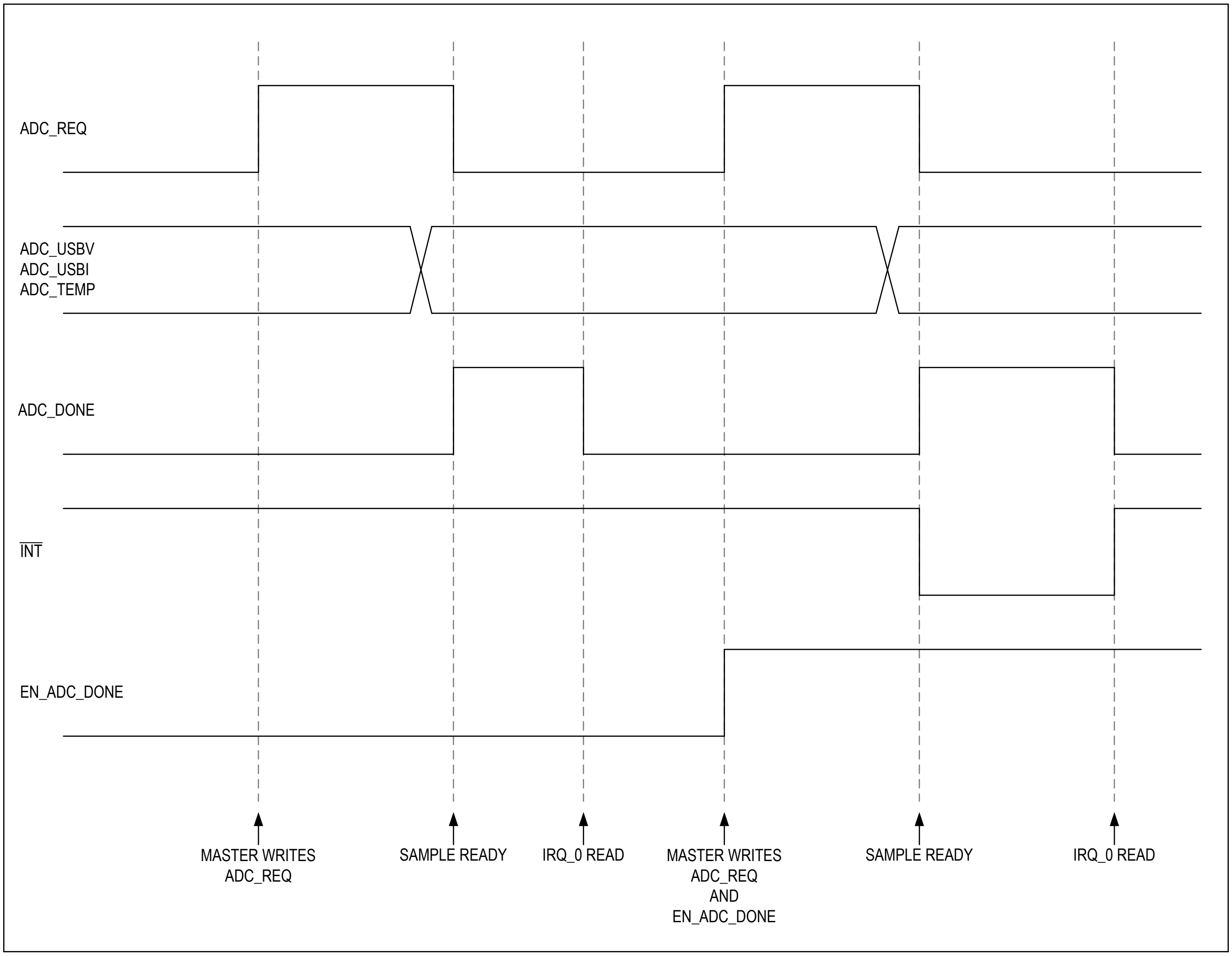
Functional Diagrams

DCDC_ON Reset Behavior and Timing Diagram



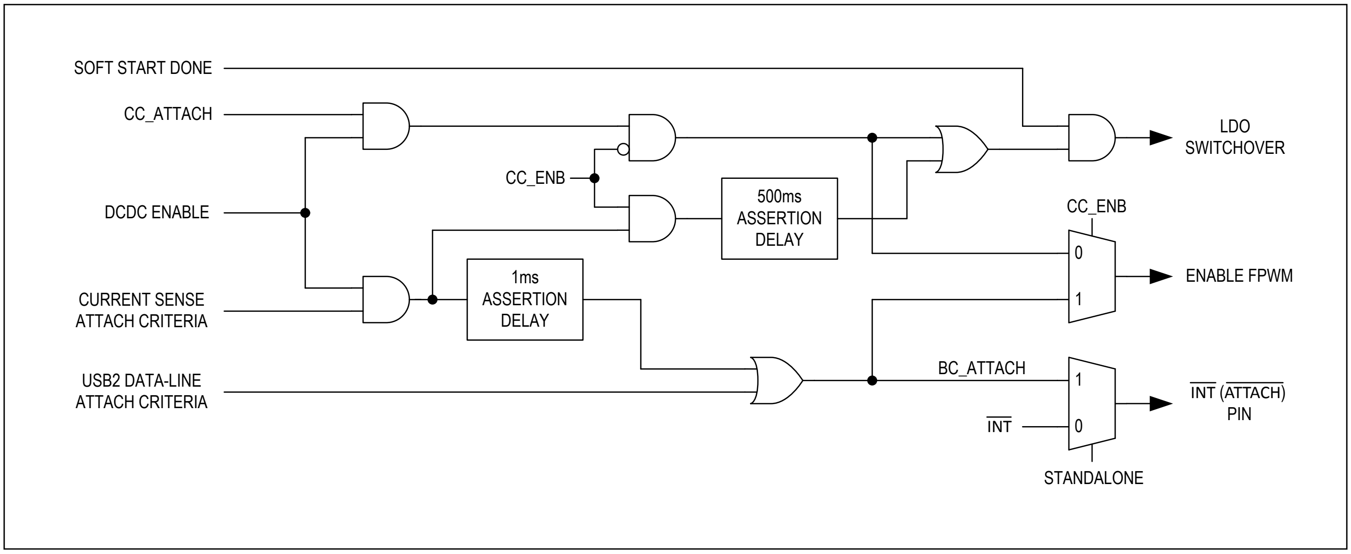
Functional Diagrams (continued)

ADC Timing Diagram

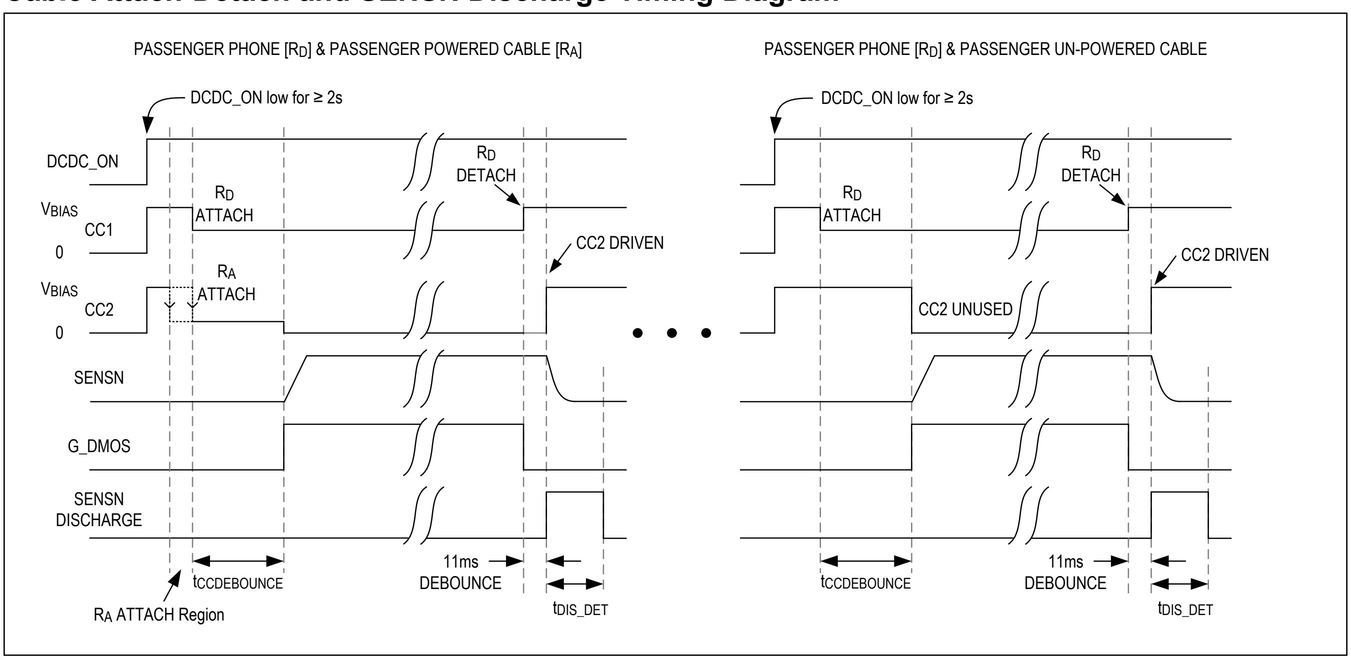


Functional Diagrams (continued)

ATTACH Logic Diagram

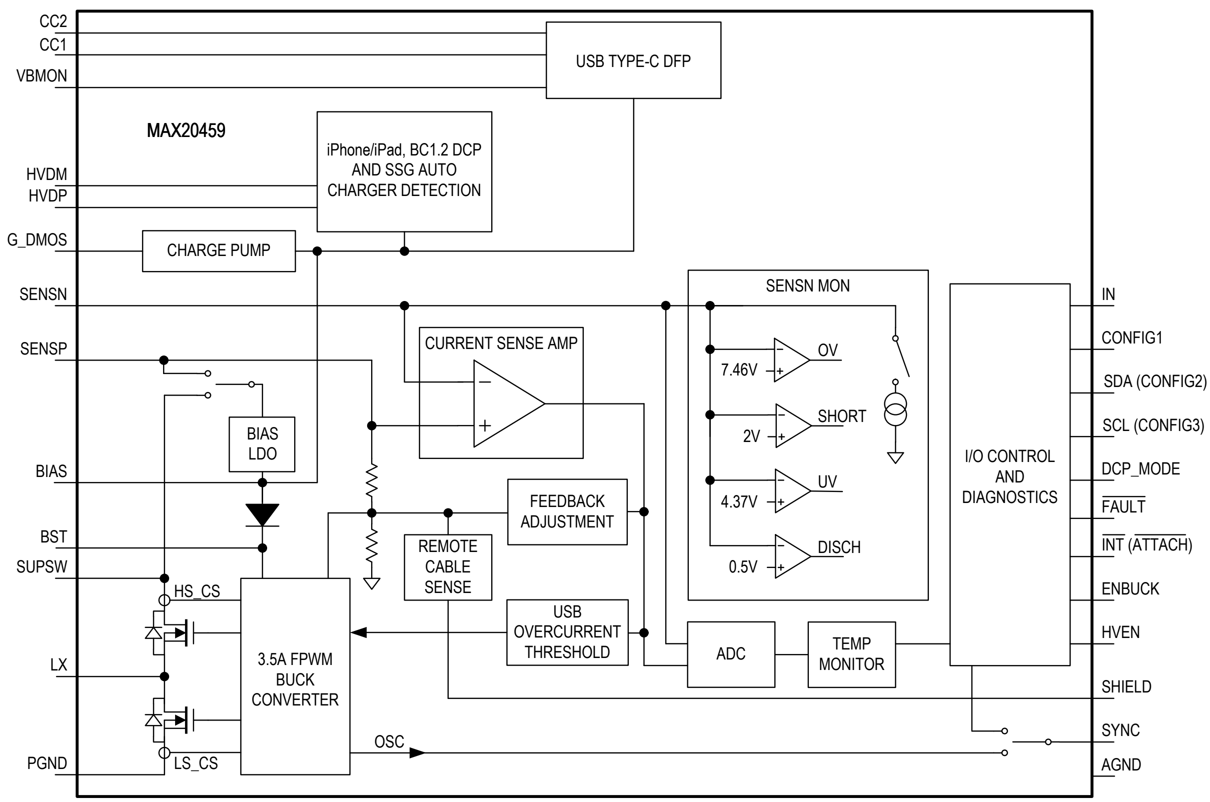


Cable Attach-Detach and SENSN Discharge Timing Diagram



Functional Diagrams (continued)

Detailed Block Diagram



Detailed Description

The MAX20459 combines a 5V/3A automotive-grade step-down converter and a USB Type-C host charger emulator. The MAX20459ATJA variant is configured through I^2C, while the MAX20459ATJC variant is configured using resistors connected to the CONFIG1, CONFIG2, and CONFIG3 pins. This device family is designed for high-power USB ports in automotive dedicated charging applications.

The MAX20459 HVD+ and HVD- pins are protected from shorts up to 18V, and include internal ESD protection circuitry.The internal host-charger port-detection circuitry offers automatic sensing and conformance to multiple standards, including USB Type-C 3.0A/1.5A/0.5A, USB-IF BC1.2 DCP mode, Apple 1A and 2.4A DCP modes, Samsung DCP, and China YD/T1591-2009.

The high-efficiency step-down DC-DC converter operates with an input voltage up to 28V and is protected from load-dump transients up to 40V. The DC-DC converter can be programmed for or synced to switching frequencies from 310kHz to 2.2MHz. The converter can deliver 3A of continuous current at an ambient temperature of 105°C.

The MAX20459 features a high-side current-sense amplifier and a programmable feedback-adjustment circuit designed to provide automatic USB voltage adjustment to compensate for voltage drops. The precision current-sense internal circuitry allows for an accurate DC output current limit, which minimizes the solution component size and cost.

USB Type-C

USB Type-C introduces a new connector, cable, and detection mechanism while maintaining backwards-compatibility with the existing USB ecosystem. The Type-C connector has a small form factor, is reversible, and bi-directional (eliminates the Type A/Type B distinction). To maintain the USB host/device relationship, Type-C requires a configuration channel (CC). The CC pins are used to advertise and detect current capabilities, but also device attachment.

A Type-C implementation supports, but does not require, BC1.2. It is also desirable to implement BC1.2 detection on HVDP/HVDM in addition to CC detection. This ensures the highest possible charge current when a legacy adapter is used. Table 1 shows the USB-IF mandated precedence of power negotiation, see USB Type-C 2.0 for details.

MAX20459 provides an integrated Type-C 5V solution tailored to the automotive market. The device integrates all control and power circuitry necessary to provide a 5V/3A Downstream Facing Port (DFP) with high conversion efficiency and low thermal footprint, additionally providing BC1.2 charge detection to maintain compatibility and enable fast charging.

Table 1. Charge Detection Precedence

PRECEDENCE	MODE OF OPERATION		NOMINAL VOLTAGE	MAXIMUM CURRENT
Highest	USB Type-C @ 3A Advertisement		5V	3A
	USB Type-C @ 1.5A Advertisement		5V	1.5A
	USB BC1.2		5V	≤1.5A
Lowest	Default USB Power	USB 3.1	5V	900 mA
		USB 2.0	5V	500 mA

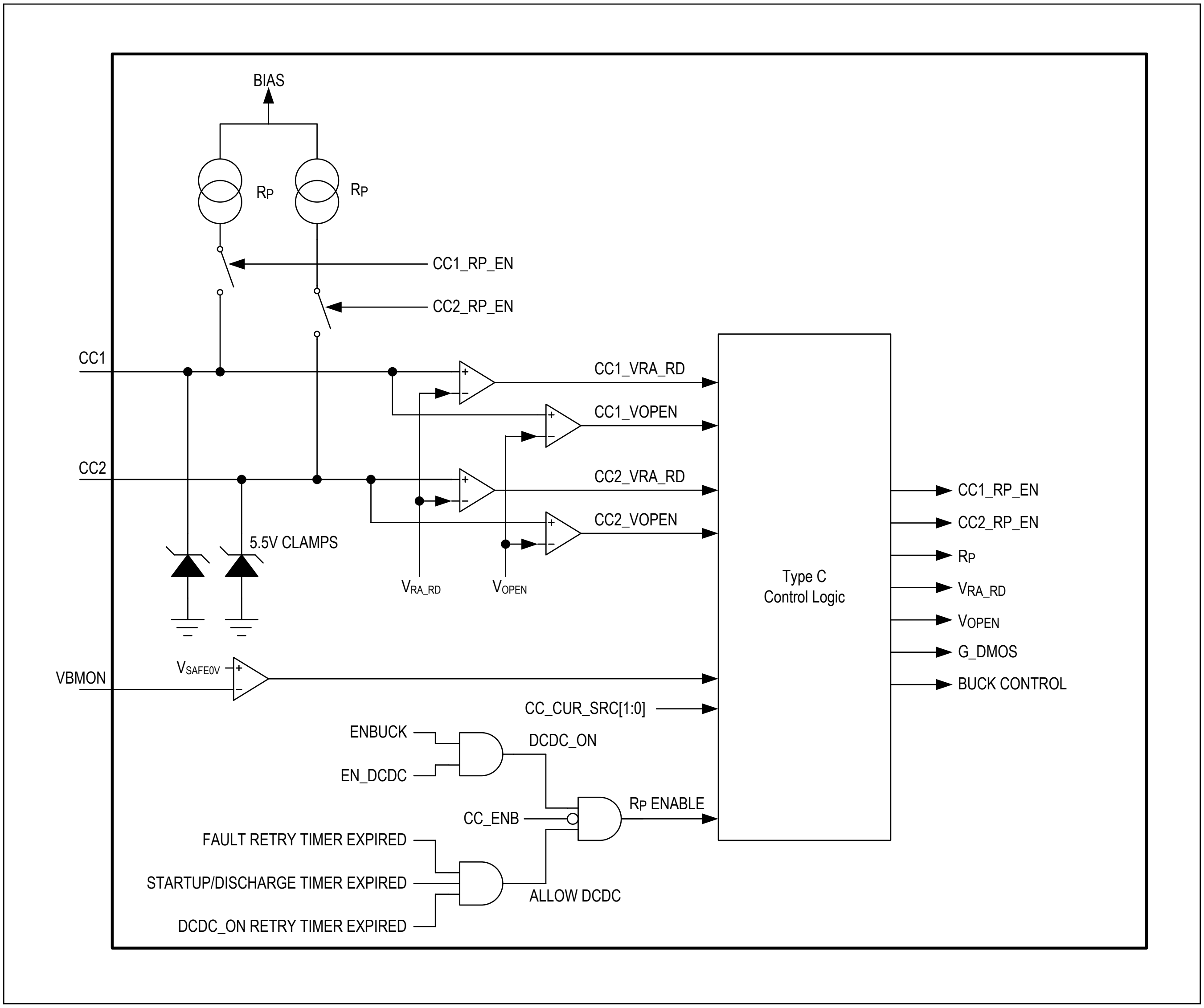


Figure 1. USB Type-C Block Diagram

V_{BUS}

Type-C includes new requirements for V_{BUS}, even when operating exclusively in 5V mode. When no device is attached to the CC pins, the host must turn the V_{BUS} source off so that a near-zero voltage is present at the receptacle pin. To achieve this, MAX20459 disables the external FET gate drive and turns off the buck converter when in a detached state, reducing quiescent current. The MAX20459 integrates control and discharge circuits to ensure all Type-C timing requirements are met. Throughout this document, the term V_{BUS} is used loosely to refer to voltage at SENSP, SENSN or VBMON. When more precision is required, the specific pin name is referenced.

External FET Gate Drive (G_DMOS Pin)

MAX20459 includes a gate drive for an optional external FET that can be used to isolate the bulk capacitance when V_{BUS} is not being sourced. A 2017 ECN from USB-IF increased the capacitance for source-only ports between V_{BUS} and GND when V_{BUS} is not being sourced from 10µF to 3000µF, effectively removing the need for an isolation FET. Therefore, the external FET on MAX20459 is optional.

If not used, terminate G_DMOS with a 2.7MΩ resistor to ground or a 10pF capacitor to ground. If used, connect the G_DMOS pin to the gate of the external FET. If V_{BUS} short-to-battery is required with the external FET, the FET should be appropriately rated. The external DMOS device must be a 20V V_{GS} type. The charge pump generates at least 7V.

Legacy Devices

The Type-C specification ensures inter-operability with Type-A/Type-B devices by defining requirements for legacy adapters. As a DFP, relevant adapters will connect from the Type-C receptacle to either a Type-B plug or to a Type-A receptacle, which can then be used with any legacy Type-A cable. A compliant legacy adapter of this type must include an R_D termination inside the adapter. In this case, MAX20459 will detect a Type-C attachment whenever the adapter is connected, regardless of whether a portable device is connected. The portable device will see the DFP as a BC1.2 port (when configured as such).

USB Type-A-Only Operation

The following configurations allow using MAX20459 as a Type-A charger:

- On the I²C variant, CC_ENB can be set to 1 to bypass the Type-C state machine and allow only Type-A operation.
- On the MAX20459 standalone variant, connect one of the CC pins to a 5.1kΩ resistor to ground and the other to a 100kΩ resistor to ground.

Power-Up and Enabling

System Enable (HVEN)

HVEN is used as the main enable to the device and initiates system start-up and configuration. If HVEN is at a logic-low level, SUPSW power consumption is reduced and the device enters a standby, low-quiescent-current level. HVEN is compatible with inputs from 3.3V logic up to automotive battery. After a system reset (e.g., HVEN toggle, BIAS UV), the I²C variant asserts the $\overline{INT}$ pin to indicate that the IC has not been configured. The buck converter is forced off until the CONFIGURED bit of SETUP_4 is written to a 1 and a device attachment has occurred. This ensures that a portable device cannot attach before the IC registers are correctly set for the application.

DC-DC Enable (ENBUCK)

The buck regulator on the MAX20459 is controlled by the ENBUCK pin for stand-alone variants, and by both the ENBUCK pin and the I²C interface for I²C variants. DCDC_ON, the logical AND of ENBUCK and DCDC_EN, determines if the buck converter can be enabled by the Type-C control logic. On stand-alone variants, DCDC_EN is always high and only ENBUCK can be used to enable the buck converter. On I²C variants, setting ENBUCK low overrides an I²C EN_DCDC enable command. ENBUCK can be directly connected to the BIAS or IN pin for applications that do not require GPIO control of the DC-DC converter enable.

3.3V Input (IN)

IN is used as a clamping voltage to protect the internal DCP circuitry pins during an ESD or overvoltage event on the HVD+ and HVD- pins. Bypass IN with a 1µF ceramic capacitor, place it close to the IN pin. For applications without a 3.3V rail available, provide the required voltage on IN by using a voltage divider from BIAS. Recommended values for the resistor divider are 1kΩ and 2kΩ, see Typical Application Circuits.

Linear Regulator Output (BIAS)

BIAS is the output of a 5V linear regulator that powers the internal logic, control circuitry, and DC-DC drivers. BIAS is internally powered from SUPSW or SENSP and automatically powers up when HVEN is high and SUPSW voltage exceeds V_{UV_SUPSW}. The BIAS output contains an undervoltage lockout that keeps the internal circuitry disabled when BIAS is below V_{UV_BIAS}. The linear regulator automatically powers down when HVEN is low, and the device enters low-shutdown-current mode. Bypass BIAS to GND with a 2.2µF ceramic capacitor as close to the pin as possible.

Power-On Sequencing

ENBUCK acts as the master disable for the DC-DC converter. If ENBUCK is low when HVEN is set high, all variants keep the buck converter in the disabled state until ENBUCK is set high.

Step-Down DC-DC Regulator

Step-Down Regulator

The MAX20459 features a current-mode, step-down converter with integrated high-side and low-side MOSFETs. The low-side MOSFET enables fixed-frequency, forced-PWM operation under light loads. The DC-DC features a cycle-by-cycle current limit, and intelligent transition from skip mode to forced-PWM mode which makes the devices ideal for automotive applications.

Wide Input Voltage Range

The device is specified for a wide 4.5V to 28V input voltage range. SUPSW provides power to the internal BIAS linear regulator and internal power switch. Certain conditions such as cold crank can cause the voltage at the output to drop below the programmed output voltage. Under such conditions, the device operates in a high duty-cycle mode to facilitate minimum dropout from input to output.

Maximum Duty-Cycle Operation

The MAX20459 has a maximum duty cycle of 98% (typ). The IC monitors the on-time (time for which the high-side FET is on) in both PWM and skip modes for every switching cycle. Once the on-time is detected continuously for 7.5μs, the low-side FET is forced on for 60ns (typ) every 7.5μs. The input voltage at which the device enters dropout changes depending on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design. The input voltage at which the device enters dropout can be approximated as:

$$V_{SUPSW} = \frac{V_{OUT} + \left(I_{LOAD} \times R_{ONH}\right)}{0.98}$$

Note: The equation above does not take into account the efficiency and switching frequency but will provide a good first-order approximation. Use the R_{ONH} (max) in the Electrical Characteristics table.

Output Voltage (SENSP)

The device features a precision internal feedback network connected to SENSP that is used to set the output voltage of the DC-DC converter. The network nominally sets the no-load DC-DC converter output voltage to 5.15V.

Soft-Start

When the DC-DC converter is enabled, the regulator initiates soft-start by gradually ramping up the output voltage from 0V to 5.15V in approximately 8ms. This soft-start feature reduces inrush current during startup and is guaranteed into compliant USB loads. See *USB Loads*.

Reset Behavior

The MAX20459 implements a discharge function on SENSN any time that the DC-DC regulator is disabled for any reason. When the discharge function is activated, current (I_{SENSN_DIS}) is drained through a current-limited FET and a reset timer is also started. This timer prevents the DC-DC regulator from starting up again until the timer has expired. This allows for easy compatibility with USB specifications, and removes the need for long discharge algorithms to be implemented in system software. See the relevant *Functional Diagrams* and Figure 1 for reset timer details.

Reset Criteria

The MAX20459 DC-DC converter will automatically reset for all undervoltage, overvoltage, overcurrent and overtemperature fault conditions. See Table 9 for details. The fault retry timer is configurable in the SETUP_3 register. This timer is activated after a fault condition is removed and prevents the buck converter from switching on until the timer expires.

Another internal retry timer is enabled after DCDC_ON is set low or a Type-C detach event. DCDC_ON toggle causes buck shutdown and prevents the buck from switching on until $t_{BUCKOFF\_CD}$ expires. A Type-C detach event will cause buck shutdown and prevent the buck from switching on until $t_{BUCKOFF\_DET}$ expires.

Switching Frequency Configuration

The DC-DC switching frequency can be referenced to an internal oscillator or from an external clock signal on the SYNC pin. The internal oscillator frequency is set by the FSW[2:0] bits of the SETUP_1 register, which has a POR value corresponding to 2.2MHz. The internal oscillator can be programmed via I^2C to eight discrete values from 310kHz to 2.2MHz. For standalone variants, FSW configuration value is loaded from the CONFIG1 pin at startup with four discrete values from 310kHz to 2.2MHz available.

Switching Frequency Synchronization (SYNC Pin)

When the SYNC pin is configured to operate as an output, skip mode operation is disallowed, and the internal oscillator drives the SYNC pin. This allows other devices to synchronize with the MAX20459 180 degrees out of phase for EMI reduction.

When SYNC is configured as an input, the SYNC pin becomes a logic-level input that can be used for both operating-mode selection and frequency control. Connecting SYNC to GND or an external clock enables fixed-frequency, forced-PWM mode. Connecting SYNC to a logic-high signal allows intelligent skip-mode operation (Type-A mode, i.e. CC_ENB = 1) or FPWM mode (default Type-C mode, i.e. CC_ENB = 0). The device can be externally synchronized to frequencies within ±20% of the programmed internal oscillator frequency.

Forced-PWM Operation

In forced-PWM mode, the device maintains fixed-frequency PWM operation over all load conditions, including no-load conditions.

Intelligent Skip-Mode Operation and Attach Detection

When the SYNC pin is configured as an input and CC_ENB = 1 (via I^2C only), but neither a clocked signal nor a logic-low level exists on the SYNC pin, the MAX20459 operates in skip mode at very light load/no load conditions. Intelligent device attach detection is used to determine when a device is attached to the USB port. The device intelligently exits skip mode and enters forced-PWM mode when a device is attached and remains in forced-PWM mode as long as the attach signal persists. This minimizes the EMI concerns caused by automotive captive USB cables and poorly shielded consumer USB cables. The device attach event is also signaled by the ATTACH pin (stand-alone variants) or ATTACH bits (I^2C variants). The criteria for device attach detection and intelligent skip-mode operation are shown in Table 2. Note that when operating in Type-C mode, the buck only switches on when a Type-C device is attached. This means skip mode cannot be entered if CC_ENB = 0.

Table 2. DC-DC Converter Intelligent Skip Mode Truth Table

CC_ENB	SYNC PIN	SYNC_ DIR BIT	DATA SWITCH CHARGE DETECTION MODE	DCP ATTACH DETECTION	CURRENT SENSE ATTACH DETECTION	DC-DC CONVERTER OPERATION
0	x	x	x	x	x	Forced-PWM Mode: Type-C Device Attached
1	x	1	x	x	x	Forced-PWM Mode: Continuous
1	0	0	x	x	x	Forced-PWM Mode: Continuous
1	Clocked	0	x	x	x	Forced-PWM Mode: Continuous
1	1	0	1A / 2.4A Auto DCP Modes	0	0	Intelligent Skip Mode: No Device Attached
1	1	0	1A / 2.4A Auto DCP Modes	1	x	Forced-PWM Mode: Device Attached

Table 2. DC-DC Converter Intelligent Skip Mode Truth Table (continued)

CC_ENB	SYNC PIN	SYNC_ DIR BIT	DATA SWITCH CHARGE DETECTION MODE	DCP ATTACH DETECTION	CURRENT SENSE ATTACH DETECTION	DC-DC CONVERTER OPERATION
1	1	0	1A / 2.4A Auto DCP Modes	x	1	Forced-PWM Mode: Device Attached

Spread-Spectrum Option

Spread-spectrum operation is offered to improve the EMI performance of the MAX20459. Spread-spectrum operation is enabled by the SS_EN bit of the SETUP_0 register, which is pre-loaded on startup from the CONFIG1 pin for both standalone and I²C variants. The internal operating frequency modulates the switching frequency by up to ±3.4% relative to the internally generated operating frequency. This results in a total spread-spectrum range of 6.8%. Spread-spectrum mode is only active when operating from the internal oscillator. Spread-spectrum clock dithering is not possible when operating from an external clock.

Current Limit

The MAX20459 limits the USB load current using both a fixed internal peak current threshold of the DC-DC converter, as well as a user-programmable external DC load current-sense amplifier threshold. This allows the current limit to be adjusted between 300mA and 3A, depending on the application requirements, and protects the system in the event of a fault. Upon exceeding either the LX peak or user-programmable current thresholds, the high-side FET is immediately turned off and current-limit algorithms are initiated. In some cases, the designer may want to increase the load to 160%, refer to *Selecting a Current-Sense Resistor* for details.

On the I²C variant, the ILIM_ITRIP bit of the SETUP_2 register determines the output voltage droop required to initiate a DC-DC converter reset during VBUS_ILIM. If the USB current limit is detected for 16ms, and the output voltage falls below the reset threshold (4.38V typ.) but stays above the 2.0V threshold, the $\overline{\text{FAULT}}$ pin asserts, the VBUS_ILIM bit of the IRQ_1 register is set, and the DC-DC converter resets (if ILIM_ITRIP = 0). Conversely, if ILIM_ITRIP = 1, the DC-DC converter will not reset, and it will keep acting as a current source.

On the standalone variant, if the USB current limit is detected for 16ms, and the output voltage falls below the reset threshold (4.38V typ.) but stays above the 2.0V threshold, the $\overline{\text{FAULT}}$ pin asserts, the DC-DC converter will not reset and will keep acting as a current source.

On all variants, the DC-DC converter immediately resets if the output voltage droops to less than 2.0V and either the external current threshold is exceeded, or the internal LX peak-current threshold is exceeded for four consecutive switching cycles.

Output Short-Circuit Protection

The DC-DC converter output (SENSP, SENSN) is protected against both short-to-ground and short-to-battery conditions. If a short-to-ground or undervoltage condition is encountered, the DC-DC converter immediately resets, asserts the $\overline{\text{FAULT}}$ pin, flags the fault in the IRQ_1 register, and then reattempts soft-start after the reset delay. This pattern repeats until the short circuit has been removed.

If a short-to-battery is encountered ($V_{SENSN} > V_{OV\_SENSN}$), the buck converter shuts down, G_DMOS is disabled, the $\overline{\text{FAULT}}$ pin is asserted, and the fault is flagged in the IRQ_1 register. The buck converter stays shutdown until the fault condition resolves and 2s timer expires.

Thermal Overload Protection

Thermal-overload protection limits the total power dissipated by the device. A thermal-protection circuit monitors the die temperature. If the die temperature exceeds +165°C, the device will shut down, allowing it to cool. Once the device has cooled by 10°C, the device is enabled again. This results in a pulsed output during continuous thermal-overload conditions, protecting the device during fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature of +150°C. See *Layout Considerations* for more information.

Pre-Thermal Overload Warning

The MAX20459 I^2C variant features a thermal overload warning flag which sets the THM_WARN bit of the IRQ_2 register when the die temperature crosses +140°C. This allows a system software implementation of thermal foldback or load shedding algorithms to prevent a thermal overload condition.

Automatic Thermal Foldback

The MAX20459 implements a thermal foldback feature that, when enabled, reduces the Type-C current limit and advertisement. On the standalone variant, when a thermal warning occurs, the output current limit and the R_P current advertisement are reduced to the setting immediately below what was set by the CONFIG3 resistor (i.e. Type-C R_P from 3.0A to 1.5A and ILIM from 3.04A to 2.60A). When the die temperature drops below the thermal-warning threshold, the R_P advertisement and current-limit threshold will return to their original settings based on the value of the CONFIG3 resistor. Note that CONFIGx resistor values are only read at POR.

On the I^2C variant, when a thermal warning occurs, the R_P current advertisement is reduced to the setting immediately below what was set by the CC_SRC_CUR[1:0] register (ie. Type-C R_P from 3.0A to 1.5A) and the current limit changes to 1.62A (min). When the die temperature drops below the thermal-warning threshold, the R_P advertisement and current-limit threshold will return to their original settings based on the values of CC_SRC_CUR[1:0] and ILIM[2:0] registers, respectively.

Note that Type-C allows for dynamic R_P changes in the Attached.SRC state without re-initializing detection. MAX20459 thermal foldback does not force BUS to reset or change the BC1.2 mode. Alternative thermal foldback algorithms are available and can be done in system software. Contact Maxim Applications for support.

USB Current-Limit and Output-Voltage Adjustment

Current-Sense Amplifier (SENSP, SENSN)

MAX20459 features an internal USB load current-sense amplifier to monitor the DC load current delivered to the USB port. The V_{SENSE} voltage (V_{SENSP} - V_{SENSN}) is used internally to provide precision DC current-limit and voltage-compensation functionality. A 33mΩ sense resistor should be placed between SENSP and SENSN.

In some cases, the designer may want to increase the load to 160%, refer to *Selecting a Current-Sense Resistor* for details.

USB DC Current Limit Configuration

The MAX20459 allows configuration of the precision DC current limit by the ILIM[2:0] bits of the SETUP_2 register. I^2C configuration enables selection of eight discrete DC current-limit values. See SETUP_2 for current-limit configuration values.

The standalone variant of the device allow selection of a subset of the eight available current-limit options by reading the CONFIG3 resistor. See Table 7 and the Applications Information section for more information.

In some cases, the designer may want to increase the load to 160%, refer to Selecting a Current-Sense Resistor for details.

Voltage Feedback Adjustment Configuration

The MAX20459 compensates voltage drop for up to 474mΩ of total series resistance on the V_{BUS} and GND path. Voltage gain is configured by selecting suitable resistors connected to CONFIG2 and CONFIG3 on the standalone variant, or by changing the GAIN[4:0] register on the I^2C variant.

In some cases, the designer may want to increase the load to 160%, refer to Selecting a Current-Sense Resistor for details.

Remote-Sense Feedback Adjustment (SHIELD Pin)

The remote-sense feature (available by custom order only) gives another option to adjust the output voltage by sensing the ground node on the USB port at the far end of the captive cable, either with the cable shield or with an additional sensing wire. This feature automatically senses the cable resistance and adjusts the voltage compensation without changing the GAIN[4:0] setting.

The user must compensate for the voltage drop due to the sense resistor, the load-line behavior of the buck, and any difference between the V_{BUS} and GND conductors. Contact Maxim Applications for support and ordering instructions.

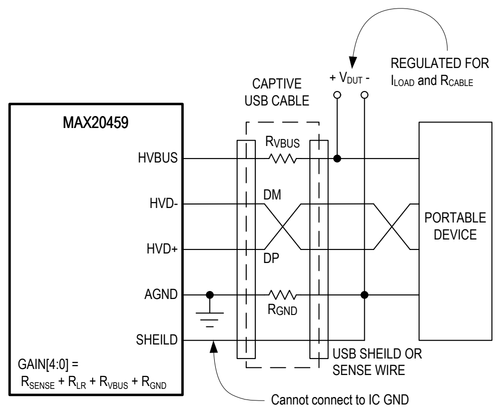


Figure 2. Remote Cable-Sense Diagram

High Voltage Modes Configuration

I²C variants of MAX20459 allow high output voltage mode configurations for flexible use in higher power charging applications, and for load-dump protected battery pass-through output to automotive modules. Contact Maxim Applications for support.

Automatic Charge Detection with ESD and Short-Circuit Protection

To maintain compatibility with non-Type-C devices, MAX20459 includes automatic dedicated charger-detection circuitry on the USB 2.0 data D+/D- lines. The device is compatible with Apple iPhone (1A), iPad (2.4A), BC1.2 DCP, and legacy Samsung charge-detection methods. See Table 3 for the I²C variant and Table 4 for the standalone variant.

The MAX20459 does not require an external ESD array, and protects the HVD+ and HVD- pins up to ±15kV Air Gap/±8kV Contact Discharge with the 150pF/330Ω IEC 61000-4-2 model, as well as protecting up to ±15kV Air Gap/±8kV Contact Discharge with the 330pF/2kΩ or 330pF/330Ω ISO 10605 model. See *ESD Protection* for additional information. Additionally, the HVD+ and HVD- short-circuit protection features include protection for short to +5V BUS and protection for short to +18V car battery.

Table 3. Charge-Detection Mode Truth Table (I²C Variant)

DEVICE SUFFIX	DEVICE INPUTS				SB SWITCHES	CHARGE-DETECTION MODE
	HVEN	CD[1]	CD[0]	DCP_MODE		
X	0	X	X	X	0	Off
ATJA	1	1	0	0	1	Auto-DCP/Apple 2.4A (DCP)
ATJA	1	1	1	0	1	Auto-DCP/Apple 1A (DCP)
ATJA	1	1	X	1	1	

Table 4. Charge-Detection Mode Truth Table (Standalone Variant)

DEVICE SUFFIX	DEVICE INPUTS		SB SWITCHES	CHARGE-DETECTION MODE
	HVEN	DCP_MODE		
X	0	X	0	Off
ATJC	1	0	1	Auto-DCP/Apple 2.4A (DCP)

Table 4. Charge-Detection Mode Truth Table (Standalone Variant) (continued)

ATJC	1	1	1	Auto-DCP/Apple 1A (DCP)

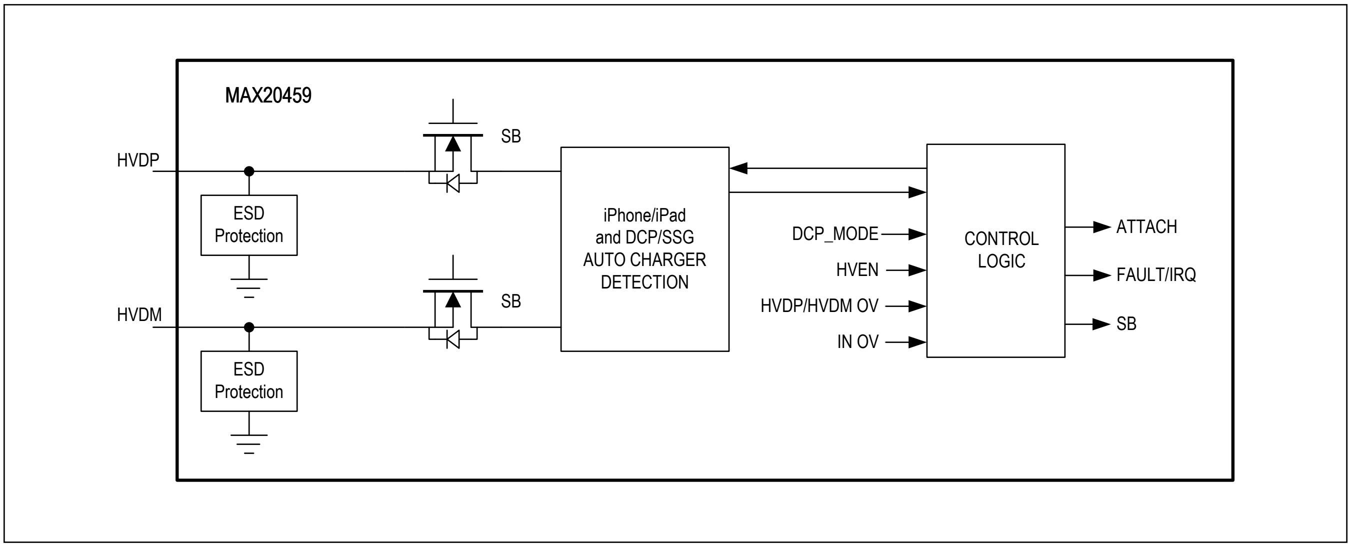


Figure 3. Charge Detection Block Diagram

I²C, Control, and Diagnostics

I²C Configuration (CONFIG1 and I²C)

The MAX20459 I²C variant allows basic device configuration through a resistor placed between the CONFIG1 pin and GND. The configuration parameters correlating to the chosen resistor are pre-loaded into their respective I²C registers on startup when HVEN is toggled high. After startup, the user is free to change the affected I²C registers as desired.

For the I²C variant, CONFIG1 sets the startup value of the DC-DC spread spectrum enable bit SS_EN and the SYNC direction-control bit SYNC_DIR. CONFIG1 also sets the two LSBs of the I²C slave address. The configuration table for the I²C variant CONFIG table is shown in Table 5.

In some cases, the designer may want to increase the load to 160%, refer to *Selecting a Current-Sense Resistor* for details.

Table 5. CONFIG1 Pin Table (I²C Version)

RESISTANCE (typ, Ω)	STEP	SS_EN	SYNC_DIR	I²C_ADDR LSBs
Short to GND	**0**	1 (ON)	1 (IN)	0b00
619	**1**	1 (ON)	1 (IN)	0b01
976	**2**	1 (ON)	1 (IN)	0b10
1370	**3**	1 (ON)	1 (IN)	0b11
1820	**4**	1 (ON)	0 (OUT)	0b00
2370	**5**	1 (ON)	0 (OUT)	0b01
3090	**6**	1 (ON)	0 (OUT)	0b10
3920	**7**	1 (ON)	0 (OUT)	0b11
4990	**8**	0 (OFF)	1 (IN)	0b00
6340	**9**	0 (OFF)	1 (IN)	0b01

Table 5. CONFIG1 Pin Table (I²C Version) (continued)

RESISTANCE (typ, Ω)	STEP	SS_EN	SYNC_DIR	I²C_ADDR LSBs
8250	**10**	0 (OFF)	1 (IN)	0b10
11000	**11**	0 (OFF)	1 (IN)	0b11
15400	**12**	0 (OFF)	0 (OUT)	0b00
23700	**13**	0 (OFF)	0 (OUT)	0b01
44200	**14**	0 (OFF)	0 (OUT)	0b10
Short to BIAS (or R > 71.5kΩ)	**15**	0 (OFF)	0 (OUT)	0b11

Standalone Configuration (CONFIG1–CONFIG3)

The MAX20459 standalone variant allows full device configuration from three resistors placed among the three CONFIG pins and AGND. CONFIG1 sets the internal oscillator switching frequency, the SYNC pin direction, and enables the DC-DC spread-spectrum mode. CONFIG2 sets the 4 LSBs of the voltage adjustment gain (GAIN[3:0]). CONFIG3 sets the USB DC current limit and sets the MSB of voltage-adjustment gain (GAIN[4]). See Table 6 and Table 7 for CONFIG options. See the GAIN[4:0] register description for lookup values. See the *Applications Information* section for setting selection and *Ordering Information* for variant part number information.

Table 6. CONFIG1 Pin Table (Standalone Variant)

RESISTANCE (typ, Ω)	STEP	SS_EN	SYNC_DIR	FSW (kHz)
Short to GND	**0**	ON	IN	2200
619	**1**	ON	IN	488
976	**2**	ON	IN	350
1370	**3**	ON	IN	310
1820	**4**	ON	OUT	2200
2370	**5**	ON	OUT	488
3090	**6**	ON	OUT	350
3920	**7**	ON	OUT	310
4990	**8**	OFF	IN	2200
6340	**9**	OFF	IN	488
8250	**10**	OFF	IN	350
11000	**11**	OFF	IN	310
15400	**12**	OFF	OUT	2200
23700	**13**	OFF	OUT	488
44200	**14**	OFF	OUT	350
Short to BIAS (or R > 71.5kΩ)	**15**	OFF	OUT	310

Table 7. CONFIG2 and CONFIG3 Pin Table (Standalone Variant)

RESISTANCE (typ, Ω)	STEP	GAIN[3:0]	THM_FLDBK_EN	GAIN[4]	CURRENT LIMIT (A, min)	TYPE-C MODE (A)
		CONFIG2	**CONFIG3**			
Short to GND	**0**	0b0000	1 (ON)	0	0.55	0.5
619	**1**	0b0001	1 (ON)	0	1.62	1.5
976	**2**	0b0010	1 (ON)	0	2.60	1.5

Table 7. CONFIG2 and CONFIG3 Pin Table (Standalone Variant) (continued)

RESISTANCE (typ, Ω)	STEP	GAIN[3:0]	THM_FLDBK_EN	GAIN[4]	CURRENT LIMIT (A, min)	TYPE-C MODE (A)
1370	**3**	0b0011	1 (ON)	0	3.04	3.0
1820	**4**	0b0100	1 (ON)	1	0.55	0.5
2370	**5**	0b0101	1 (ON)	1	1.62	1.5
3090	**6**	0b0110	1 (ON)	1	2.60	1.5
3920	**7**	0b0111	1 (ON)	1	3.04	3.0
4990	**8**	0b1000	0 (OFF)	0	0.55	0.5
6340	**9**	0b1001	0 (OFF)	0	1.62	1.5
8250	**10**	0b1010	0 (OFF)	0	2.60	1.5
11000	**11**	0b1011	0 (OFF)	0	3.04	3.0
15400	**12**	0b1100	0 (OFF)	1	0.55	0.5
23700	**13**	0b1101	0 (OFF)	1	1.62	1.5
44200	**14**	0b1110	0 (OFF)	1	2.60	1.5
Short to BIAS (or R > 71.5kΩ)	**15**	0b1111	0 (OFF)	1	3.04	3.0

I²C Diagnostics and Event Handling

The I²C-based diagnostic functionality is independent of the $\overline{\text{FAULT}}$ pin. Setting the IRQMASK bit for a specific fault condition will not mask the $\overline{\text{FAULT}}$ pin for the respective fault. IRQMASK register functionality affects only the behavior of the $\overline{\text{INT}}$ pin. This allows the $\overline{\text{FAULT}}$ pin to be tied to overcurrent fault input of a hub controller or SoC, while the I²C interface is simultaneously used by the system software for advanced diagnostic functionality.

Interrupt and Attach Output ($\overline{\text{INT}}$($\overline{\text{ATTACH}}$))

The MAX20459 $\overline{\text{INT}}$($\overline{\text{ATTACH}}$) pin functions as an interrupt ($\overline{\text{INT}}$) for the I²C variant. The $\overline{\text{INT}}$ pin will assert an interrupt based on the configuration of the IRQ_MASK_0, IRQ_MASK_1, and IRQ_MASK_2 registers. Interrupt configuration allows the $\overline{\text{INT}}$ pin to assert any of the featured fault detection, as well as on device attach/detach, and for USB voltage/current ADC conversion completion. The $\overline{\text{INT}}$ pin will only assert while a masked IRQ bit is asserted, which means that its behavior is also dependent on the IRQ_AUTOCLR bit.

The standalone variant of MAX20459 feature an open-drain, active-low, $\overline{\text{ATTACH}}$ output that serves as the attach-detection pin for standalone variants. The $\overline{\text{ATTACH}}$ pin can be used for GPIO input to a microprocessor, or to drive an LED for attach/charge indication.

The $\overline{\text{INT}}$($\overline{\text{ATTACH}}$) assertion logic is shown in *ATTACH Logic Diagram*.

I²C Output Voltage and Current Measurement

The MAX20459 I²C variant allows measurement of the instantaneous SENSN voltage and DC output current using an integrated ADC. To initiate a measurement, set the ADC_REQ bit of the ADC_REQUEST register. The ADC_REQ bit will be cleared by the IC once the measurement is complete and the ADC samples are available. Additionally, the ADC_DONE bit of the IRQ_0 register will be set when the sample is available. ADC_DONE can be masked to assert an interrupt when the sample is ready.

The sampled measurements can be read from the ADC_USBV, ADC_USBI, and ADC_TEMP registers. The new sample will persist in the register until another sample request is initiated by setting the ADC_REQ bit.

All measurements provide 8 bits of resolution. The measured SENSN voltage has a range of 0V to 19.8V. Convert the sample to a voltage by:

$$V_{SENSN} = \frac{19.8V}{256} \cdot \text{ADC\_USBV (Volts)}$$

The measured SENSE voltage has a range of 0 to 116mV. Convert the sample to a current by:

$$I_{LOAD} = \frac{116mV}{256} \cdot \frac{ADC\_USBI}{R_{SENSE}} \text{ (Amps)}$$

The measured die temp has a range from -40ºC to 170ºC and a temperature resolution of 3.5ºC. Convert the sample to a die temperature by T_J = 3.5ºC · ADC_TEMP - 270 (ºC).

I^2C Interface

The MAX20459 features an I^2C, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the MAX20459 and the master at clock rates up to 400kHz. The master, typically a microcontroller, generates SCL and initiates data transfer on the bus. Figure 4 shows the 2-wire interface timing diagram.

A master device communicates to the MAX20459 by transmitting the proper address followed by the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The MAX20459 SDA line operates as both an input and an open-drain output. A pullup resistor greater than 500Ω is required on the SDA bus. The MAX20459 SCL line operates as an input only. A pullup resistor greater than 500Ω is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. The SCL and SDA inputs suppress noise spikes to assure proper device operation even on a noisy bus.

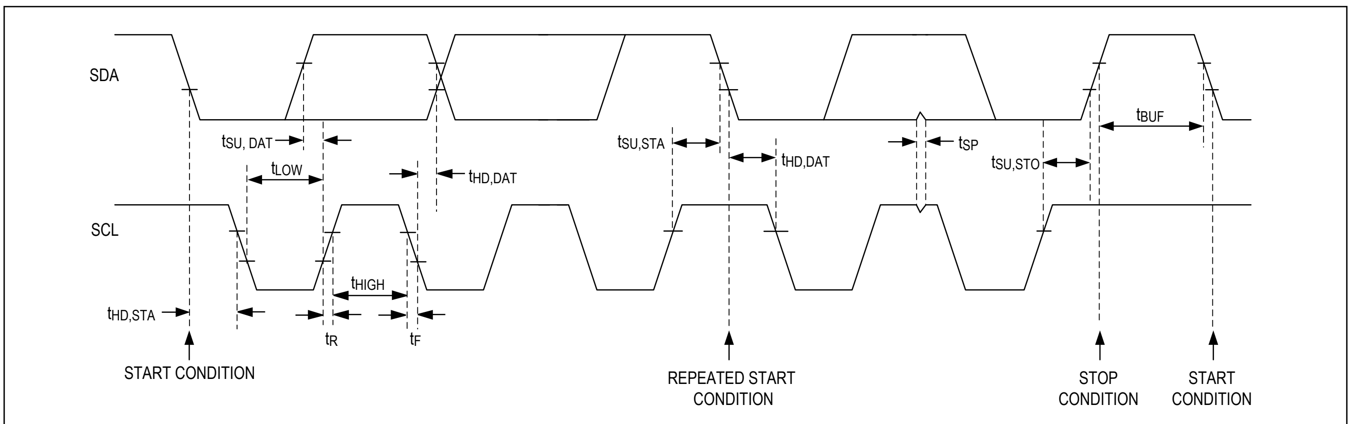


Figure 4. I^2C Timing Diagram

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see *STOP and START Conditions*). SDA and SCL idle high when the I^2C bus is not busy.

STOP and START Conditions

A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 5). A START (S) condition from the master signals the beginning of a transmission to the MAX20459. The master terminates transmission, and frees the bus, by issuing a STOP (P) condition. The bus remains active if a REPEATED START (Sr) condition is generated instead of a STOP condition.

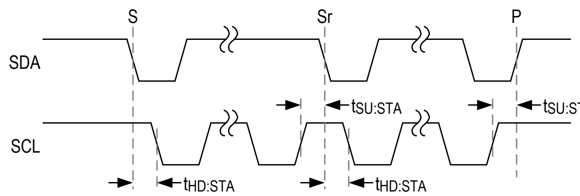


Figure 5. START, STOP and REPEATED START Conditions

Early STOP Condition

The MAX20459 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition.

Clock Stretching

In general, the clock signal generation for the I²C bus is the responsibility of the master device. The I²C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The MAX20459 does not use any form of clock stretching to hold down the clock line.

I²C General Call Address

The MAX20459 does not implement the I²C specification general call address. If the MAX20459 sees the general call address (0b0000_0000), it will not issue an acknowledge.

I²C Slave Addressing

Once the device is enabled, the I²C slave address is set by the CONFIG1 pin.

The address is defined as the 7 most significant bits (MSBs) followed by the R/W bit. Set the R/W bit to 1 to configure the devices to read mode. Set the R/W bit to 0 to configure the device to write mode. The address is the first byte of information sent to the devices after the START condition.

Table 8. I²C Slave Addresses

CONFIG1 CODE	A6	A5	A4	A3	A2	A1	A0	7-BIT ADDRESS	WRITE	READ
0b00	0	1	1	0	0	0	0	0x30	0x60	0x61
0b01	0	1	1	0	0	0	1	0x31	0x62	0x63
0b10	0	1	1	0	0	1	0	0x32	0x64	0x65
0b11	0	1	1	0	0	1	1	0x33	0x66	0x67

Acknowledge

The acknowledge bit (ACK) is a clocked ninth bit that the device uses to handshake receipt of each data byte (Figure 6). The device pulls down SDA during the master-generated ninth clock pulse. The SDA line must remain stable and low during the high period of the acknowledge clock pulse. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master can reattempt communication.

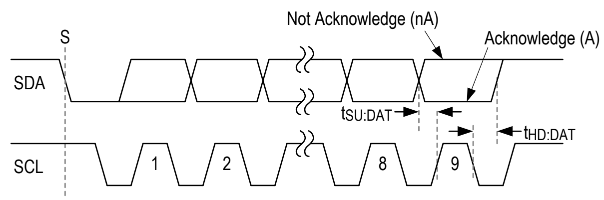


Figure 6. Acknowledge Condition

Write Data Format

A write to the device includes transmission of the following:

- START condition
- Slave address with the write bit set to 0,
- 1 byte of data to register address
- 1 byte of data to the command register
- STOP condition.

Read Data Format

A read from the device includes transmission of the following:

- START condition
- Slave address with the write bit set to 0
- 1 byte of data to register address
- Restart condition
- Slave address with read bit set to 1
- 1 byte of data to the command register
- STOP condition

Figure 7 illustrates the proper format for one frame.

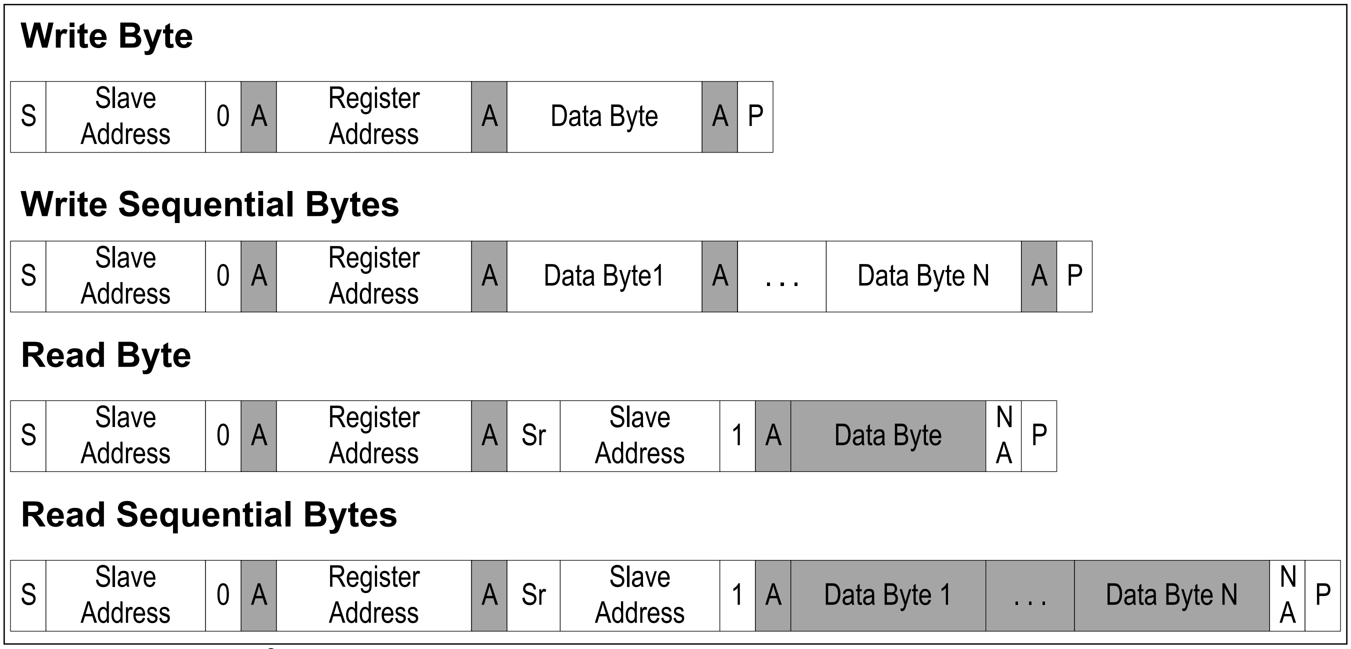


Figure 7. Data Format of I²C Interface

Fault Detection and Diagnostics

Fault Detection

The MAX20459 features advanced device-protection features with automatic fault handing and recovery. Table 9 summarizes the conditions that generate a fault, and the actions taken by the device. For all variants, the $\overline{\text{FAULT}}$ output remains asserted as long as a fault condition persists.

Fault Output Pin ($\overline{\text{FAULT}}$)

The MAX20459 features an open-drain, active-low $\overline{\text{FAULT}}$ output. The MAX20459 is designed to eliminate false $\overline{\text{FAULT}}$ reporting by using an internal deglitch and fault-blanking timer. This ensures that $\overline{\text{FAULT}}$ is not falsely asserted during normal operation such as starting into heavy capacitive loads. The $\overline{\text{FAULT}}$ pin is designed such that it can be tied directly to the fault input of a microcontroller or used to enable an LED.

Table 9. Fault Conditions

EVENT	IRQ REGISTER BITS (I²C ONLY)	DEBOUNCE PRIOR TO ACTION	ACTION TAKEN
Thermal Shutdown	THM_SHD	Immediate	Assert $\overline{\text{FAULT}}$ pin, shut down DC-DC converter, disconnect charge-detection circuitry, and disable R_P. When fault resolves and RETRY_TMR expires, release $\overline{\text{FAULT}}$ pin, enable R_P and DC-DC converter.
Thermal Warning/ Foldback	THM_WARN	20 ms	If enabled, initiate thermal-foldback algorithm by reducing the type-C R_P by one step and current limit. When fault resolves and RETRY_TMR expires, return to original current-advertisement and current-limit settings.
IN Overvoltage	IN_OV	Immediate	Assert $\overline{\text{FAULT}}$ pin and associated IRQ bit, shut down DC-DC converter, disconnect charge-detection circuitry, disable R_P, and reset BC1.2. When fault resolves and RETRY_TMR expires, release $\overline{\text{FAULT}}$ pin, reconnect charge detection circuitry, enable R_P and DC-DC converter.

Table 9. Fault Conditions (continued)

EVENT	IRQ REGISTER BITS (I^2C ONLY)	DEBOUNCE PRIOR TO ACTION	ACTION TAKEN
HVDP/HVDM Overvoltage	DATA_OV	Immediate	Assert $\overline{FAULT}$ pin, shut down DC-DC converter, disconnect charge-detection circuitry, disable R_P, and reset BC1.2. When fault resolves and RETRY_TMR expires, release $\overline{FAULT}$ pin, reconnect charge detection circuitry, enable R_P and DC-DC converter.
USB DC Overcurrent	VBUS_ILIM	16 ms	Assert $\overline{FAULT}$ pin after overcurrent condition persists for 16ms. When fault resolves and RETRY_TMR expires, release $\overline{FAULT}$ pin.
USB DC Overcurrent and SENSN < 4.38V	VBUS_ILIM_UV	16 ms	Standalone variant or I²C variant with ILIM_ITRIP = 1: Assert $\overline{FAULT}$ pin after overcurrent and undervoltage condition persists for 16ms. When fault resolves and RETRY_TMR expires, release $\overline{FAULT}$ pin. I²C variant and ILIM_ITRIP = 0: Assert $\overline{FAULT}$ pin, shut down DC-DC converter, and disable R_P after overcurrent and undervoltage condition persists for 16ms. When RETRY_TMR expires after shutdown, release $\overline{FAULT}$ pin, enable R_P and DC-DC converter.
SENSN < 4.38V	VBUS_UV	16 ms	Assert $\overline{FAULT}$ pin after undervoltage condition persists for 16ms. When fault resolves and RETRY_TMR expires, release $\overline{FAULT}$ pin.
USB DC Overcurrent and SENSN < 2V	VBUS_SHT_GND	Immediate	Assert $\overline{FAULT}$ pin, shut down DC-DC converter, disconnect charge-detection circuitry, and disable R_P. When RETRY_TMR expires after shutdown, release $\overline{FAULT}$ pin, reconnect charge detection circuitry, enable R_P and DC-DC converter.
LX Overcurrent for Four Consecutive Cycles and SENSN < 2V	VBUS_SHT_GND	Immediate	Assert $\overline{FAULT}$ pin, shut down DC-DC converter, disconnect charge detection circuitry, and disable R_P. When RETRY_TMR expires after shutdown, release $\overline{FAULT}$ pin, reconnect charge detection circuitry, enable R_P and DC-DC converter.
SENSN Overvoltage	VBUS_OV	Immediate	Assert $\overline{FAULT}$ pin and associated IRQ bit, shut down DC-DC converter, disconnect charge detection circuitry, and disable R_P. When fault resolves and RETRY_TMR expires, release $\overline{FAULT}$ pin, reconnect charge detection circuitry, enable R_P and DC-DC converter.
V_{BUS} Pre-Overvoltage	VBUS_PRE_OV	16 ms	Assert $\overline{FAULT}$ pin and associated IRQ bit after overvoltage condition persists for 16ms. After overvoltage no longer exists and RETRY_TMR expires, release $\overline{FAULT}$ pin.

Register Map

Summary Table

ADDRESS	NAME	MSB							LSB
USER_CMDS									
0x00	SETUP_0[7:0]	–	THM_FLDBK_EN	EN_DCDC	VOUT[2:0]			SYNC_DIR	SS_EN
0x01	SETUP_1[7:0]	FSW[2:0]			GAIN[4:0]				
0x02	SETUP_2[7:0]	–	–	–	ILIM_ITRIP	–	ILIM[2:0]		
0x03	SETUP_3[7:0]	RETRY_TMR[1:0]		CD[1:0]		CC_ENB	–	CC_SRC_CUR[1:0]	
0x04	SETUP_4[7:0]	–	–	–	–	–	–	–	CONFIGURED
0x05	ADC_REQUEST[7:0]	–	–	–	–	–	–	–	ADC_REQ
0x06	CC_REQUEST[7:0]	–	–	–	–	–	–	CC_FORCE_ERR	CC_SRC_RST
0x07	IRQ_MASK_0[7:0]	IRQ_AUTOCLR	–	EN_CC_STATE_EV	EN_CC_ATTACH_IRQ	EN_BC_ATTACH_IRQ	EN_CC_ATTACH_EV	EN_BC_ATTACH_EV	EN_ADC_DONE
0x08	IRQ_MASK_1[7:0]	–	EN_VBUS_PRE_OV	EN_VBUS_ILIM_UV	EN_VBUS_ILIM	EN_VBUS_OV	EN_VBUS_UV	EN_VBUS_SHT_GND	EN_THM_SHD
0x09	IRQ_MASK_2[7:0]	–	–	EN_VBUS_PREBIAS	–	EN_THM_WARN	EN_IN_OV	EN_DATA_OV	–
0x0A	IRQ_0[7:0]	UNCONFIGURED	–	CC_STATE_EV	CC_ATTACH_IRQ	BC_ATTACH_IRQ	CC_ATTACH_EV	BC_ATTACH_EV	ADC_DONE
0x0B	IRQ_1[7:0]	–	VBUS_PRE_OV	VBUS_ILIM_UV	VBUS_ILIM	VBUS_OV	VBUS_UV	VBUS_SHT_GND	THM_SHD
0x0C	IRQ_2[7:0]	–	–	VBUS_PREBIAS	–	THM_WARN	IN_OV	DATA_OV	–
0x0D	STATUS_0[7:0]	–	–	–	CC_ATTACH	BC_ATTACH	VBMON_SAFE	–	VBUS_STAT
0x0E	STATUS_1[7:0]	–	–	CC_PIN_STATE[1:0]		CC_STATE[3:0]			
0x10	ADC_0[7:0]	ADC_USBI[7:0]							
0x11	ADC_1[7:0]	ADC_USBV[7:0]							
0x12	ADC_2[7:0]	ADC_TEMP[7:0]							

Register Details

SETUP_0 (0x0)

BIT	7	6	5	4	3	2	1	0
Field	–	THM_FLDBK_EN	EN_DCDC	VOUT[2:0]			SYNC_DIR	SS_EN
Reset	–	0b0	0b1	0b000				
Access Type	–	Write, Read	Write, Read	Write, Read			Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
THM_FLDBK_EN	6	Lowers the type-C advertised current capability and the output current limit when Thermal Warning is tripped.	0 = Disable Thermal Foldback 1 = Enable Thermal Foldback
EN_DCDC	5	DC/DC Converter Enable. Internally AND'ed with the ENBUCK pin	0 = Disable V_{BUS} Buck Converter 1 = Enable V_{BUS} Buck Converter
VOUT	4:2	V_{BUS} Output Level Selection	0b000 = 5V 0b001 = 9V 0b010 = 12V 0b011 = 15V 0b100 = 18V (protected battery pass-through) 0b101 = 5V 0b110 = 5V 0b111 = 5V
SYNC_DIR	1	SYNC Pin Direction Selection. Initial value set by CONFIG1 resistor.	0 = Output 1 = Input
SS_EN	0	Spread Spectrum Enable. Initial value set by CONFIG1 resistor.	0 = Disable spread-spectrum function 1 = Enable spread-spectrum function

SETUP_1 (0x1)

BIT	7	6	5	4	3	2	1	0
Field	FSW[2:0]			GAIN[4:0]				
Reset	0b000			0b00000				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
FSW	7:5	DC/DC Convertor Switching-Frequency Selection. Initial value set by CONFIG1 resistor.	0b000 = 2200 kHz 0b001 = 1200 kHz 0b010 = 790 kHz 0b011 = 600 kHz 0b100 = 488 kHz 0b101 = 410 kHz 0b110 = 350 kHz 0b111 = 310 kHz

BITFIELD	BITS	DESCRIPTION	DECODE
GAIN	4:0	The gain of the voltage correction applied to the buck converter output (based on DC load sensed by current-sense amp). R_{SENSE} = 33mΩ.	0: 0mΩ 1: 18mΩ 2: 36mΩ 3: 54mΩ 4: 72mΩ 5: 90mΩ 6: 108mΩ 7: 126mΩ 8: 144mΩ 9: 162mΩ 10: 180mΩ 11: 198mΩ 12: 216mΩ 13: 234mΩ 14: 252mΩ 15: 270mΩ 16: 288mΩ 17: 306mΩ 18: 324mΩ 19: 342mΩ 20: 360mΩ 21: 378mΩ 22: 396mΩ 23: 414mΩ 24: 432mΩ 25: 450mΩ 26: 468mΩ 27: 486mΩ 28: 504mΩ 29: 522mΩ 30: 540mΩ 31: 558mΩ

SETUP_2 (0x2)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ILIM_ITRIP	–	ILIM[2:0]		
Reset	–	–	–	0b1	–	0b111		
Access Type	–	–	–	Write, Read	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ILIM_ITRIP	4	Determines the buck's retry behavior under USB DC current-limit conditions	0 = VBUS_ILIM_UV fault enabled, VBUS_ILIM fault disabled 1 = VBUS_ILIM_UV fault disabled, VBUS_ILIM fault enabled

BITFIELD	BITS	DESCRIPTION	DECODE
ILIM	2:0	USB DC current-limit threshold. R_{SENSE} = 33mΩ.	USB DC Current-Limit Threshold (min in Amps) 0b000 = 0.3 0b001 = 0.55 0b010 = 0.8 0b011 = 1.05 0b100 = 1.62 0b101 = 2.1 0b110 = 2.6 0b111 = 3.04

SETUP_3 (0x3)

BIT	7	6	5	4	3	2	1	0
Field	RETRY_TMR[1:0]		CD[1:0]		CC_ENB	–	CC_SRC_CUR[1:0]	
Reset	0b00				0b0	–	0b01	
Access Type	Write, Read		Write, Read		Write, Read	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RETRY_TMR	7:6	Determines the length of the RETRY timer after a fault condition	0b00 = 2.0s 0b01= 1.0s 0b10 = 0.5s 0b11= 16ms
CD	5:4	BC1.2 Charge-Detection Configuration Selection. This register is preloaded at startup with 0b10 when DCP_MODE = 0 and with 0b11 when DCP_MODE = 1.	0b00 = Reserved 0b01 = Reserved 0b10 = Auto-DCP/Apple 2.4A 0b11 = Auto-DCP/Apple 1.0A
CC_ENB	3	Disable Type-C Detection	0 = Type-C Enabled 1 = Type-C Disabled (for Type-A operation only)
CC_SRC_CUR	1:0	Type-C DFP Source Pullup Current Advertisement (R_P).	0b00 = 0.5A 0b01 = 1.5A 0b10 = 3.0A 0b11 = 0.5A

SETUP_4 (0x4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	CONFIGURED
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CONFIGURED	0	I^2C Configuration Complete Indicator. Upon power-up, the buck converter is prevented from turning on until this bit is written to a one, indicating the part is fully configured for its intended mode of operation.	0 = I^2C configuration pending 1 = I^2C configuration complete

ADC_REQUEST (0x5)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	ADC_REQ
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ADC_REQ	0	ADC V/I Sample Request. When a 1 is written, ADC V/I sampling is initiated. This bit is cleared once the requested sampling is complete and the ADC results are updated. The status of the ADC conversion (data ready) can be monitored in the IRQ0 register.	0 = No ADC sample requested 1 = ADC sample requested

CC_REQUEST (0x6)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	CC_FORCE_ERR	CC_SRC_RST
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CC_FORCE_ERR	1	Type-C Force Error Request. This is a request bit (write-only). Forces the Type-C state machine to go through error recovery. This bit will always read back zero.	0 = No change to current operating state 1 = Force transition to Error Recovery state
CC_SRC_RST	0	Type-C Force Source Reset Request. This is a request bit (write-only). The Type-C state machine will be forced back to the UnAttached.SRC state, restarting Type-C detection. This bit will always read back 0.	0 = No change to current operating state 1 = Force transition to UnAttached.SRC state

IRQ_MASK_0 (0x7)

A read-write register that configures which of the conditions in the IRQ_0 register will assert an Interrupt. See the IRQ_0 register for condition descriptions.

BIT	7	6	5	4	3	2	1	0
Field	IRQ_AUTOCLR	–	EN_CC_STATE_EV	EN_CC_ATTACH_IRQ	EN_BC_ATTACH_IRQ	EN_CC_ATTACH_EV	EN_BC_ATTACH_EV	EN_ADC_DONE
Reset	0b0	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
IRQ_AUTOCLR	7	IRQ Autoclear	0 = IRQ register flags are latched on until read 1 = IRQ register flags are automatically cleared when the error condition is removed
EN_CC_STATE_EV	5	CC_STATE Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_CC_ATTACH_IRQ	4	Type-C ATTACH STATUS Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_BC_ATTACH_IRQ	3	BC1.2 ATTACH STATUS Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_CC_ATTACH_EV	2	Type-C ATTACH EVENT Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_BC_ATTACH_EV	1	BC1.2 ATTACH EVENT Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_ADC_DONE	0	ADC_DONE Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt

IRQ_MASK_1 (0x8)

A read-write register that configures which of the conditions in the IRQ_1 register will assert an Interrupt. See the IRQ_1 register for condition descriptions.

BIT	7	6	5	4	3	2	1	0
Field	–	EN_VBUS_PRE_OV	EN_VBUS_ILIM_UV	EN_VBUS_ILIM	EN_VBUS_OV	EN_VBUS_UV	EN_VBUS_SHT_GND	EN_THM_SHD
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EN_VBUS_PRE_OV	6	VBUS_PRE_OV Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_VBUS_ILIM_UV	5	VBUS_ILIM_UV Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_VBUS_ILIM	4	VBUS_ILIM Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_VBUS_OV	3	VBUS_OV Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_VBUS_UV	2	VBUS_UV Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_VBUS_SHT_GND	1	VBUS_SHT_GND Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_THM_SHD	0	THM_SHD Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt

IRQ_MASK_2 (0x9)

A read-write register that configures which of the conditions in the IRQ_2 register will assert an Interrupt. See the IRQ_2 register for condition descriptions.

BIT	7	6	5	4	3	2	1	0
Field	–	–	EN_VBUS_ PREBIAS	–	EN_THM_ WARN	EN_IN_OV	EN_DATA_ OV	–
Reset	–	–	0b0	–	0b0	0b0	0b0	–
Access Type	–	–	Write, Read	–	Write, Read	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
EN_VBUS_P REBIAS	5	VBUS_PREBIAS Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_THM_W ARN	3	THM_WARN Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_IN_OV	2	IN_OV Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_DATA_O V	1	DATA_OV Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt

IRQ_0 (0xA)

A read-only register that includes flags which indicate a number of operating conditions. These flags can assert an interrupt by setting the corresponding bit in the MASK register.

IRQ_0 holds notifications of expected operations rather than error/fault conditions.

BIT	7	6	5	4	3	2	1	0
Field	UNCONFIG URED	–	CC_STATE _EV	CC_ATTAC H_IRQ	BC_ATTAC H_IRQ	CC_ATTAC H_EV	BC_ATTAC H_EV	ADC_DON E
Reset	0b0	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	–	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
UNCONFIGU RED	7	I^{2}C Unconfigured Indicator Bit	0 = Device is fully configured (CONFIGURED written to 1) 1 = Device is not fully configured (CONFIGURED has not been written to 1)
CC_STATE_ EV	5	Type-C State Change Indicator. Clear on read. Not affected by IRQ_AUTOCLR.	0 = No change in Type-C state since last read 1 = Type-C state has changed since last read
CC_ATTACH _IRQ	4	Type-C ATTACH Indicator. This bit indicates a Type-C device attach is observed on the CC pins. Applies to Attached.SRC states. Further attach details can be read in the STATUS registers.	0 = No Type-C device attached 1 = Type-C device attached
BC_ATTACH _IRQ	3	BC1.2 ATTACH Indicator. This bit indicates a BC1.2 device attach is observed on the HVDP/HVDM pins.	0 = No device attached 1 = Device attached

BITFIELD	BITS	DESCRIPTION	DECODE
CC_ATTACH_EV	2	Type-C ATTACH Event Detected. This bit indicates a Type-C device attach was initiated and/or terminated as observed on the CC pins. This bit differs from CC_ATTACH (which indicates the current Type-C attach status in real time) in that it is issued only when the status changes from unattached to attached or vice-versa. Clear on read. Not affected by IRQ_AUTOCLR.	0 = No attach or detach event detected since last read 1 = New attach and/or detach event detected
BC_ATTACH_EV	1	BC1.2 ATTACH Event Detected. This bit indicates a BC1.2 device attach was initiated and/or terminated as observed on the HVDP/HVDM pins.This bit differs from BC_ATTACH (which indicates the current BC1.2 attach status in real time) in that it is issued only when the status changes from unattached to attached or vice-versa. Clear on read. Not affected by IRQ_AUTOCLR.	0 = No attach or detach event detected since last read 1 = New attach and/or detach event detected
ADC_DONE	0	ADC Meaurement Complete Indicator. Clear on read.	0 = No new data available since last read 1 = New data available

IRQ_1 (0xB)

A read-only register that includes flags which indicate a number of error conditions. These flags can assert an interrupt by setting the corresponding bit in the MASK register.

BIT	7	6	5	4	3	2	1	0
Field	–	VBUS_PRE_OV	VBUS_ILIM_UV	VBUS_ILIM	VBUS_OV	VBUS_UV	VBUS_SHT_GND	THM_SHD
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_PRE_OV	6	V_{BUS} Pre-Overvoltage Fault Detected. Asserts if overvoltage exists on VBMON when Type-C is enabled and no Type-C device is attached. Clear on read if condition is resolved.	0 = No event 1 = Event detected
VBUS_ILIM_UV	5	V_{BUS} Current Limit and SENSN UV Fault Detected. Disabled when ILIM_ITRIP = 1. Clear on read if condition is resolved.	0 = No event 1 = Event detected
VBUS_ILIM	4	V_{BUS} Current-Limit Condition Detected. Disabled when ILIM_ITRIP = 0. Clear on read if condition is resolved.	0 = No event 1 = Event detected
VBUS_OV	3	V_{BUS} Overvoltage Fault Detected. Detected on SENSN pin. Clear on read if condition is resolved.	0 = No event 1 = Event detected

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_UV	2	V_{BUS} Under Voltage Fault Detected. Detected on SENSN pin. Clear on read if condition is resolved.	0 = No event 1 = Event detected
VBUS_SHT_GND	1	V_{BUS} Short to Ground Fault Detected. Detected on SENSN pin. Clear on read if condition is resolved.	0 = No event 1 = Event detected
THM_SHD	0	Overtemperature Fault Detected. Asserts when the die temperature exceeds 165°C (typ). Clear on read if condition is resolved.	0 = No event 1 = Event detected

IRQ_2 (0xC)

A read-only register that includes flags which indicate a number of error conditions. These flags can assert an interrupt by setting the corresponding bit in the MASK register.

BIT	7	6	5	4	3	2	1	0
Field	–	–	VBUS_PREBIAS	–	THM_WARN	IN_OV	DATA_OV	–
Reset	–	–	0b0	–	0b0	0b0	0b0	–
Access Type	–	–	Read Clears All	–	Read Clears All	Read Clears All	Read Clears All	–

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_PREBIAS	5	V_{BUS} Pre-Bias. Asserts if Type-C is enabled and VBMON > V_{SAFE0V} when no Type-C device is attached.	0 = No event 1 = Event detected
THM_WARN	3	Thermal Warning Condition Detected. Asserts when the temperature has reached 130°C (typ). If thermal foldback is enabled, the type-C current advertisement and current limit will be lowered while this bit is asserted. Clear on read if condition is resolved.	0 = No event 1 = Event detected
IN_OV	2	IN Pin Overvoltage Fault Detected. Clear on read if condition is resolved.	0 = No event 1 = Event detected
DATA_OV	1	DATA Pin Overvoltage Fault Detected. Clear on read if condition is resolved.	0 = No event 1 = Event detected

STATUS_0 (0xD)

A read-only register that includes information on the current status of the IC.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	CC_ATTACH	BC_ATTACH	VBMON_SAFE	–	VBUS_STAT
Reset	–	–	–	0b0	0b0	0b0	–	0b0
Access Type	–	–	–	Read Only	Read Only	Read Only	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
CC_ATTACH	4	Type-C ATTACH Status Indicator. This bit indicates the current Type-C attach status on the CC pins. More details can be read in the STATUS_1 register.	0 = No Type-C device currently attached 1 = Type-C device currently attached
BC_ATTACH	3	BC1.2 ATTACH Status Indicator. This bit indicates the current device attach status on the HVDP/HVDM pins. More details can be read in the STATUS_1 register.	0 = No device currently attached 1 = Device currently attached
VBMON_SAFE	2	VBMON (V_{BUS}) Safe Status Indicator. Determines if the DC-DC converter can be turned on after a Type-C attach. Only applicable with Type-C enabled.	0 = $V_{BUS} > V_{SAFE0V}$ 1 = $V_{BUS} < V_{SAFE0V}$
VBUS_STAT	0	Type-C V_{BUS} Status Indicator	0 – V_{BUS} not applied to receptacle 1 – V_{BUS} applied to receptacle (Attached.SRC)

STATUS_1 (0xE)

A read-only register that includes information on the current status of the IC.

BIT	7	6	5	4	3	2	1	0
Field	–	–	CC_PIN_STATE[1:0]		CC_STATE[3:0]			
Reset	–	–	0b00					
Access Type	–	–	Read Only		Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
CC_PIN_STATE	5:4	Type-C Active CC Pin/Orientation Indicator	0b00 = No Attach 0b01 = R_D detected on CC1 0b10 = R_D detected on CC2 0b11 = Not used
CC_STATE	3:0	Type-C Functional Status/State Indicator	0b0000 = Disabled 0b0010 = Error Recovery 0b0011 = Unattached.SRC 0b0110 = AttachWait.SRC 0b1000 = Attached.SRC (CC2) 0b1100 = Attached.SRC (CC1)

ADC_0 (0x10)

BIT	7	6	5	4	3	2	1	0
Field	ADC_USBI[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
ADC_USBI	7:0	USB Output Current ADC Measurement Result	I_{LOAD} = ((116mV/256) x ADC_USBI)/R_{SENSE} (amperes)

ADC_1 (0x11)

BIT	7	6	5	4	3	2	1	0
Field	ADC_USBV[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
ADC_USBV	7:0	USB Voltage ADC Measurement Result	V_{SENSP} = (19.8V/256) x ADC_USBV (volts), when VOUT[2:0] = 0b000

ADC_2 (0x12)

BIT	7	6	5	4	3	2	1	0
Field	ADC_TEMP[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
ADC_TEMP	7:0	Die Temp ADC Measurement Result	Die Temp = 3.5°C x ADC_TEMP - 270 (°C)

Applications Information

DC-DC Switching Frequency Selection

The switching frequency (f_{SW}) for MAX20459 is programmable through the CONFIG1 resistor (on standalone variants) or by I^2C register writes.

Higher switching frequencies allow for smaller PCB area designs with lower inductor values and less output capacitance. Consequently, peak currents and I^2R losses are lower at higher switching frequencies, but core losses, gate-charge currents, and switching losses increase.

To avoid AM-band interference, operation between 500kHz and 1.8MHz is not recommended.

DC-DC Input Capacitor Selection

The input capacitor supplies the instantaneous current needs of the buck converter and reduces the peak currents drawn from the upstream power source. The input bypass capacitor is a determining factor in the input voltage ripple.

The input capacitor RMS current rating requirement ($I_{IN(RMS)}$) is defined by the following equation:

$$I_{IN(RMS)} = I_{LOAD}\frac{\sqrt{V_{SENSP} \times \left(V_{SUPSW} - V_{SENSP}\right)}}{V_{SUPSW}}$$

$I_{IN(RMS)}$ has a maximum value when the input voltage equals twice the output voltage ($V_{SUPSW} = 2 \cdot V_{SENSP}$), so $I_{IN(MAX)} = \frac{1}{2} \cdot I_{LOAD(MAX)}$. I_{LOAD} is the measured operating load current, while $I_{LOAD(MAX)}$ refers to the maximum load current.

Choose an input capacitor that exhibits less than 10ºC self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input voltage ripple is composed of V_Q (caused by the capacitor discharge) and V_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple current capability at the input. Assume the contribution from the ESR and capacitor discharge is equal to 50%. Calculate the input capacitance and ESR required for a specified input voltage ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{LOAD(MAX)} + \frac{\Delta I_L}{2}}$$

where:

$$\Delta I_L = \frac{\left(V_{SUPSW} - V_{SENSP}\right) \times V_{SENSP}}{V_{SUPSW} \times f_{SW} \times L}$$

and:

$$C_{IN} = \frac{I_{LOAD(MAX)} \times D\left(1 - D\right)}{\Delta V_Q \times f_{SW}} \text{ where } D = \frac{V_{SENSP}}{V_{SUPSW}}$$

Where D is the buck converter duty cycle.

Bypass SUPSW with 0.1μF parallel to 10μF of ceramic capacitance close to the SUPSW and PGND pins. The ceramic input capacitor of a buck converter has a high $\frac{di}{dt}$, minimize the PCB current-loop area to reduce EMI. Bypass SUPSW with 47μF of bulk electrolytic capacitance to dampen line transients.

DC-DC Output Capacitor Selection

To ensure stability and compliance with the USB and Apple specifications, follow the recommended output filters listed in Table 10. For proper functionality, a minimum amount of ceramic capacitance must be used, regardless of f_{SW}. Additional capacitance for lower switching frequencies can be low-ESR electrolytic types (< 0.25Ω).

DC-DC Output Inductor Selection

Three key inductor parameters must be considered when selecting an inductor: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). To select the proper inductance value, the ratio of inductor peak-to-peak AC current to DC average current (LIR) must be selected. A small LIR will reduce the RMS current in the output capacitor and results in small output-ripple voltage, but this requires a larger inductor. A good compromise between size and loss is LIR = 0.35 (35%). Determine the inductor value using the equation below.

$$L = \frac{V_{SENSP} \times \left(V_{SUPSW} - V_{SENSP}\right)}{V_{SUPSW} \times f_{SW} \times I_{LOAD(MAX)} \times LIR}$$

where V_{SUPSW}, V_{SENSP}, and I_{OUT} are typical values (such that efficiency is optimum for nominal operating conditions). Ensure that the indutor I_{SAT} is above the buck converter's cycle-by-cycle peak current limit.

Table 10. Recommended Output Filters For I_{LOAD} of 3A

f_{SW} (kHz)	L_{OUT} (µH)	RECOMMENDED C_{OUT}
2200	1.5	22µF ceramic OR 10µF ceramic + low-ESR 22µF electrolytic (< 0.8Ω)
488	8.2	3 x 22µF ceramic OR 22µF ceramic + low-ESR 68µF electrolytic (< 0.25Ω)
310	12	22µF ceramic + low-ESR 68µF electrolytic (< 0.25Ω)

Layout Considerations

Proper PCB layout is critical for robust system performance. See the MAX20459 EV kit datasheet for a recommended layout. Minimize the current-loop area and the parasitics of the DC-DC conversion circuitry to reduce EMI. The input capacitor placement should be prioritized because in a buck converter, the ceramic input capacitor has high $\frac{di}{dt}$. Place the input capacitor as close as possible to the IC SUPSW and PGND pins. Shorter traces should be prioritized over wider traces.

A low-impedance ground connection between the input and output capacitor is required (route through the ground pour on the exposed pad). Connect the exposed pad to ground. Place multiple vias in the pad to connect to all other ground layers for proper heat dissipation (failure to do so may result in the IC repeatedly reaching thermal shutdown). Do not use separate power and analog ground planes; use a single common ground and manage currents through component placement. High-frequency return current flows through the path of least impedance (through the ground pour directly underneath the corresponding traces).

Determining USB System Requirements

In a Dedicated USB Charging Port (DCP) application, the user port is generally located in a front-facing configuration on the DCP or HUB module. To avoid V_{BUS} voltage drop at the user port when current increases due to trace, connector, and output ferrite resistance, MAX20459 implement voltage-adjustment circuitry that increases the buck's output-voltage regulation point linearly with the output current. The voltage-adjustment gain can be set using either external resistors or I^2C depending on the variant. The gain setting must be calculated to take into account all series element and voltage drops in the charging path, including ground return. See the USB Voltage Adjustment section for calculating the optimum gain setting for your application. User cable can be of different length and type, and therefore should not be included in the calculations.

USB Loads

MAX20459 is compatible with both USB-compliant and non-compliant loads. A compliant USB device is not allowed to sink more than 30mA and must not present more than 10µF of capacitance when initially attached to the port. The device then begins its HVD+/HVD- connection and enumeration process. After completion of the connect process, the device can pull 100mA/150mA and must not present a capacitance greater than 10μF. This is considered the hot-inserted, USB-compliant load of 44Ω in parallel with 10μF.

For non-compliant USB loads, the ICs can also support both a hot insertion and soft-start into a USB load of 2Ω in parallel with 330μF.

USB Output Current Limit

The USB load current is monitored by an internal current-sense amplifier through the voltage created across R_{SENSE}. MAX20459 offers an adjustable USB current-limit threshold. See SETUP_2 or Table 7 to select an appropriate register or resistor value for the desired current limit.

USB Voltage Adjustment

Figure 8 shows a DC model of the voltage-correction function of MAX20459. Without voltage adjustment (V_{ADJ} = 0, GAIN[4:0] = 0), the voltage seen by the device at the end of the cable will decrease linearly as load current increases. To compensate for this, the output voltage of the buck converter should increase linearly with load current. The slope of SENSP is called R_{COMP} such that $V_{ADJ} = R_{COMP} \cdot I_{LOAD}$ and $R_{COMP} = GAIN[4:0] \cdot R_{LSB} \cdot \frac{R_{SENSE}}{33m\Omega}$ (see Figure 9). The R_{COMP} adjustment values available on MAX20459 are listed in the GAIN[4:0] register description and are based on a 33mΩ sense resistor.

For $V_{DUT} = V_{NO\_LOAD}$; $0 \leq I_{LOAD}$, R_{COMP} must equal the sum of the system resistances. Calculate the minimum R_{COMP} for the system so that V_{DUT} stays constant:

$$R_{COMP\_SYS} = R_{LR} + R_{SENSE} + R_{PCB} + R_{CABLE\_VBUS} + R_{CABLE\_GND}$$

Where $R_{CABLE\_VBUS} + R_{CABLE\_GND}$ is the round-trip resistance of the USB cable (including the effect from the cable shield, if it conducts current), R_{LR} is the buck converter's load regulation expressed in mΩ (51mΩ typ.), and R_{PCB} is the resistance of any additional V_{BUS} parasitics (the V_{BUS} FET, PCB trace, ferrites, and the USB connectors). Find the setting for GAIN[4:0] using the minimum R_{COMP}.

$$\text{GAIN[4:0]} = ceiling\left(\frac{R_{COMP\_SYS}}{R_{LSB}} \cdot \frac{33m\Omega}{R_{SENSE}}\right)$$

The nominal DUT voltage can then be estimated at any load current by:

$$V_{DUT} = V_{NO\_LOAD} + R_{LSB} \cdot GAIN[4:0] \cdot \frac{R_{SENSE}}{33m\Omega} \cdot I_{LOAD} - R_{COMP\_SYS} \cdot I_{LOAD}$$

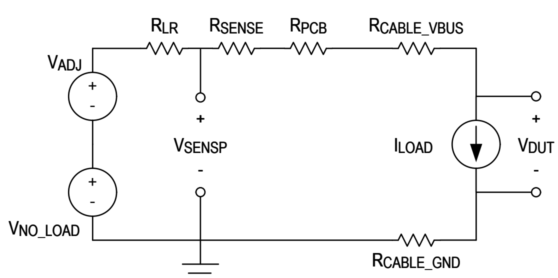


Figure 8. DC Voltage Adjustment Model

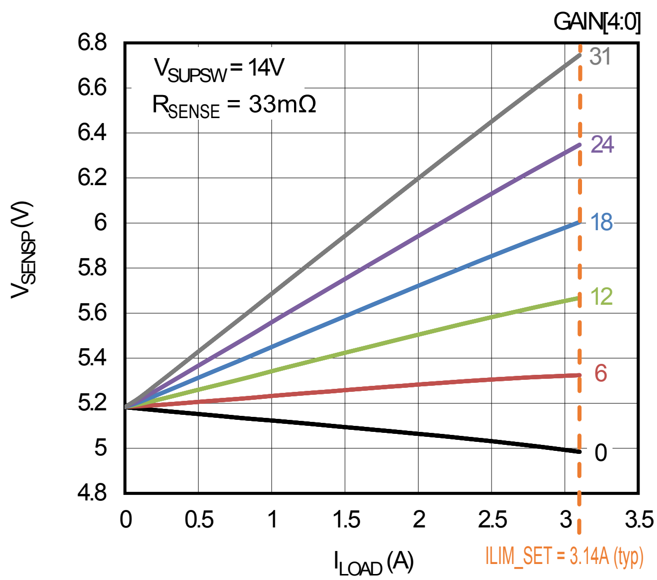


Figure 9. Increase in SENSP vs. USB Current

Selecting a Current-Sense Resistor

The external current-sense resistor (R_{SENSE}) is critical for accurate current-limit, voltage-adjustment, attach-detection, and ADC measurement. Select a resistor with high precision and low temperature variation (ppm). It is highly recommended that designs use a resistor with an exact value of 33mΩ. Since the current limit and voltage adjustment are selected digitally (there are a discrete number of levels), changing this value also changes the possible current-limit thresholds, the voltage-adjustment compensation and the attach threshold. The specifications in the register and resistor tables will need to be scaled accordingly.

Some systems require the need to supply up to 160% of $I_{LOAD(MAX)}$ for brief periods. It is possible to increase the MAX20459 current limit beyond 3.04A (min) by decreasing R_{SENSE} using this scaling factor:

$$R_{SENSE} = 33m\Omega \cdot \frac{3.04A}{1.6 \cdot I_{LOAD(MAX)}}.$$

Example CONFIG Resistor Selection

With R_{PCB} = 20mΩ, R_{SENSE} = 33mΩ, and R_{LR} = 51mΩ, the total system resistance is R_{COMP_SYS} = 20 + 33 + 51 = 104mΩ. The desired GAIN[4:0] register setting is then ceiling(104/18) = 6 = 0b00110, which sets the adjustment level to 108mΩ. To set GAIN[4:0] using the CONFIG resistors, the appropriate step must be selected for both CONFIG2 and CONFIG3. The MSB of the GAIN register (GAIN[4]) is selected by CONFIG3. In this example, GAIN[4] = 0b0. If it is a 3A application with automatic thermal foldback, then CONFIG3 should be set to Step 3, which is set with a 1370Ω resistor on the CONFIG3 pin.

From the previous calculation, GAIN[3:0] = 0b0110. This corresponds to Step 6 and a CONFIG2 resistor of 3090Ω. CONFIG1 sets the remaining parameters. For example, to run the buck using the internal clock switching at 488kHz with spread spectrum enabled, CONFIG1 should be set to Step 1 (619Ω).

USB Type-C Certification

Industry specifications at times make changes. If a change prevents the use of non-BC 1.2 protocols, this application change should be considered. Consider using a 0Ω resistor between USB Type-C D+/- and open MAX20459 HVD+/-.

ESD Protection

The high-voltage MAX20459 requires no external ESD protection. All Maxim devices incorporate ESD protection structures to protect against electrostatic discharges encountered during handling and assembly. While competing solutions can latch-up and require the power to be cycled after an ESD event, the MAX20459 continues to work without latch-up. When used with the configuration shown in the Typical Application Circuit, the MAX20459 is characterized for protection to the following limits:

- ±15kV ISO 10605 (330pF, 330Ω) Air Gap
- ±15kV ISO 10605 (330pF, 2kΩ) Air Gap
- ±8kV ISO 10605 (330pF, 330Ω) Contact
- ±8kV ISO 10605 (330pF, 2kΩ) Contact
- ±15kV IEC 61000-4-2 (150pF, 330Ω) Air Gap
- ±8kV IEC 61000-4-2 (150pF, 330Ω) Contact

Note: All application-level ESD testing is performed on the standard evaluation kit.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for test setup, test methodology, and test results.

Human Body Model

Figure 10 shows the Human Body Model, and Figure 12 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. MAX20459 helps users design equipment that meets Level 4 of IEC 61000-4-2. The main difference between tests done using the Human Body Model and IEC 61000-4-2 is a higher peak current in IEC 61000-4-2. Because the series resistance is lower in the IEC 61000-4-2 ESD test model Figure 11, the ESD withstand-voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 13 shows the current waveform for the 8kV, IEC 61000-4-2 Level 4 ESD Contact Discharge test. The Air Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

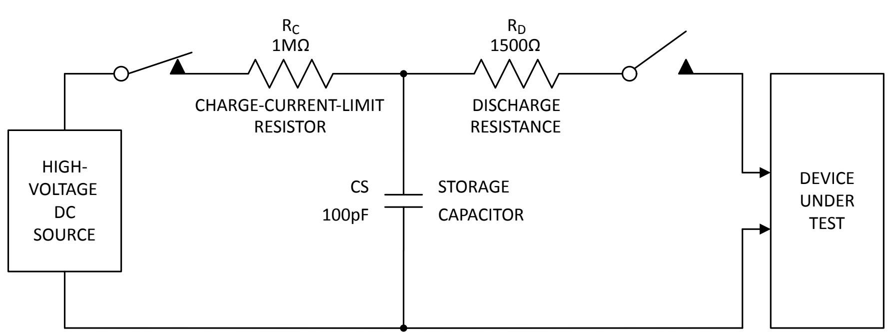


Figure 10. Human Body ESD Test Model

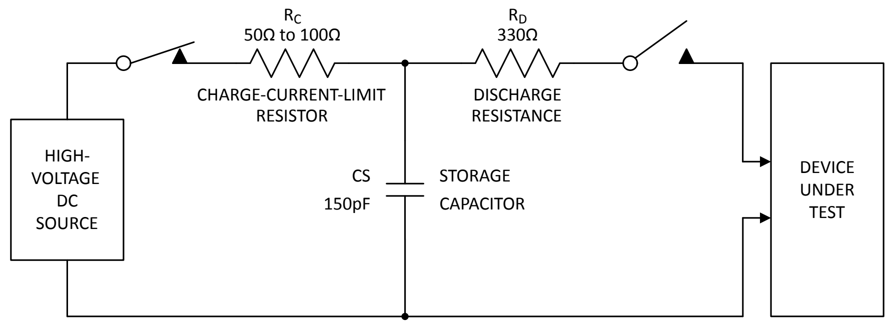


Figure 11. IEC 61000-4-2 ESD Test Model

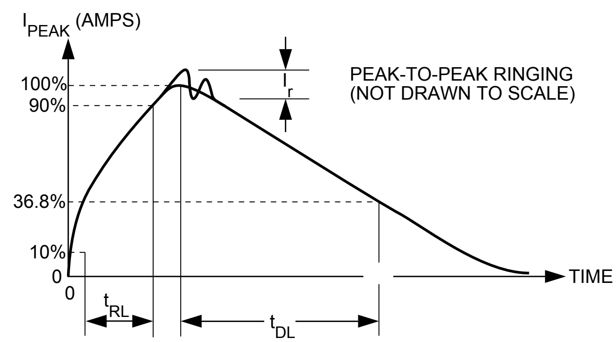


Figure 12. Human Body Current Waveform

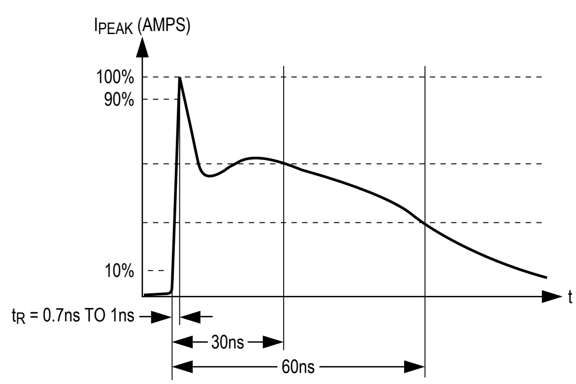
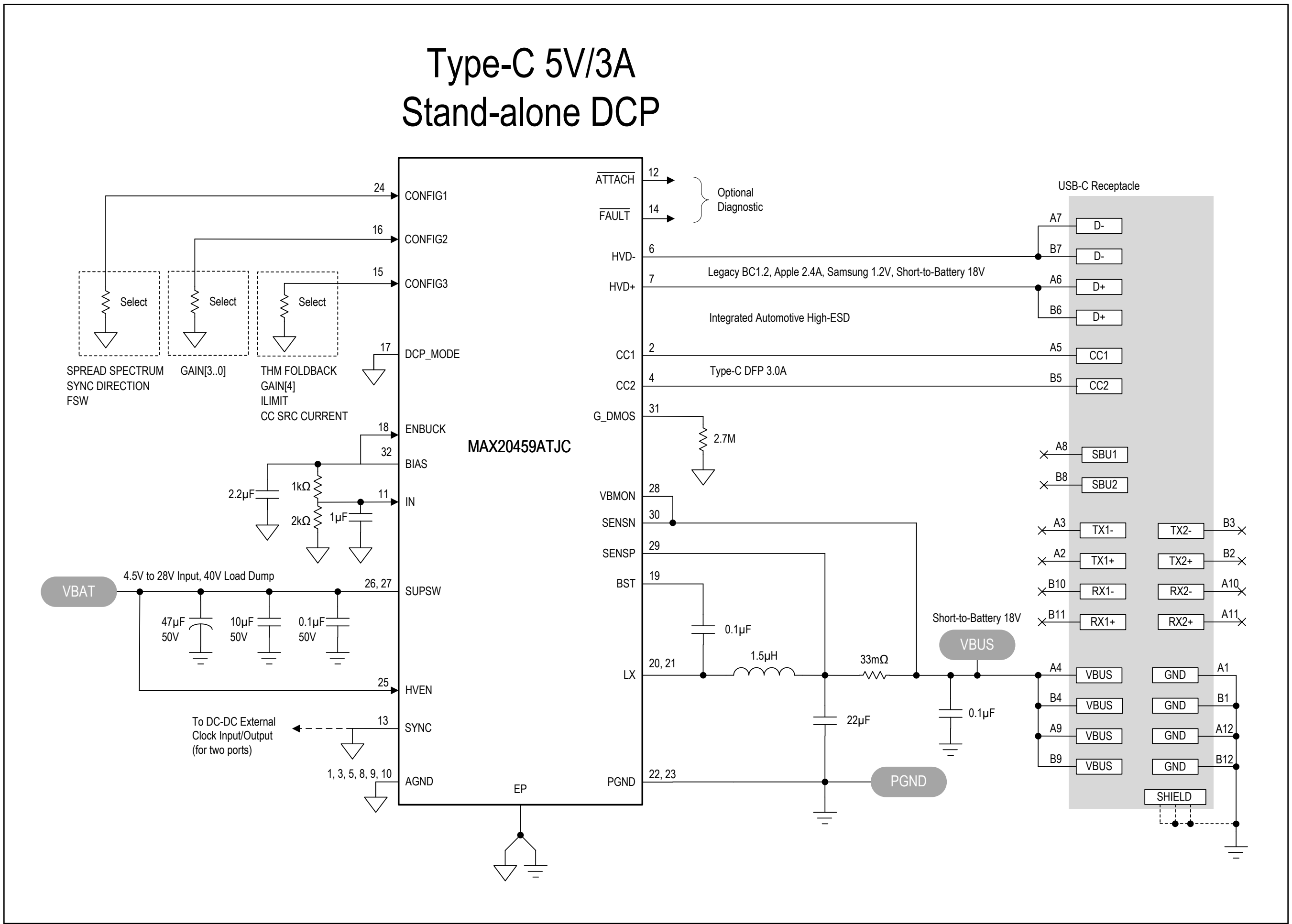


Figure 13. IEC 61000-4-2 Current Waveform

Typical Application Circuits



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	I^2C
MAX20459ATJA/V+	-40°C to +125°C	32 TQFN-EP*	Yes
MAX20459ATJC/V+	-40°C to +125°C	32 TQFN-EP*	No

/V Denotes Automotive Qualified Parts

+ Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/19	Initial release	—
1	6/20	Updated *Benefits and Features, Thermal Resistance*, *Absolute Maximum Ratings*, *Package Information*, *Electrical Characteristics*, ToCs 16, 18-19, 21-22, *SCL(Config3) Pin* Description, *ENBUCK Reset Behavior and Timing Diagram, Attach Logic Diagram, CC Attachment and VBUS Discharge*, *Maximum Duty-Cycle Operation, Switching Frequency Synchronization (SYNC Pin)*, *Spread-Spectrum Option*, *Voltage Feedback Adjustment Configuration*, *Remote-Sense Feedback Adjustment (SHIELD Pin)*, Table 8, *SETUP_0 (0x0)*, *SETUP_3 (0x3)*, *IRQ_2 (0xC)*.	1, 8-9, 11, 15-16, 18-19, 21, 26-29, 37, 40, 42, 47
2	1/21	Updated USB Type-C functionality to meet latest specifications (search for t_{DIS_DET}). Improved SYNC pin logic for multi-port applications (search for SYNC). Expanded design methods for overcurrent flexibility (search for $I_{LOAD(MAX)}$).	1 - 57