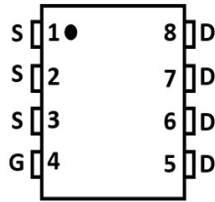
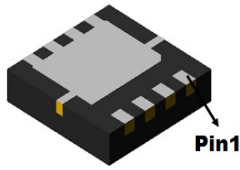
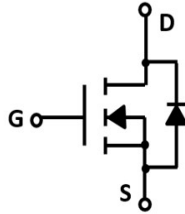


## N-Channel Enhancement Mode Field Effect Transistor



**DFN3.3X3.3**



### Product Summary

- $V_{DS}$  30 V
- $I_D$  60 A
- $R_{DS(ON)}$ ( at  $V_{GS}=10V$ ) < 2.5 mohm
- $R_{DS(ON)}$ ( at  $V_{GS}=4.5V$ ) < 3.8 mohm
- 100% UIS Tested
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$

### Applications

- DC-DC Converters
- Power management functions
- Backlighting

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	30	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_C=25^\circ\text{C}$	$I_D$	60	A
	$T_C=100^\circ\text{C}$		38	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	240	A
Total Power Dissipation @ $T_C=25^\circ\text{C}$ <sup>B</sup>		$P_D$	75	W
Total Power Dissipation @ $T_C=100^\circ\text{C}$ <sup>B</sup>		$P_D$	30	W
Total Power Dissipation @ $T_A=25^\circ\text{C}$ <sup>C</sup>		$P_D$	6.2	W
Single Pulse Avalanche Energy <sup>D</sup>		$E_{AS}$	400	mJ
Thermal Resistance Junction-to-Case		$R_{\theta JC}$	1.67	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-Ambient		$R_{\theta JA}$	20	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ60N03A	F1	Q60N03A	5000	10000	100000	13" reel



# YJQ60N03A

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> =20A		2.0	2.5	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> =20A		3.0	3.8	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V		0.85	1.2	V
Gate resistance	R <sub>g</sub>	F=1 MHz, Open drain		2.9		Ω
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHZ		4498		pF
Output Capacitance	C <sub>oss</sub>			800		
Reverse Transfer Capacitance	C <sub>rss</sub>			643		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub> (10V)	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =20A		92.7		nC
Total Gate Charge	Q <sub>g</sub> (4.5V)			46		
Gate-Source Charge	Q <sub>gs</sub>			13.5		
Gate-Drain Charge	Q <sub>gd</sub>			22.8		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =20A, di/dt=500A/us		3.0		
Reverse Recovery Time	t <sub>rr</sub>			15		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =20V, I <sub>D</sub> =4A, R <sub>L</sub> =0.75Ω R <sub>GEN</sub> =3Ω		11		ns
Turn-on Rise Time	t <sub>r</sub>			80		
Turn-off Delay Time	t <sub>D(off)</sub>			39		
Turn-off fall Time	t <sub>f</sub>			92		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. The value of R<sub>θJA</sub> is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C.

D. T<sub>J</sub>=25°C, V<sub>DD</sub>=20V, V<sub>G</sub>=10V, L=2.0mH, R<sub>g</sub>=25Ω.



## ■ Typical Performance Characteristics

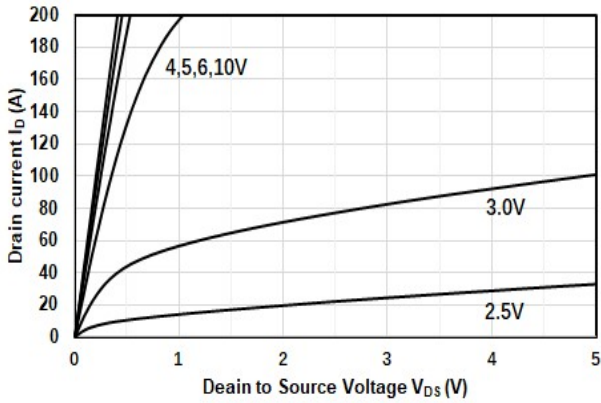


Figure1. Output Characteristics

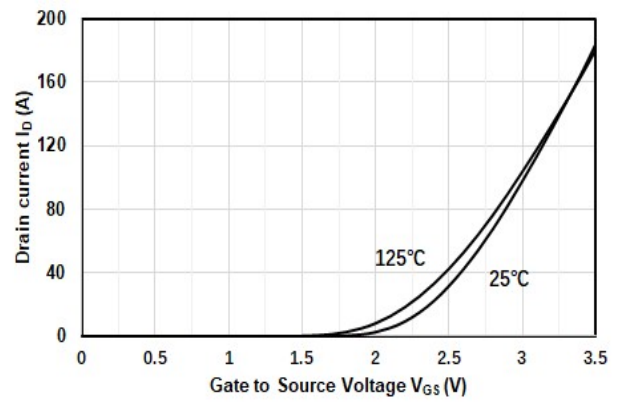


Figure2. Transfer Characteristics

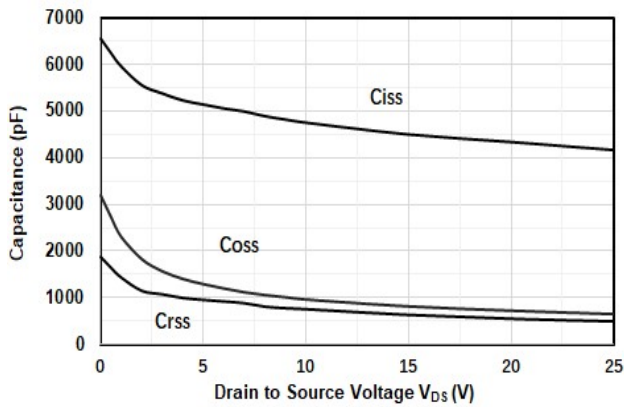


Figure3. Capacitance Characteristics

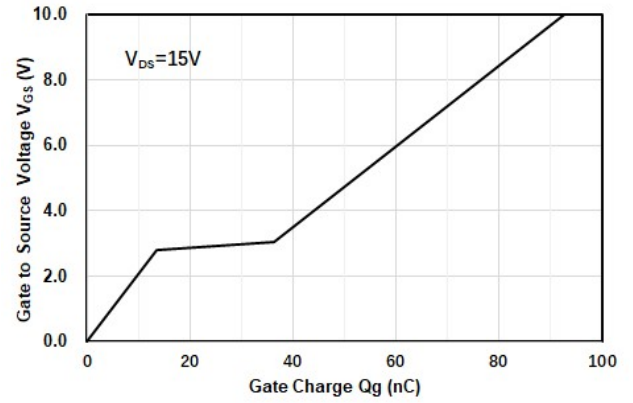


Figure4. Gate Charge

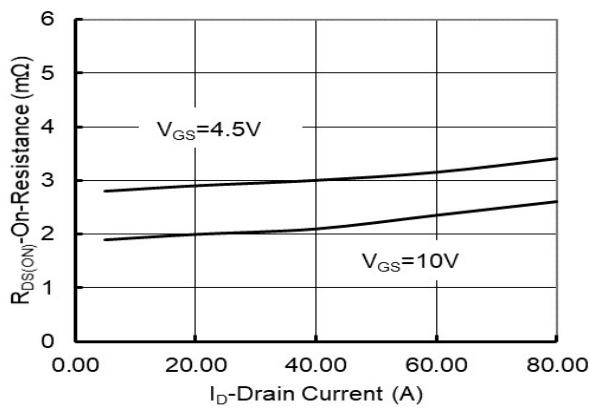


Figure5. Drain-Source on Resistance

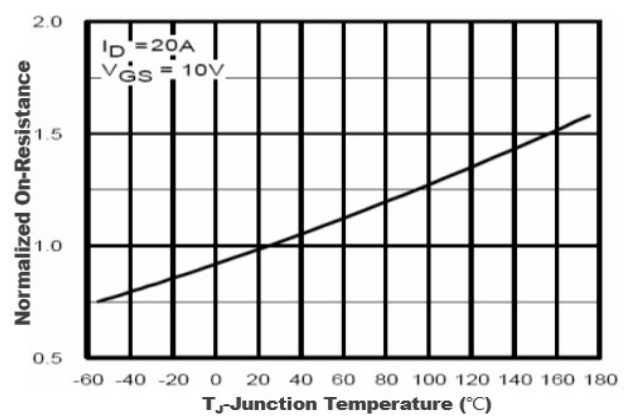


Figure6. Drain-Source on Resistance



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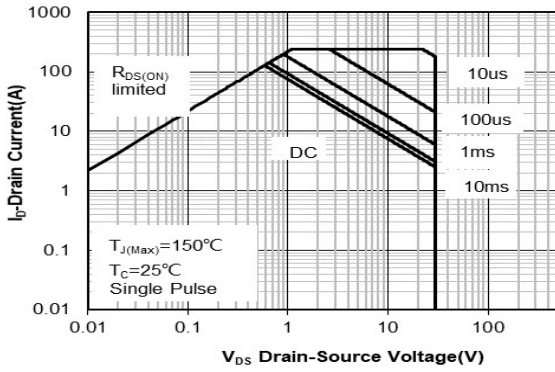


Figure7. Safe Operation Area

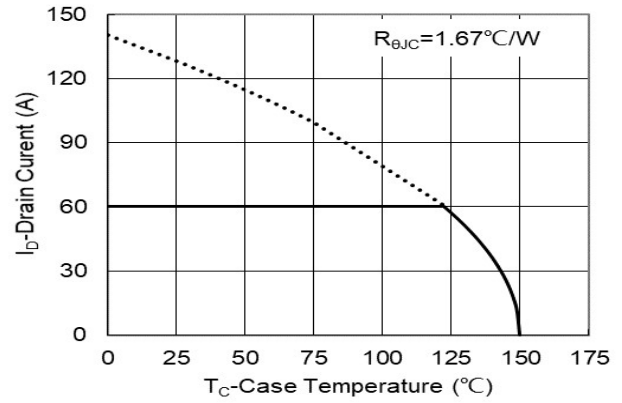


Figure8. Drain current vs. Case Temperature

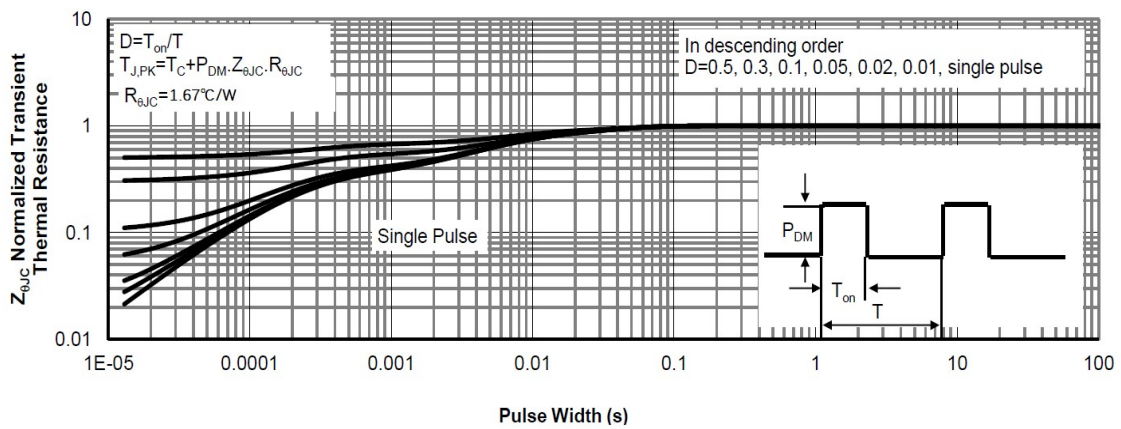
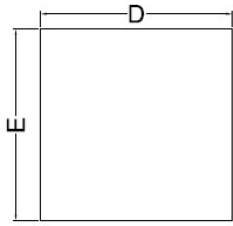


Figure9. Normalized Maximum Transient Thermal Impedance

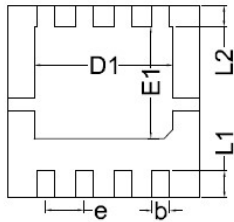


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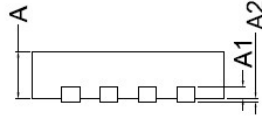
## ■ DFN3.3X3.3 Package information



Top View  
正面视图

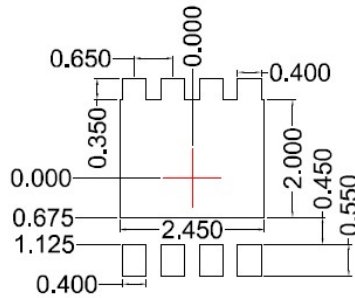


Bottom View  
背面视图



Side View  
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



Suggested Solder Pad Layout  
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10\text{mm}$ .
3. The pad layout is for reference purposes only.



# YJQ60N03A

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