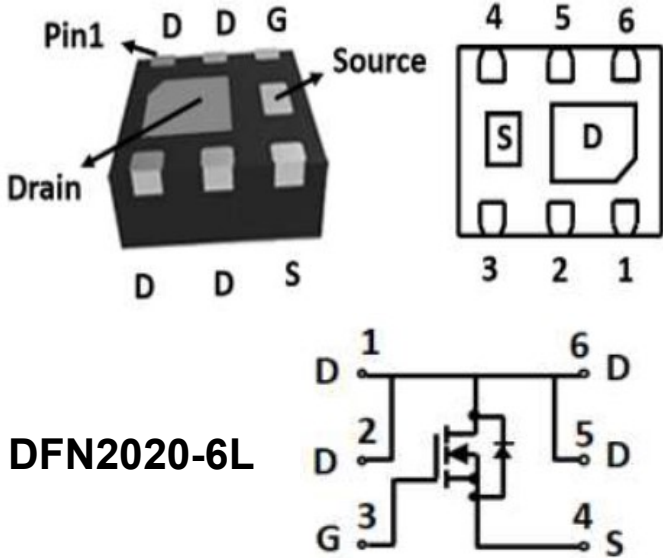


N-Channel Enhancement Mode Field Effect Transistor



DFN2020-6L

Product Summary

- V_{DS} 20V
- I_D 13A
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) < 9mohm
- $R_{DS(ON)}$ (at $V_{GS}=2.5V$) < 12mohm
- $R_{DS(ON)}$ (at $V_{GS}=1.8V$) < 18.5mohm
- 100% ∇V_{DS} Tested

General Description

- Trench Power LV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching

Applications

- Battery protection
- Load switch
- Power management

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	20	V
Gate-source Voltage		V_{GS}	± 10	V
Drain Current	$T_A=25^\circ C$	I_D	13	A
	$T_A=70^\circ C$		8	
Pulsed Drain Current ^A		I_{DM}	32	A
Total Power Dissipation	$T_A=25^\circ C$	P_D	2.2	W
	$T_A=70^\circ C$		1.4	
Thermal Resistance Junction-to-Ambient ^B		$R_{\theta JA}$	57	$^\circ C/W$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ C$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ10N02A	F1	Q10N02	3000	30000	120000	7" reel



YJQ10N02A

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =20V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±10V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	0.45	0.62	1.0	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =4.5V, I _D =13A		7.8	9	mΩ
		V _{GS} =2.5V, I _D =6.5A		9.5	12	
		V _{GS} =1.8V, I _D =4A		12	18.5	
Diode Forward Voltage	V _{SD}	I _S =13A, V _{GS} =0V			1.2	V
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =10V, V _{GS} =0V, f=1MHZ		888		pF
Output Capacitance	C _{oss}			133		
Reverse Transfer Capacitance	C _{rss}			117		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =4.5V, V _{DS} =10V, I _D =6.8A		11.05		nC
Gate-Source Charge	Q _{gs}			1.73		
Gate-Drain Charge	Q _{gd}			3.1		
Turn-on Delay Time	t _{D(on)}	V _{GS} =4.5V, V _{DS} =10V, I _D =6.8A R _{GEN} =3Ω		7		ns
Turn-on Rise Time	t _r			46		
Turn-off Delay Time	t _{D(off)}			30		
Turn-off fall Time	t _f			52		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

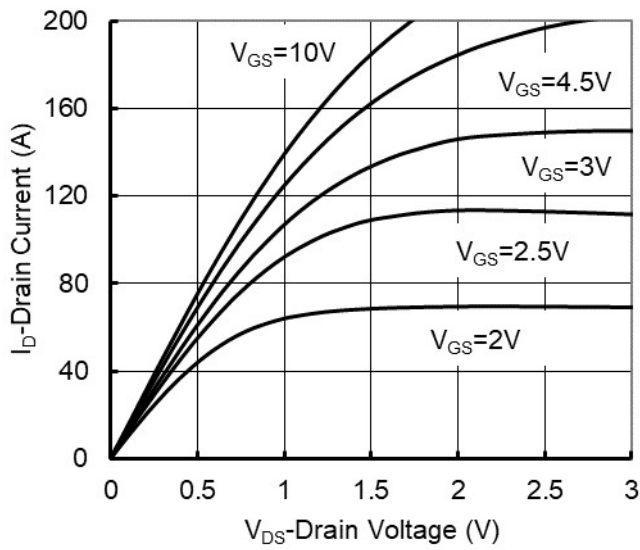


Figure1. Output Characteristics

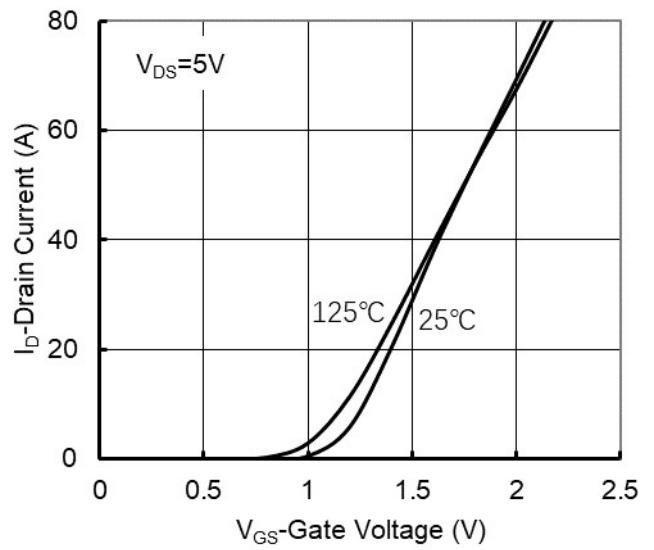


Figure2. Transfer Characteristics

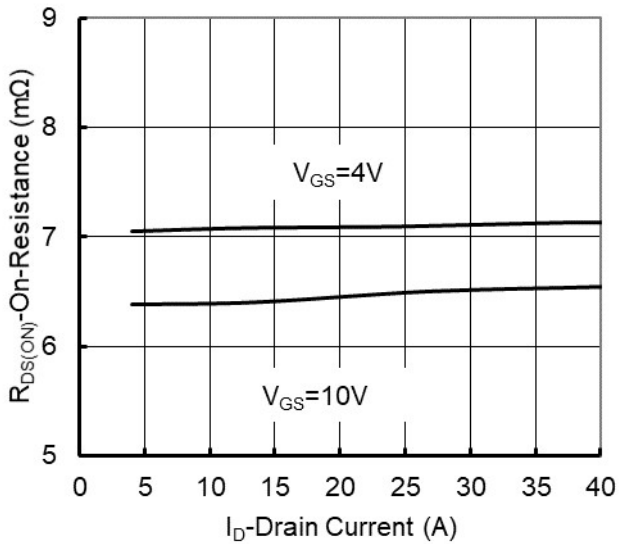


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

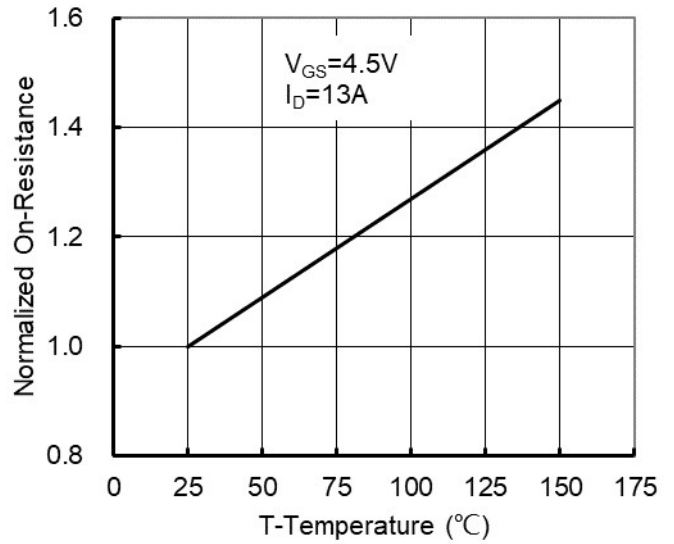


Figure 4: On-Resistance vs. Junction Temperature

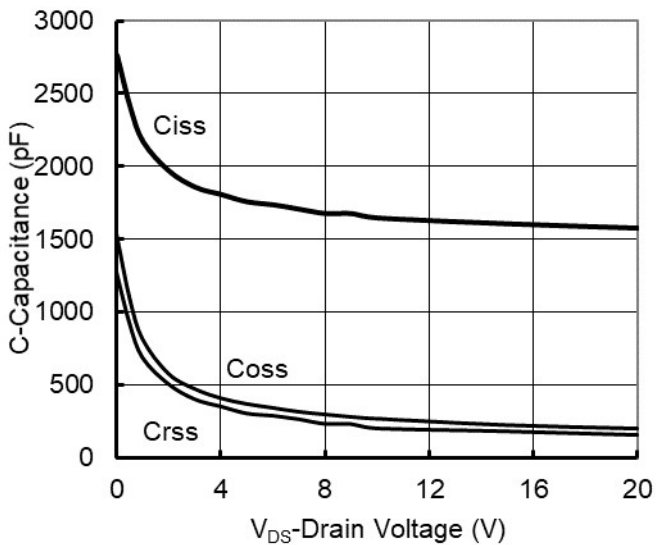


Figure5. Capacitance Characteristics

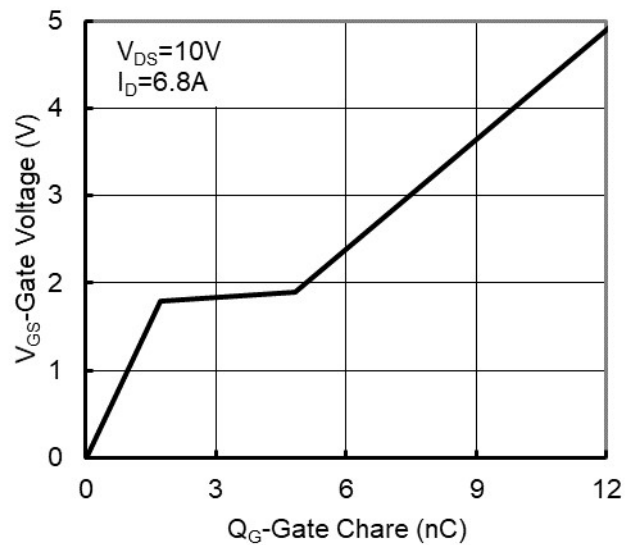


Figure6. Gate Charge



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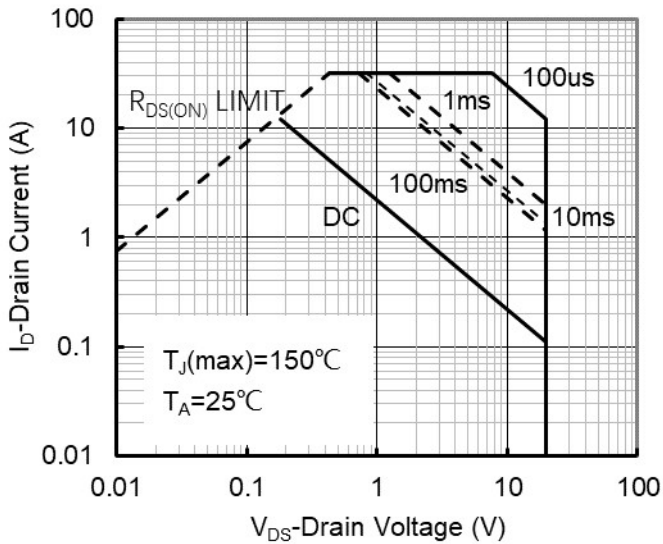


Figure7. Safe Operation Area

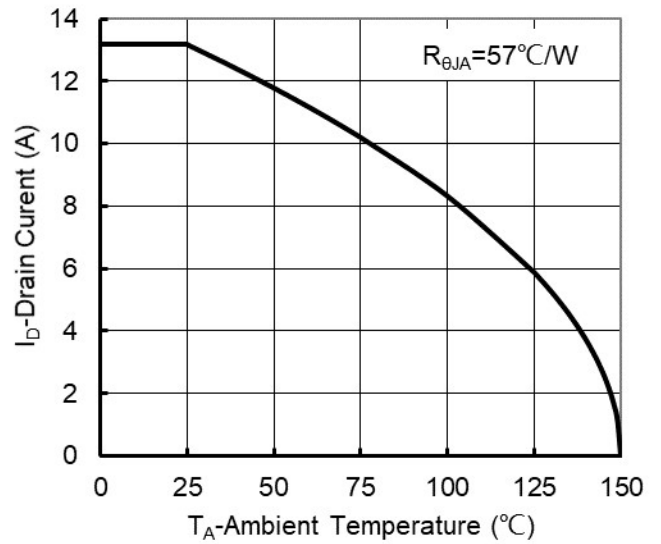


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

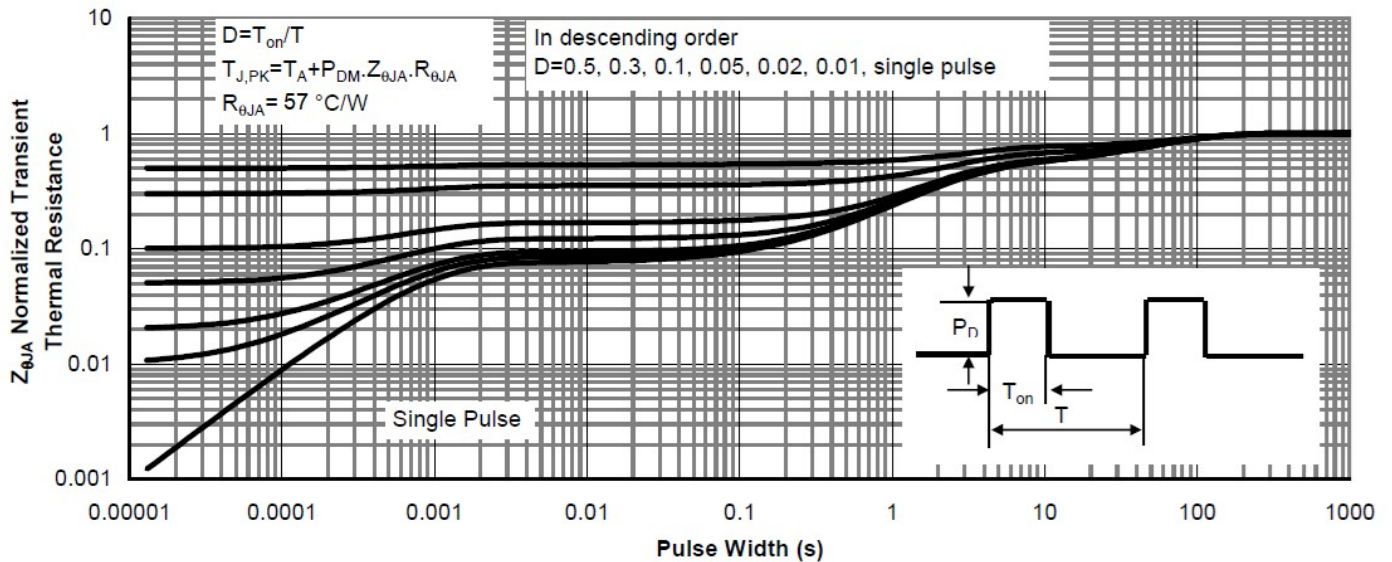


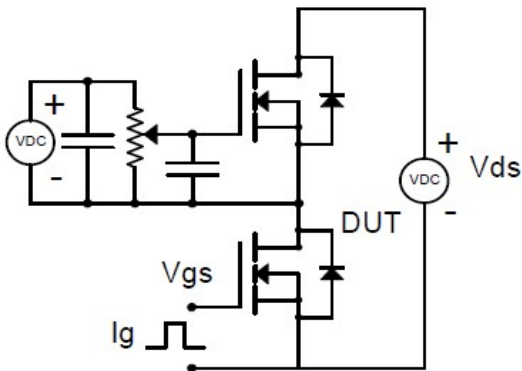
Figure9. Normalized Maximum Transient Thermal Impedance



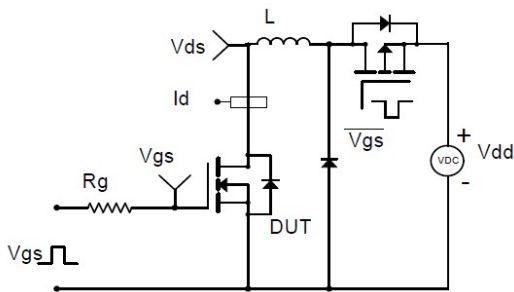
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform

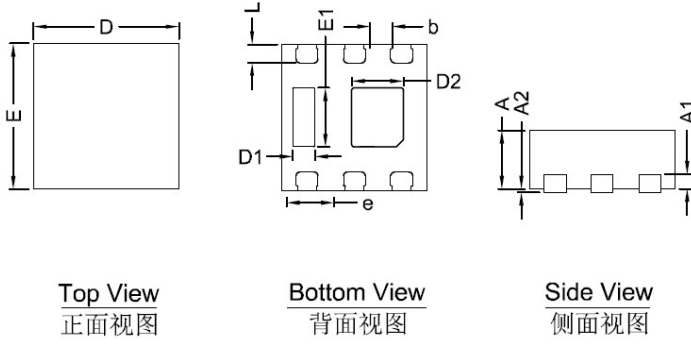


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

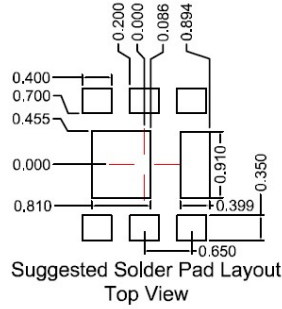


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DFN2020-6L Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	1.90	2.00	2.10
E	1.90	2.00	2.10
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	0.20	0.30	0.40
D2	0.61	0.71	0.81
E1	0.71	0.81	0.91
L	0.15	0.25	0.35
b	0.20	0.30	0.40
e	0.65 BSC		



- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: ± 0.10 mm.
 3. The pad layout is for reference purposes only.



YJQ10N02A

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