# NCV890430

# Synchronous Regulator – Automotive, Step-Down, 100% Duty Cycle

## 0.6 A, 2 MHz

The NCV890430 is a fixed-frequency Synchronous Buck regulator intended for Automotive, battery-connected applications that operate with up to a 45 V input supply. It is suitable for automotive systems requiring low noise and low shutdown currents that also need to operate at low input voltage close to the output voltage. A reset pin (with adjustable delay) simplifies interfacing with a microcontroller. This part also features an enable input that can either be connected to a low voltage (such as a micro-controller output) or high voltage (such as the battery input), and a synchronization input.

The NCV890430 also provides several protection features expected in automotive power supply systems such as current limit, short circuit protection, and thermal shutdown. In addition, the high switching frequency produces low output voltage ripple even when using small inductor values and all-ceramic input output filter capacitors – forming a space-efficient switching regulator solution.

### Features

- Internal 550 mΩ P-channel and 300 mΩ N-channel Power Switches
- Capable of 100% Duty Cycle Operation
- $V_{IN}$ Operating Range 3.5 V to 37 V
- Withstands Load Dump to 45 V
- 2 MHz Free-running Switching Frequency
- Low Shutdown Current < 10 μA
- High Voltage Enable Pin
- Synchronization Input Pin
- Maximum DC Output Current of at Least 0.6 A
- Fixed Output Voltage (5 V, 3.3 V, 2.5 V Versions)
- ±2% Output Voltage Accuracy
- DFN Package with Wettable Flanks (Pin Edge Plating per JEDEC MO220)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

### Typical Applications

- Automotive Infotainment and Instrumentation
- Automotive Body Applications
- Linear Regulator Replacement
- Rear View Camera

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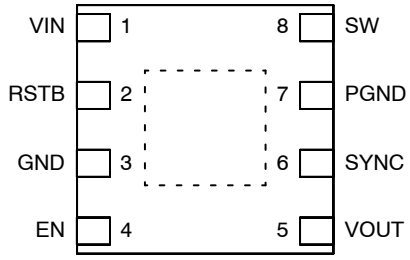
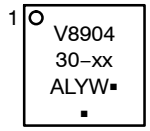
**DFN8, 3x3, 0.65P**
**CASE 506CS**

### PIN CONNECTIONS




(DFN8 Top View)

### MARKING DIAGRAM




V890430−xx = Specific Device Code
xx = 25, 33 or 50
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 9 of this data sheet.

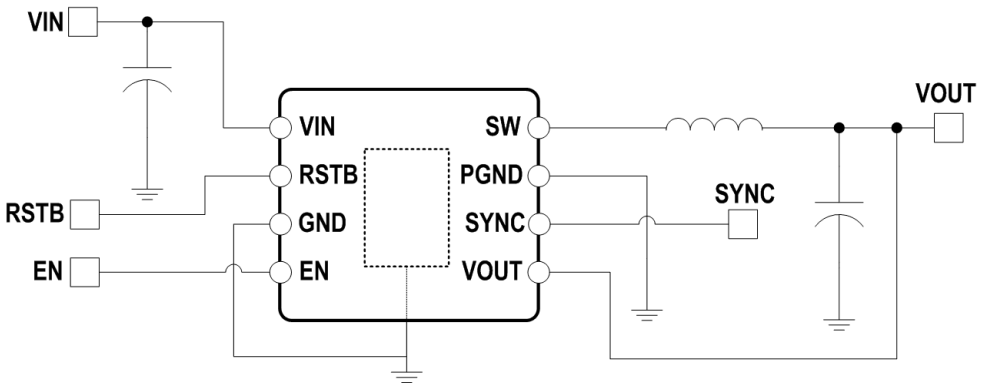



**Figure 1. Typical Application Schematic**

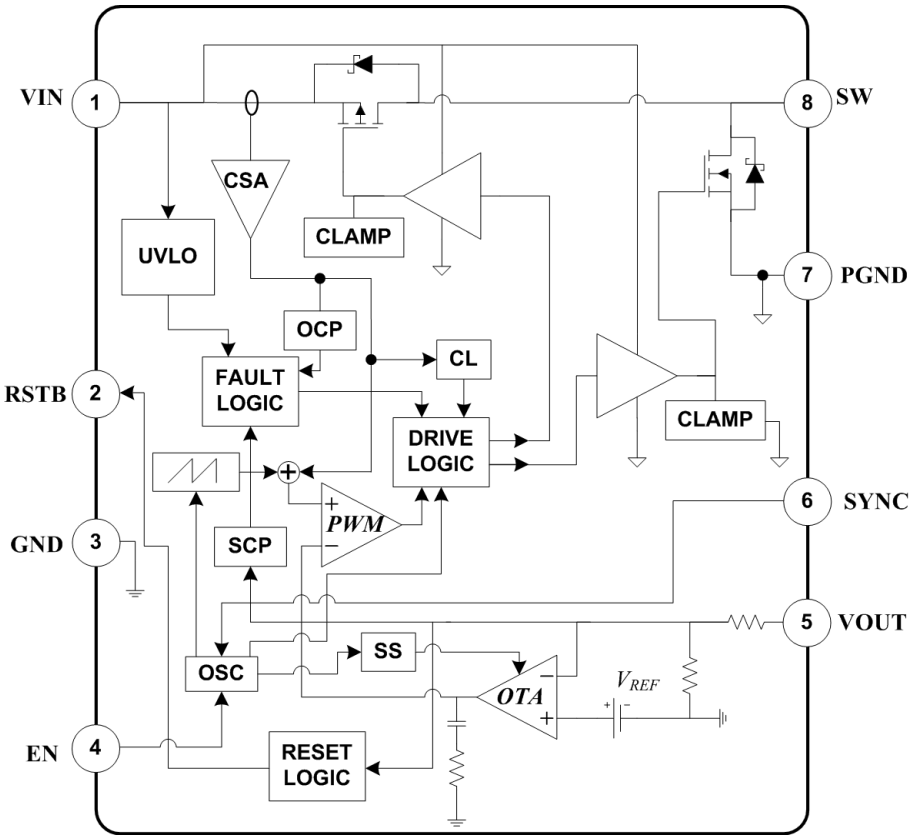



**Figure 2. Simplified Block Diagram**

**Table 1. PIN FUNCTION DESCRIPTIONS**

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | VIN | Input voltage from battery. Place an input filter capacitor in close proximity to this pin. |
| 2 | RSTB | Reset reporting flag. Open drain output, pulling down to ground when the output voltage is out of regulation. The value of the external pull-up resistor determines the delay time that the Reset is held low. |
| 3 | GND | Analog ground reference − should be connected directly to the output capacitor ground and the exposed pad. |
| 4 | EN | Enable input. Connecting a “high” voltage (TTL compatible, battery voltage tolerant) to this pin turns on the regulator. A low voltage forces the part into a very low Iq shutdown mode. |
| 5 | VOUT | Output voltage sensing for regulation. |
| 6 | SYNC | Synchronization input. Connecting an external clock to this pin synchronizes switching to the rising edge of the SYNC signal. |
| 7 | PGND | Power ground, connect directly to the input capacitor ground and to the exposed pad. |
| 8 | SW | Switching node of the Regulator. Connect the output inductor to this pin. |
| Exposed Pad | EPAD | Must be connected to GND (pin 3, electrical ground) and to a low thermal resistance path to the ambient temperature environment. |

**Table 2. ABSOLUTE MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Min/Max Voltage VIN | | −0.3 to 45 | V |
| Max Voltage VIN to SW | | 45 | V |
| Min/Max Voltage SW | | −0.7 to 40 | V |
| Min Voltage SW − 20 ns | | −3.0 | V |
| Min/Max Voltage EN | | −0.3 to 40 | V |
| Min/Max Voltage on SYNC, RSTB | | −0.3 to 6 | V |
| Min/Max Voltage VOUT | | −0.3 to 18 | V |
| Thermal Resistance, DFN8 Junction-to-Ambient (Note 1) | $R_{\theta JA}$ | 40 | °C/W |
| Storage Temperature Range | | −55 to +150 | °C |
| Operating Junction Temperature Range | $T_J$ | −40 to +150 | °C |
| ESD withstand Voltage (Human Body Model) | $V_{ESD}$ | 2.0 | kV |
| Moisture Sensitivity | MSL | Level 1 | |
| Peak Reflow Soldering Temperature (Note 1) | | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted on 1 sq. in. of a 4-layer PCB with 1 oz. copper thickness.

**Table 3. ELECTRICAL CHARACTERISTICS**

($V_{IN}$ = 4.5 V to 28 V, EN = 5 V. Min/Max values are valid for the temperature range −40°C ≤ $T_J$ ≤ 150°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **QUIESCENT CURRENT** | | | | | | |
| Quiescent Current, Enabled | $V_{IN}$ = 13.2 V, no switching | $I_{qEN}$ | | 2.0 | 3.0 | mA |
| Quiescent Current, Shutdown | $V_{IN}$ = 13.2 V, $V_{EN}$ = 0 V, $T_J$ = 25 °C | $I_{qSD}$ | | 5.0 | 8.0 | μA |
| **UNDERVOLTAGE LOCKOUT – VIN** | | | | | | |
| UVLO Start Threshold | $V_{IN}$ Rising | $V_{UVLSTT}$ | 4.1 | | 4.5 | V |
| UVLO Stop Threshold | $V_{IN}$ Falling | $V_{UVLSTP}$ | 3.2 | | 3.5 | V |
| **SOFT-START** | | | | | | |
| Soft-Start Completion Time | | $t_{SS}$ | 0.8 | 1.4 | 2.0 | ms |
| **OUTPUT VOLTAGE** | | | | | | |
| Output Voltage during Regulation | 100 μA < $I_{OUT}$ < 0.6 A<br>5.0 V Option<br>3.3 V Option<br>2.5 V Option | $V_{OUTreg}$ | <br>4.9<br>3.234<br>2.45 | <br>5.0<br>3.3<br>2.5 | <br>5.1<br>3.366<br>2.55 | V |
| **OSCILLATOR** | | | | | | |
| Frequency | 4.5 V < $V_{IN}$ < 18 V<br>20 V < $V_{IN}$ < 28 V | $f_{SW}$<br>$f_{SW(HV)}$ | 1.8<br>0.9 | 2.0<br>1.0 | 2.2<br>1.1 | MHz |
| **VBAT OVERVOLTAGE SHUTDOWN MONITOR** | | | | | | |
| Overvoltage Stop Threshold | | $V_{OV1SP}$ | 37 | | 40 | V |
| Overvoltage Start Threshold | | $V_{OV1ST}$ | 34.5 | | | V |
| Overvoltage Hysteresis | | $V_{OV1HY}$ | 0.9 | 1.7 | 2.5 | V |
| **VIN FREQUENCY FOLDBACK MONITOR** | | | | | | |
| Frequency Foldback Threshold | $V_{IN}$ Rising<br>$V_{IN}$ Falling | $V_{FLDUP}$<br>$V_{FLDDN}$ | 18.4<br>18 | | 20<br>19.8 | V |
| Frequency Foldback Hysteresis | | $V_{FLDHY}$ | 0.2 | 0.3 | 0.4 | V |
| **PEAK CURRENT LIMIT** | | | | | | |
| Current Limit Threshold | | $I_{LIM}$ | 1.5 | 1.7 | 1.9 | A |
| Low-Side Current Limit Threshold | $V_{SW}$ = 13.2 V | $I_{LIMLS}$ | 1.5 | 2.1 | 2.7 | A |
| **POWER SWITCHES** | | | | | | |
| High-Side Switch ON Resistance | | $R_{DSON-HS}$ | | 550 | 1000 | mΩ |
| Low-Side Switch ON Resistance | | $R_{DSON-LS}$ | | 300 | 550 | mΩ |
| Leakage Current $V_{IN}$ to SW | EN = 0 V, $V_{SW}$ = 0 | $I_{LKSWH}$ | | | 10 | μA |
| Leakage Current SW to GND | EN = 0 V, $V_{SW}$ = $V_{IN}$ | $I_{LKSWL}$ | | | 10 | μA |
| Minimum ON Time | Measured at SW Pin 2.5 V Option<br>3.3 V & 5.0 V Options | $t_{ONMIN}$ | 35<br>45 | | 55<br>70 | ns |
| Minimum OFF Time when Not 100% Duty Cycle | Measured at SW Pin at $f_{SW}$ = 2 MHz | $t_{OFFMIN}$ | | 30 | 50 | ns |
| Non-Overlap Time | | $t_{NOVLP}$ | | 10 | | ns |
| **SLOPE COMPENSATION** | | | | | | |
| Ramp Slope (Note 2)<br>(With Respect to Switch Current) | 4.5 V < $V_{IN}$ < 18 V<br>20 V < $V_{IN}$ < 28 V | $S_{ramp}$<br>$S_{ramp(HV)}$ | 1.05<br>0.45 | 1.5<br>0.70 | 1.95<br>0.95 | A/μs |

**Table 3. ELECTRICAL CHARACTERISTICS** (continued)
($V_{IN}$ = 4.5 V to 28 V, EN = 5 V. Min/Max values are valid for the temperature range −40°C ≤ $T_J$ ≤ 150°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SHORT CIRCUIT FREQUENCY FOLDBACK** | | | | | | |
| Switching Frequency in Short-Circuit Condition<br>Lowest Foldback Frequency<br>Lowest Foldback Frequency – High $V_{IN}$ | <br>$V_{OUT}$ = 0 V, 4.5 V < $V_{IN}$ < 18 V<br>$V_{OUT}$ = 0 V, 20 V <$V_{IN}$ < 28V | <br>$f_{SWAF}$<br>$f_{SWAFHV}$ | <br>450<br>225 | <br>550<br>275 | <br>650<br>325 | kHz |
| **HICCUP MODE** | | | | | | |
| Hiccup Mode | $V_{SW}$ = 0 V, no switching | $f_{SWHIC}$ | 24 | 32 | 40 | kHz |
| Hiccup Mode 2 – SW Short to Battery | $V_{SW}$ = 13.2 V | $f_{SWHICLS}$ | 24 | 32 | 40 | kHz |
| **SYNCHRONIZATION** | | | | | | |
| SYNC Input Resistance to Ground | $V_{SYNC}$ = 5.0 V | $R_{H(SYNC)}$ | 50 | | 200 | kΩ |
| SYNC Input High Threshold Voltage | | $V_{HSYNC}$ | 2.0 | | | V |
| SYNC Input Low Threshold Voltage | | $V_{LSYNC}$ | | | 0.8 | V |
| SYNC High Pulse Width | $V_{SYNC}$ > max $V_{HSYNC}$ | $t_{HSYNC}$ | 40 | | | ns |
| SYNC Low Pulse Width | $V_{SYNC}$ < min $V_{LSYNC}$ | $t_{LSYNC}$ | 40 | | | ns |
| External SYNC Frequency | 2.5 V Option<br>3.3 V & 5.0 V Options | $f_{SYNC}$ | 1.8<br>1.8 | | 2.2<br>2.5 | MHz |
| Master Reassertion Time | Time from Last Rising SYNC Edge to First Un-synchronized Turn-on. | $t_{I(SYNC)}$ | | 650 | | ns |
| **RESET** | | | | | | |
| Reset Threshold | $V_{OUT}$ Decreasing<br>$V_{OUT}$ Increasing | $K_{RES\_LO}$<br>$K_{RES\_HI}$ | 91<br>91.5 | 93 | 95<br>97 | % |
| Reset Hysteresis (Ratio of VOUT) | | $K_{RES\_HYS}$ | 0.5 | | | % |
| Leakage Current into RSTB Pin | | | | | 1.0 | μA |
| Noise-Filtering Delay | From $V_{OUT}$ < $V_{RESET}$ to RSTB Pin Going Low | $t_{RES\_FILT}$ | 10 | | 25 | μs |
| Reset Delay Time | $I_{RSTB}$ = 1.1 mA<br>$I_{RSTB}$ = 500 μA<br>$I_{RSTB}$ = 100 μA | $t_{RESET}$ | <br>4.0<br>19 | 1.0<br>5.0<br>24 | <br>6.0<br>29 | μs<br>ms<br>ms |
| Reset Delay Modes | Power Good Mode (No Delay)<br>Delay Mode | | 1000 | | <br>600 | μA |
| Reset Output Low Level | $I_{RSTB}$ = 1.2 mA | $V_{RESL}$ | | | 0.4 | V |
| **ENABLE** | | | | | | |
| Logic Low Threshold Voltage | | $V_{ENlow}$ | | | 0.8 | V |
| Logic High Threshold Voltage | | $V_{ENhigh}$ | 2.0 | | | V |
| EN Pin Input Current | | $I_{ENbias}$ | 8.0 | | 30 | μA |
| **THERMAL SHUTDOWN** | | | | | | |
| Thermal Shutdown Activation Temperature (Note 2) | | $T_{SD}$ | 155 | | 190 | °C |
| Thermal Shutdown Hysteresis (Note 2) | | $T_{HYS}$ | 5.0 | | 20 | °C |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
2. Not tested in production. Limits are guaranteed by design.

## TYPICAL CHARACTERISTICS

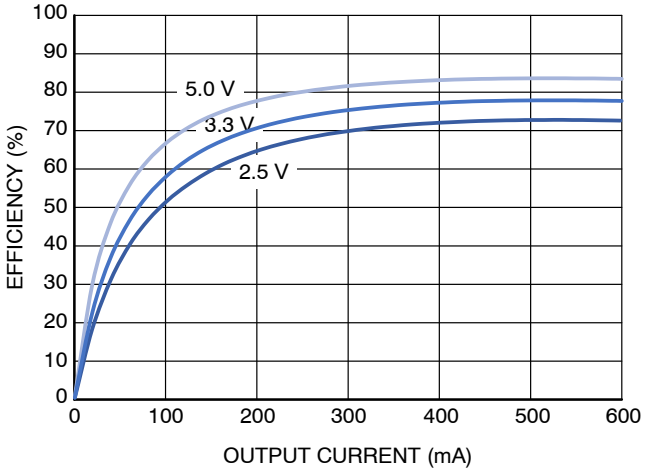



**Figure 3. Measured Efficiency vs. Output Current for 12 V Input Voltage***

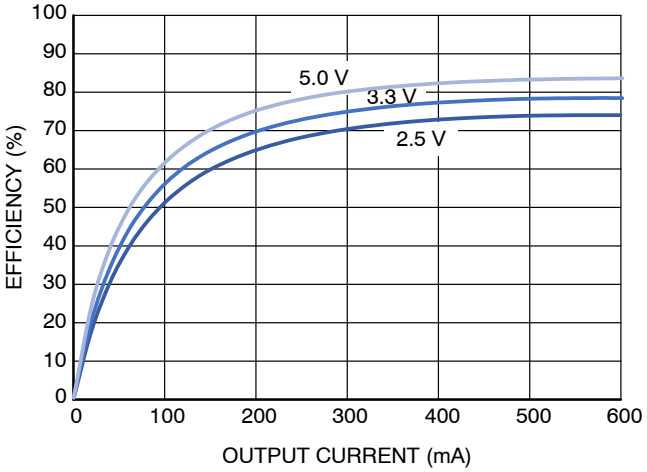



**Figure 4. Measured Efficiency vs. Output Current In Frequency Foldback – 20 V Input Voltage***

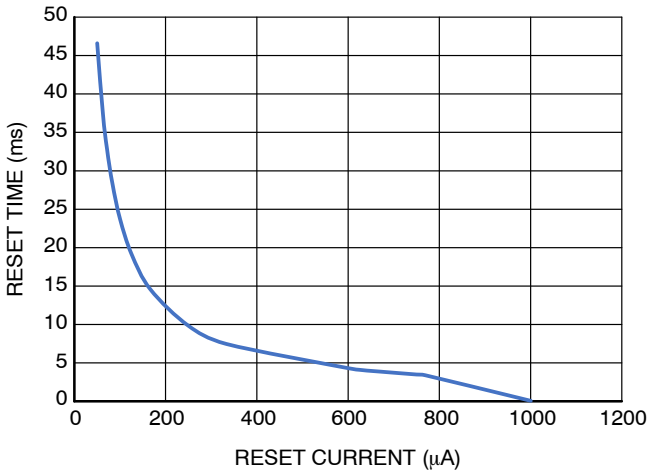



**Figure 5. Measured Reset Time vs. Reset Current****

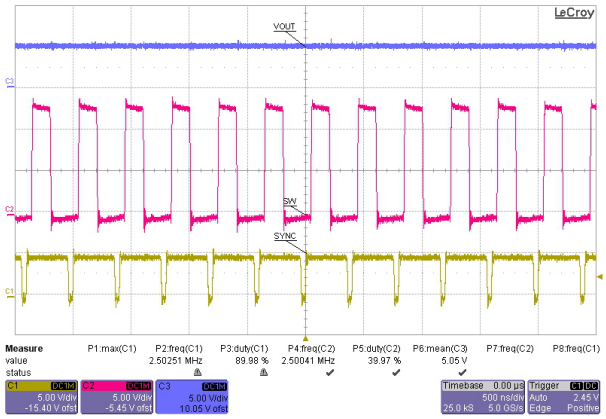



**Figure 6. Synchronization with 90% Duty, 2.5 MHz Signal at SYNC Pin**

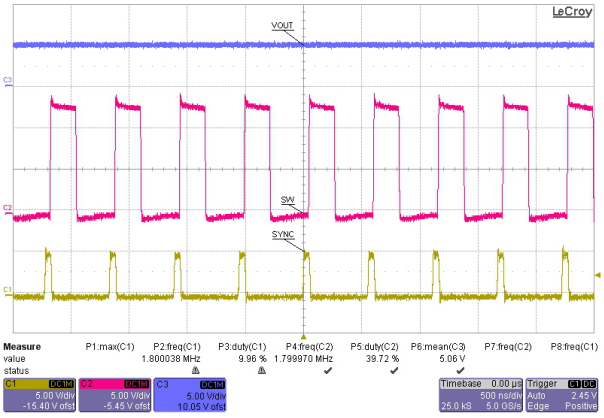



**Figure 7. Synchronization with 10% Duty, 1.8 MHz Signal at SYNC Pin**

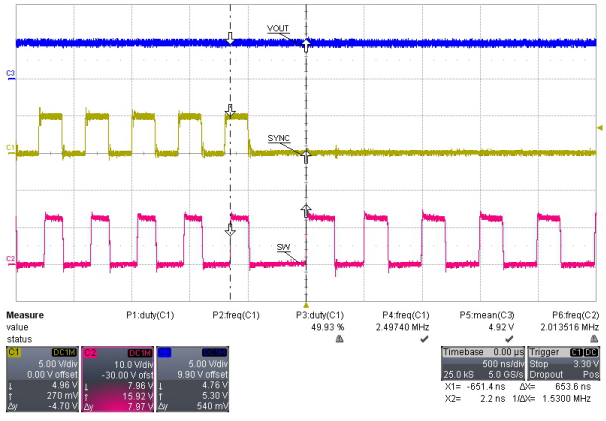



**Figure 8. Master Reassertion Time when 2.5 MHz SYNC Signal Disconnected****

*Efficiency Measurements completed with NCV890430 Demo Board and Bourns SRP4020TA−4R7M Inductor.
**Measurements completed with NCV890430 Demo board populated according to the Bill of Materials unless otherwise stated.

## APPLICATION INFORMATION

### General Description

The NCV890430 is a high-frequency synchronous switch-mode regulator with current-mode control, fixed output voltage and fixed internal closed-loop compensation, accepting a wide input voltage range typical to automotive applications.

The use of a P-channel high-side MOSFET simplifies the driving scheme (no bootstrap circuitry needed), and enables a duty cycle of 100% for low dropout operation at low input voltage.

### Input Voltage

An Undervoltage Lockout (UVLO) circuit monitors the input, and can inhibit switching and reset the soft-start circuit if there is insufficient voltage for proper regulation. Depending on the output conditions (voltage option and loading), the NCV890430 may lose regulation and run in drop-out mode before reaching the UVLO threshold: refer to the Minimum $V_{IN}$ calculation tool for details. When the input voltage drops low enough that the part cannot regulate because it reaches its maximum duty cycle, the high-side MOSFET can turn on permanently (100% duty cycle operation), to help lower the minimum voltage at which the regulator loses regulation.

An overvoltage monitoring circuit automatically terminates switching and disables the output if the input voltage exceeds 37 V (see Figure 9), but the NCV890430 can withstand input voltages up to 45 V.

To avoid skipping switching pulses and entering an uncontrolled mode of operation, the switching frequency is reduced by a factor of 2 when the input voltage exceeds the $V_{IN}$ Frequency Foldback threshold (see Figure 9 below). Frequency reduction is automatically terminated when the input voltage drops back below the $V_{IN}$ Frequency Foldback threshold. This also helps to limit the power lost in switching and generating the drive voltage for the Power Switches at high input voltage. Above the frequency foldback threshold, improved efficiency can be expected due to the lower switching frequency.

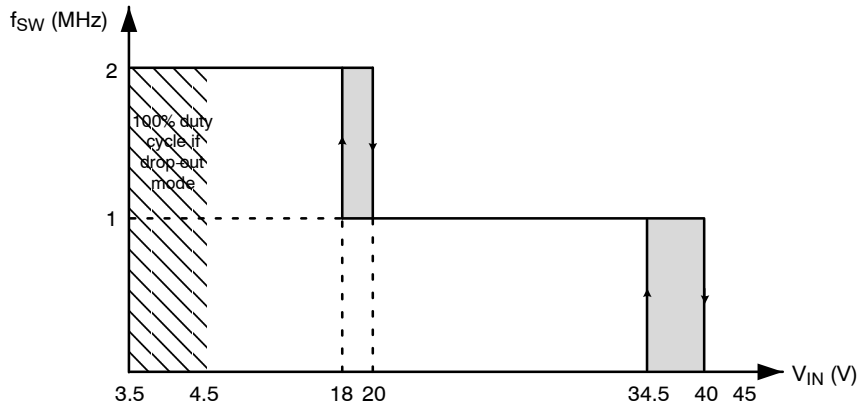



**Figure 9. NCV890430 Worst-Case Switching Frequency Profile vs. Input Voltage**

### Soft-Start

Upon being enabled or released from a fault condition, a soft-start circuit ramps the switching regulator error amplifier reference voltage to the final value, forcing the output to follow the same soft-start ramp. During soft-start, the average switching frequency is lower until the output voltage approaches regulation.

### Slope Compensation

A fixed slope compensation signal is generated internally and added to the sensed current to avoid increased output voltage ripple due to bifurcation of inductor ripple current at duty cycles above 50%. The fixed amplitude of the slope compensation signal requires the inductor to be greater than a minimum value, depending on output voltage, in order to avoid sub-harmonic oscillations. The recommended inductor value is between 1.8 and 3.3 μH, although other values are possible.

### Short Circuit Protection

During severe output overloads or short circuits, the NCV890430 automatically reduces its switching frequency. This creates duty cycles small enough to limit the peak current in the power components, while maintaining the ability to automatically reestablish the output voltage if the overload is removed.

In more severe short-circuit conditions where the inductor current reaches the peak current limit during the minimum on time, the regulator enters a hiccup mode that further reduces the power dissipation and protects the system.

### RESET Function

The RSTB pin is pulled low when the output voltage falls below 7% of the nominal regulation level, and floats when the output is properly regulated. A pull-up resistor tied to the output is needed to generate a logic high signal on this open-drain pin. The pin can be left unconnected when not used.

When the output voltage drops out of regulation, the pin goes low after a short noise-filtering delay ($t_{RES\_FILT}$). After the output goes back to regulation, the RSTB pin stays low for an adjustable delay time, simplifying the connection to a micro-controller.

The RSTB signal can either be used as a reset with delay or a power good (no delay). The adjustable delay is determined by the current into the RSTB pin, set by a resistor, as shown in Figure 10.

Use the following equation to determine the ideal reset delay time using currents less than 500 μA:

$$t_{delay} = \frac{2500}{I_{RSTB}} \qquad \text{(eq. 1)}$$

where: $t_{delay}$ is the ideal reset delay time [ms]
$I_{RSTB}$ is the current into the RSTB pin [μA]

Using $I_{RSTB}$ = 1 mA removes the delay and allows the reset to act as a “power good” pin.

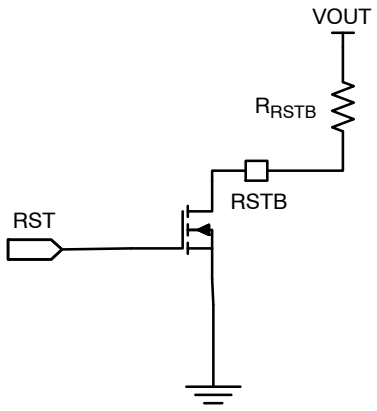



**Figure 10. Reset with Adjustable Delay on a Single Pin**

The RSTB resistor is commonly tied to VOUT. A RSTB resistor value that sets the current at the reset pin between 0.5 mA and 1 mA is not recommended due to the variation of the threshold between a set delay time and power good. Depending on the output voltage option, typical delay times can be achieved with the following resistor values:

**Table 4. TYPICAL DELAY TIMES – MEASURED**

| $R_{RSTB}$ (kΩ) | $t_{delay}$ (ms) – 5 V | $t_{delay}$ (ms) – 3.3 V | $t_{delay}$ (ms) – 2.5 V |
|---|---|---|---|
| 5 | – | – | 5 |
| 10 | 5 | 7.6 | 10 |
| 20 | 10 | 15 | 20 |
| 30 | 15 | 23 | – |
| 50 | 25 | – | – |

### Enable

The NCV890430 is designed to accept either a logic-level signal or battery voltage as an Enable signal. However, if voltages above 40 V are expected, EN should be tied to VIN through a 10 kΩ resistor in order to limit the current flowing into the overvoltage protection of the pin.

A low signal on Enable induces a shutdown mode which shuts off the regulator and minimizes its supply current to less than 5 μA by disabling all functions.

Once the switching regulator output is enabled, a soft-start is always initiated.

### Thermal Shutdown

A thermal shutdown circuit inhibits switching and resets the soft-start circuit if internal temperature exceeds a safe level indicated by the Thermal Shutdown Activation Temperature. Switching is automatically restored when temperature returns to a safe level based on the Thermal Shutdown Hysteresis.

### Synchronization

Any number of NCV890430 can be synchronized to an external clock. If a part does not have its switching frequency controlled by the SYNC input, the part will be driven at the 2 MHz default switching frequency. A rising edge at the SYNC pin causes an NCV890430 to immediately turn on the power switch. If another rising edge does not arrive at the SYNC pin, the NCV890430 will start controlling its own frequency within the Master Reassertion Time. This allows uninterrupted operation if the clock is turned off. An external pulldown resistor is not needed at the SYNC pin if it is unconnected.

### Exposed Pad

The exposed pad (EPAD) on the back of the package must be electrically connected to both the analog and the power electrical ground GND and PGND pins for proper, noise-free operation. It is recommended to connect these 2 pins directly to the EPAD with a PCB trace. Refer to the Recommended Layout for more information.

## DEVICE ORDERING INFORMATION

| Device | Output | Marking | Package | Shipping† |
|---|---|---|---|---|
| NCV890430MW50TXG | 5.0 V | V890430−50 | DFN8 (Pb−Free) | 3000 / Tape & Reel |
| NCV890430MW33TXG | 3.3 V | V890430−33 | | |
| NCV890430MW25TXG | 2.5 V | V890430−25 | | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## RECOMMENDED LAYOUT

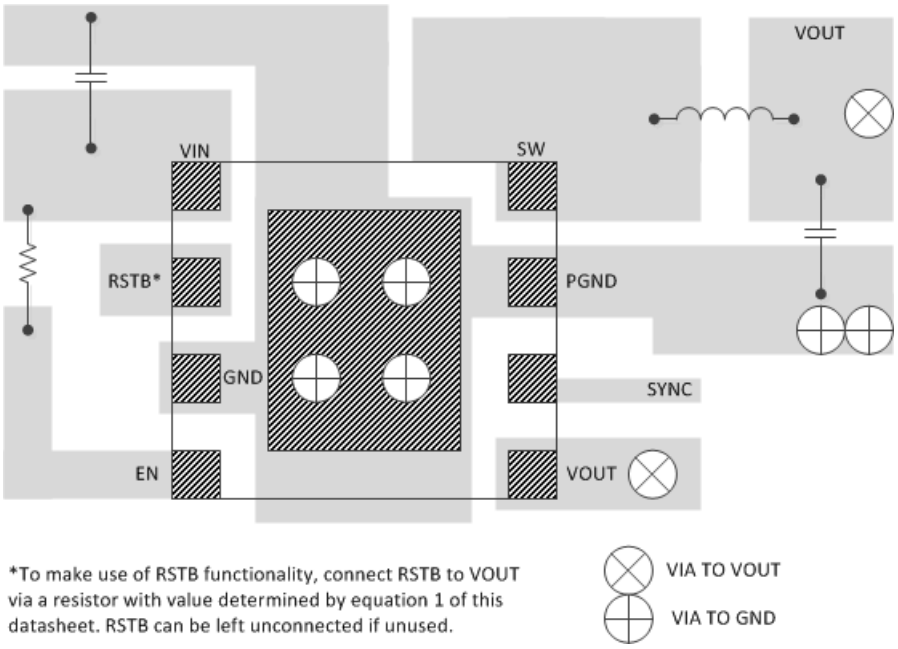



**Figure 11. Recommended NCV890430 Layout**

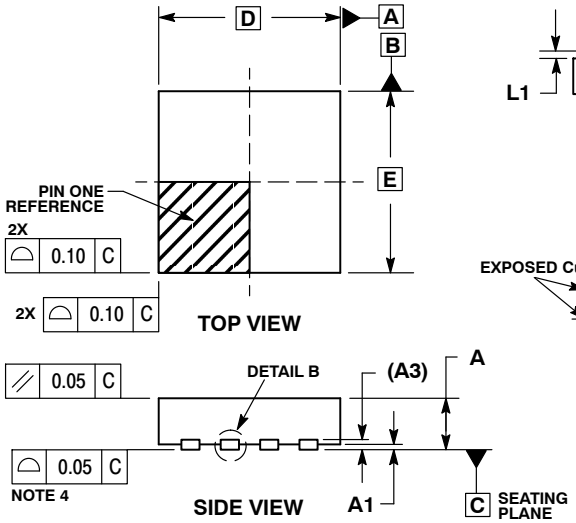
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

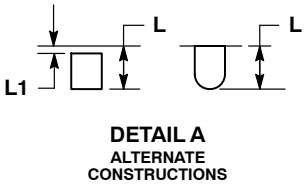
ON Semiconductor®

**DFN8, 3x3, 0.65P**
CASE 506BY
ISSUE A

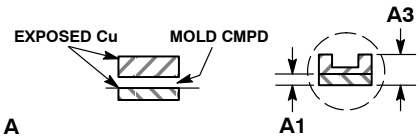
DATE 23 MAY 2012

**SCALE 2:1**



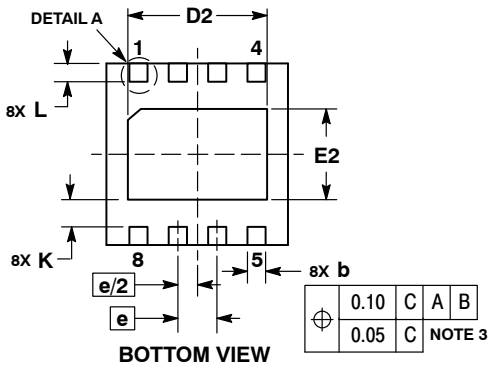

**DETAIL A**
ALTERNATE CONSTRUCTIONS




**DETAIL B**
ALTERNATE CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. FOR DEVICE OPN CONTAINING W OPTION, DETAIL B ALTERNATE CONSTRUCTION IS NOT APPLICABLE.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.25 | 0.35 |
| D | 3.00 BSC | |
| D2 | 2.20 | 2.40 |
| E | 3.00 BSC | |
| E2 | 1.40 | 1.60 |
| e | 0.65 BSC | |
| K | 0.20 | ––– |
| L | 0.20 | 0.40 |
| L1 | 0.00 | 0.15 |



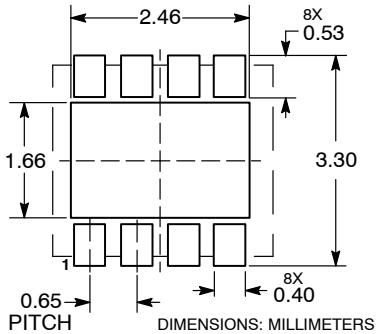

**GENERIC MARKING DIAGRAM***


XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

**RECOMMENDED SOLDERING FOOTPRINT***




DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|---|---|---|
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