# **Analog Multiplexers/Demultiplexers**

The NLHV4051, NLHV4052, and NLHV4053 analog multiplexers are digitally-controlled analog switches. The NLHV4051 effectively implements an SP8T solid state switch, the NLHV4052 a DP4T, and the NLHV4053 a Triple SPDT. All three devices feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

### **Features**

- Triple Diode Protection on Control Inputs
- Switch Function is Break Before Make
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range  $(V_{DD} V_{EE}) = 3.0$  to 18 V Note:  $V_{EE}$  must be  $\leq V_{SS}$
- Linearized Transfer Characteristics
- Low-noise 12 nV/ $\sqrt{\text{Cycle}}$ , f  $\geq$  1.0 kHz Typical
- Pin-for-Pin Replacement for CD4051, CD4052, and CD4053
- For 4PDT Switch, See MC14551B
- For Lower R<sub>ON</sub>, Use the HC4051, HC4052, or HC4053 High–Speed **CMOS** Devices
- These Devices are Pb-Free and are RoHS Compliant

## MAXIMUM RATINGS (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage Range (Referenced to $V_{EE}$ , $V_{SS} \ge V_{EE}$ )	-0.5 to +18.0	٧
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage Range (DC or Transient) (Referenced to V <sub>SS</sub> for Control Inputs and V <sub>EE</sub> for Switch I/O)	-0.5 to V <sub>DD</sub> + 0.5	<b>V</b>
I <sub>in</sub>	Input Current (DC or Transient) per Control Pin	+10	mA
I <sub>SW</sub>	Switch Through Current	±25	mA
P <sub>D</sub>	Power Dissipation per Package (Note 1)	500	mW
T <sub>A</sub>	Ambient Temperature Range	-55 to +125	°C
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range  $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub>, V<sub>EE</sub> or V<sub>DD</sub>). Unused outputs must be left open.



## ON Semiconductor®

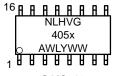
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**DT SUFFIX CASE 948F** 

## **MARKING DIAGRAMS**



SOIC-16



TSSOP-16

= 1, 2, or 3

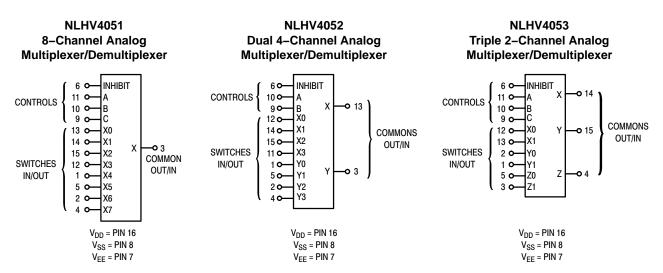
= Assembly Location

WL. L = Wafer Lot = Year = Work Week WW. W = Pb-Free Package

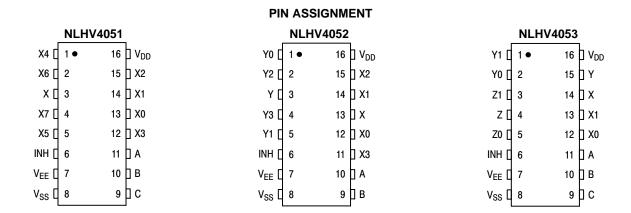
(Note: Microdot may be in either location)

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.



Note: Control Inputs referenced to V<sub>SS</sub>, Analog Inputs and Outputs reference to V<sub>EE</sub>. V<sub>EE</sub> must be ≤ V<sub>SS</sub>.



#### **ELECTRICAL CHARACTERISTICS**

				_55°C 25°C			125°C				
Characteristic	Symbol	V <sub>DD</sub>	Test Conditions	Min	Max	Min	Typ (Note 2)	Max	Min	Max	Unit
SUPPLY REQUIREMENTS	JPPLY REQUIREMENTS (Voltages Referenced to V <sub>EE</sub> )								1		
Power Supply Voltage Range	V <sub>DD</sub>	-	$V_{DD} - 3.0 \ge V_{SS} \ge V_{EE}$	3.0	18	3.0	_	18	3.0	18	V
Quiescent Current Per Package	I <sub>DD</sub>	5.0 10 15	Control Inputs: $\begin{aligned} &V_{in} = V_{SS} \text{ or } V_{DD}, \\ &Switch \text{ I/O: } V_{EE} \leq V_{\text{I/O}} \leq \\ &V_{DD}, \text{ and } \Delta V_{switch} \leq \\ &500 \text{ mV (Note 3)} \end{aligned}$		5.0 10 20		0.005 0.010 0.015	5.0 10 20		150 300 600	μΑ
Total Supply Current (Dynamic Plus Quiescent, Per Package	I <sub>D(AV)</sub>	5.0 10 15	T <sub>A</sub> = 25°C only (The channel component, (V <sub>in</sub> – V <sub>out</sub> )/R <sub>on</sub> , is not included.)		Typical	(	(0.07 μΑ/kHz (0.20 μΑ/kHz (0.36 μΑ/kHz	) f + I <sub>DD</sub>	)		μА
CONTROL INPUTS — INHII	BIT, A, B,	C (Volta	ages Referenced to V <sub>SS</sub> )								
Low-Level Input Voltage	V <sub>IL</sub>	5.0 10 15	R <sub>on</sub> = per spec, I <sub>off</sub> = per spec	- - -	1.5 3.0 4.0	- - -	2.25 4.50 6.75	1.5 3.0 4.0	- - -	1.5 3.0 4.0	V
High-Level Input Voltage	V <sub>IH</sub>	5.0 10 15	R <sub>on</sub> = per spec, I <sub>off</sub> = per spec	3.5 7.0 11	- - -	3.5 7.0 11	2.75 5.50 8.25	- - -	3.5 7.0 11	- - -	V
Input Leakage Current	I <sub>in</sub>	15	$V_{in} = 0 \text{ or } V_{DD}$	-	±0.1	-	±0.00001	±0.1	-	1.0	μΑ
Input Capacitance	C <sub>in</sub>	-		_	_	_	5.0	7.5	_	_	pF
SWITCHES IN/OUT AND CO	OMMONS	OUT/II	N — X, Y, Z (Voltages Refere	nced to	V <sub>EE</sub> )						
Recommended Peak-to-Peak Voltage Into or Out of the Switch	V <sub>I/O</sub>	ı	Channel On or Off	0	V <sub>DD</sub>	0	_	V <sub>DD</sub>	0	V <sub>DD</sub>	V <sub>PP</sub>
Recommended Static or Dynamic Voltage Across the Switch (Note 3) (Figure 5)	$\Delta V_{switch}$	1	Channel On	0	600	0	-	600	0	300	mV
Output Offset Voltage	V <sub>OO</sub>	ı	V <sub>in</sub> = 0 V, No Load	-	-	-	10	-	-	-	μV
ON Resistance	R <sub>on</sub>	5.0 10 15	$\begin{array}{l} \Delta V_{\text{switch}} \leq 500 \text{ mV} \\ \text{(Note 3) } V_{\text{in}} = V_{\text{IL}} \text{ or } V_{\text{IH}} \\ \text{(Control), and } V_{\text{in}} = \\ 0 \text{ to } V_{DD} \text{(Switch)} \end{array}$	- - -	800 400 220	- - -	250 120 80	1050 500 280	- - -	1200 520 300	Ω
$\Delta$ ON Resistance Between Any Two Channels in the Same Package	$\Delta R_{on}$	5.0 10 15		- - -	70 50 45	- - -	25 10 10	70 50 45	- - -	135 95 65	Ω
Off–Channel Leakage Current (Figure 10)	l <sub>off</sub>	15	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control) Channel to Channel or Any One Channel	-	±100	-	±0.05	±100	-	±1000	nA
Capacitance, Switch I/O	C <sub>I/O</sub>	ı	Inhibit = V <sub>DD</sub>	_	_	_	10	_	_	_	pF
Capacitance, Common O/I	C <sub>O/I</sub>	-	Inhibit = V <sub>DD</sub> (NLHV4051) (NLHV4052) (NLHV4053)	- - -	- - -	- - -	60 32 17	- - -	- - -	- - -	pF
Capacitance, Feedthrough (Channel Off)	C <sub>I/O</sub>		Pins Not Adjacent Pins Adjacent	- -	_ _	- -	0.15 0.47	- -	_ _	-	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

<sup>2.</sup> Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

For voltage drops across the switch (ΔV<sub>switch</sub>) > 600 mV (> 300 mV at high temperature), excessive V<sub>DD</sub> current may be drawn, i.e. the current out of the switch may contain both V<sub>DD</sub> and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

 $\textbf{ELECTRICAL CHARACTERISTICS} \text{ (Note 4) } (C_L = 50 \text{ pF, } T_A = 25^{\circ}\text{C) } \text{ ($V_{EE} \leq V_{SS}$ unless otherwise indicated)}$ 

Characteristic	Symbol	V <sub>DD</sub> – V <sub>EE</sub>	Typ (Note 5) All Types	Max	Unit
Propagation Delay Times (Figure 6) Switch Input to Switch Output ( $R_L = 1 \text{ k}\Omega$ ) NLHV4051	t <sub>PLH</sub> , t <sub>PHL</sub>				ns
$t_{PLH}$ , $t_{PHL}$ = (0.17 ns/pF) $C_L$ + 26.5 ns $t_{PLH}$ , $t_{PHL}$ = (0.08 ns/pF) $C_L$ + 11 ns $t_{PLH}$ , $t_{PHL}$ = (0.06 ns/pF) $C_L$ + 9.0 ns		5.0 10 15	35 15 12	90 40 30	
NLHV4052 $t_{PLH}, t_{PHL} = (0.17 \text{ ns/pF}) \text{ C}_{L} + 21.5 \text{ ns} $ $t_{PLH}, t_{PHL} = (0.08 \text{ ns/pF}) \text{ C}_{L} + 8.0 \text{ ns} $ $t_{PLH}, t_{PHL} = (0.06 \text{ ns/pF}) \text{ C}_{L} + 7.0 \text{ ns} $		5.0 10 15	30 12 10	75 30 25	ns
NLHV4053 $t_{PLH}, t_{PHL} = (0.17 \text{ ns/pF}) \text{ C}_{L} + 16.5 \text{ ns} \\ t_{PLH}, t_{PHL} = (0.08 \text{ ns/pF}) \text{ C}_{L} + 4.0 \text{ ns} \\ t_{PLH}, t_{PHL} = (0.06 \text{ ns/pF}) \text{ C}_{L} + 3.0 \text{ ns}$		5.0 10 15	25 8.0 6.0	65 20 15	ns
Inhibit to Output ( $R_L = 10 \text{ k}\Omega$ , $V_{EE} = V_{SS}$ ) Output "1" or "0" to High Impedance, or High Impedance to "1" or "0" Level	t <sub>PHZ</sub> , t <sub>PLZ</sub> , t <sub>PZH</sub> , t <sub>PZL</sub>				ns
NLHV4051		5.0 10 15	350 170 140	700 340 280	
NLHV4052		5.0 10 15	300 155 125	600 310 250	ns
NLHV4053		5.0 10 15	275 140 110	550 280 220	ns
Control Input to Output (R <sub>L</sub> = 1 k $\Omega$ , V <sub>EE</sub> = V <sub>SS</sub> ) NLHV4051	t <sub>PLH</sub> , t <sub>PHL</sub>	5.0 10 15	360 160 120	720 320 240	ns
NLHV4052		5.0 10 15	325 130 90	650 260 180	ns
NLHV4053		5.0 10 15	300 120 80	600 240 160	ns
Second Harmonic Distortion $(R_L = 10K\Omega, f = 1 \text{ kHz}) V_{in} = 5 V_{PP}$	-	10	0.07	_	%
Bandwidth (Figure 7) $ (R_L = 50 \ \Omega, \ V_{in} = 1/2 \ (V_{DD} - V_{EE}) \ p-p, \ C_L = 50 pF \\ 20 \ Log \ (V_{out} / V_{in}) = -3 \ dB) $	BW	10	17	_	MHz
Off Channel Feedthrough Attenuation (Figure 7) $R_L = 1K\Omega, V_{in} = 1/2 (V_{DD} - V_{EE}) p-p$ $f_{in} = 4.5 \text{ MHz} - \text{NLHV4051}$ $f_{in} = 30 \text{ MHz} - \text{NLHV4052}$ $f_{in} = 55 \text{ MHz} - \text{NLHV4053}$	-	10	<b>-50</b>	-	dB
Channel Separation (Figure 8) $ (R_L = 1 \text{ k}\Omega, \text{ V}_{\text{in}} = 1/2 \text{ (V}_{\text{DD}}  \text{V}_{\text{EE}}) \text{ pp}, \\ f_{\text{in}} = 3.0 \text{ MHz} $	-	10	-50	-	dB
Crosstalk, Control Input to Common O/I (Figure 9) $(R_1 = 1 \text{ k}\Omega, \ R_L = 10 \text{ k}\Omega$ $\text{Control } t_{TLH} = t_{THL} = 20 \text{ ns, Inhibit} = V_{SS})$	-	10	75	-	mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

<sup>4.</sup> The formulas given are for the typical characteristics only at 25°C.
5. Data labelled "Typ" is not lo be used for design purposes but In intended as an indication of the IC's potential performance.

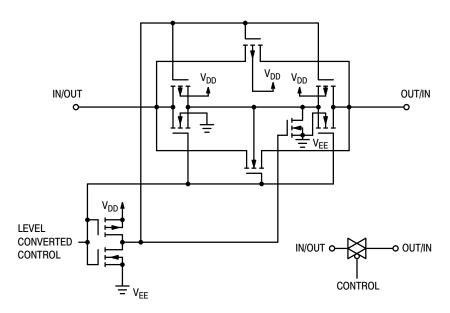


Figure 1. Switch Circuit Schematic

## **TRUTH TABLE**

Conti	Control Inputs														
	Select				ON S	witche	s								
Inhibit	C*	В	Α	NLHV4051	NLH	NLHV4052		NLHV4052		NLHV4052		NLHV4052		HV40	)53
0	0	0	0	X0	Y0	X0	Z0	Y0	X0						
0	0	0	1	X1	Y1	X1	Z0	Y0	X1						
0	0	1	0	X2	Y2	X2	Z0	Y1	X0						
0	0	1	1	Х3	Y3	Х3	Z0	Y1	X1						
0	1	0	0	X4			Z1	Y0	X0						
0	1	0	1	X5			Z1	Y0	X1						
0	1	1	0	X6			Z1	Y1	X0						
0	1	1	1	X7			Z1	Y1	X1						
1	Х	Х	Х	None	None None None										

\*Not applicable for MC14052

x = Don't Care

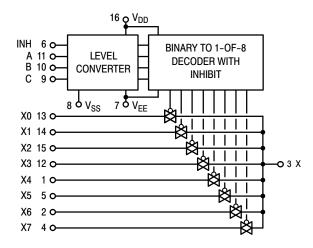


Figure 2. NLHV4051 Functional Diagram

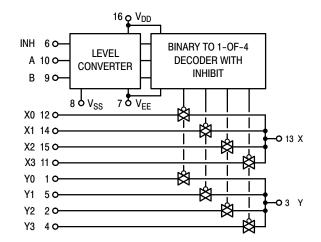


Figure 3. NLHV4052 Functional Diagram

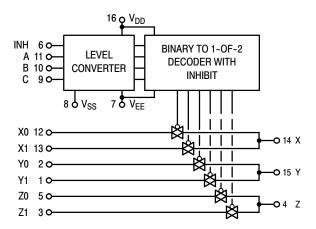


Figure 4. NLHV4053 Functional Diagram

## **TEST CIRCUITS**

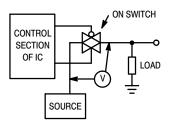


Figure 5.  $\Delta V$  Across Switch

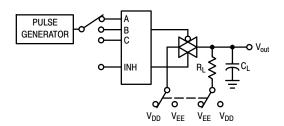


Figure 6. Propagation Delay Times, Control and Inhibit to Output

A, B, and C inputs used to turn ON or OFF the switch under test.

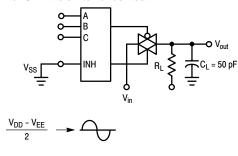


Figure 7. Bandwidth and Off-Channel Feedthrough Attenuation

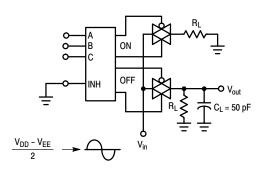


Figure 8. Channel Separation (Adjacent Channels Used For Setup)

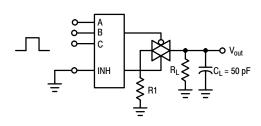


Figure 9. Crosstalk, Control Input to Common O/I

NOTE: See also Figures 7 and 8 in the MC14016B data sheet.

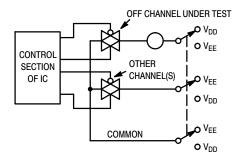


Figure 10. Off Channel Leakage

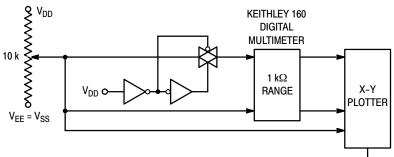


Figure 11. Channel Resistance (R<sub>ON</sub>) Test Circuit

### TYPICAL RESISTANCE CHARACTERISTICS

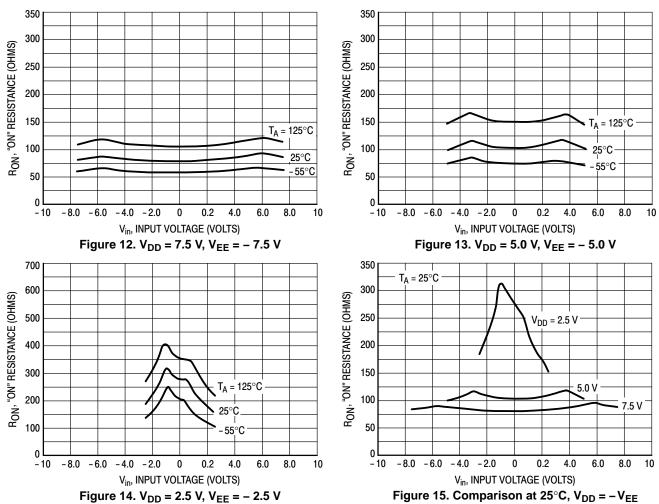


Figure 15. Comparison at 25°C,  $V_{DD} = -V_{EE}$ 

### APPLICATIONS INFORMATION

Figure A illustrates use of the on-chip level converter detailed in Figures 2, 3, and 4. The 0-to-5 V Digital Control signal is used to directly control a 9 V<sub>p-p</sub> analog signal.

The digital control logic levels are determined by V<sub>DD</sub> and V<sub>SS</sub>. The V<sub>DD</sub> voltage is the logic high voltage; the V<sub>SS</sub> voltage is logic low. For the example,  $V_{DD} = +5 \text{ V} = \text{logic}$ high at the control inputs;  $V_{SS} = GND = 0 \text{ V} = \text{logic low}$ .

The maximum analog signal level is determined by V<sub>DD</sub> and V<sub>EE</sub>. The V<sub>DD</sub> voltage determines the maximum recommended peak above VSS. The VEE voltage determines the maximum swing below VSS. For the example,  $V_{DD} - V_{SS} = 5 \text{ V}$  maximum swing above  $V_{SS}$ ;  $V_{SS} - V_{EE} = 5 \text{ V}$  maximum swing below  $V_{SS}$ . The example shows a ±4.5 V signal which allows a 1/2 volt margin at each peak. If voltage transients above V<sub>DD</sub> and/or below V<sub>EE</sub> are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The absolute maximum potential difference between V<sub>DD</sub> and V<sub>EE</sub> is 18.0 V. Most parameters are specified up to 15 V which is the recommended maximum difference between V<sub>DD</sub> and V<sub>EE</sub>.

Balanced supplies are not required. However, V<sub>SS</sub> must be greater than or equal to  $V_{EE}$ . For example,  $V_{DD} = +10 \text{ V}$ ,  $V_{SS} = +5$  V, and  $V_{EE} - 3$  V is acceptable. See the Table

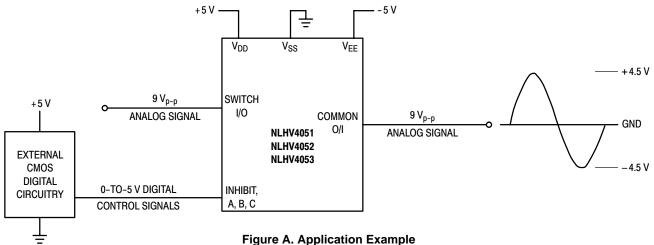


Figure A. Application Example

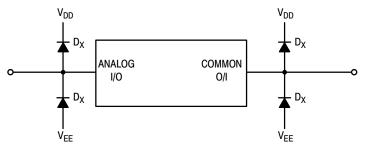


Figure B. External Germanium or Schottky Clipping Diodes

## POSSIBLE SUPPLY CONNECTIONS

V <sub>DD</sub> In Volts	V <sub>SS</sub> In Volts	V <sub>EE</sub> In Volts	Control Inputs Logic High/Logic Low In Volts	Maximum Analog Signal Range In Volts
+8	0	-8	+8/0	$+8 \text{ to } -8 = 16 \text{ V}_{p-p}$
+5	0	-12	+5/0	$+5 \text{ to } -12 = 17 \text{ V}_{p-p}$
+5	0	0	+5/0	$+5 \text{ to } 0 = 5 \text{ V}_{p-p}$
+5	0	-5	+5/0	+5 to -5 = 10 V <sub>p-p</sub>
+10	+5	-5	+10/ +5	+10 to -5 = 15 V <sub>p-p</sub>

## **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NLHV4051DR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel
NLHV4051DTR2G	TSSOP-16 (Pb-Free)	2500 / Tape & Reel
NLHV4052DR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel
NLHV4052DTR2G	TSSOP-16 (Pb-Free)	2500 / Tape & Reel
NLHV4053DR2G (In Development)	SOIC-16 (Pb-Free)	2500 / Tape & Reel
NLHV4053DTR2G (In Development)	TSSOP-16 (Pb-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## **MECHANICAL CASE OUTLINE**



**DATE 29 DEC 2006** 

- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI
- THE NOTION AND TOLETANOING FER ANSI'Y 14.5M, 1982.
  CONTROLLING DIMENSION: MILLIMETER.
  DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- PHOI HUSION.

  MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

  DIMENSION D DOES NOT INCLUDE DAMBAR
  PROTRUSION. ALLOWABLE DAMBAR PROTRUSION

  SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D

  DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	METERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	9.80	10.00	0.386	0.393	
В	3.80	4.00	0.150	0.157	
C	1.35	1.75	0.054	0.068	
D	0.35	0.49	0.014	0.019	
F	0.40	1.25	0.016	0.049	
G	1.27	BSC	0.050 BSC		
J	0.19	0.25	0.008	0.009	
K	0.10	0.25	0.004	0.009	
M	0°	7°	0°	7°	
P	5.80	6.20	0.229	0.244	
R	0.25	0.50	0.010	0.019	

STYLE 1:		STYLE 2:		STYLE 3:		STYLE 4:			
PIN 1.	COLLECTOR	PIN 1.	CATHODE	PIN 1.	COLLECTOR, DYE #1	PIN 1.	COLLECTOR, DYE	#1	
2.	BASE	2.	ANODE	2.	BASE, #1	2.	COLLECTOR, #1		
3.	EMITTER	3.	NO CONNECTION	3.	EMITTER, #1	3.	COLLECTOR, #2		
4.	NO CONNECTION	4.	CATHODE	4.	COLLECTOR, #1	4.	COLLECTOR, #2		
5.	EMITTER	5.	CATHODE	5.	COLLECTOR, #2	5.	COLLECTOR, #3		
6.	BASE	6.	NO CONNECTION	6.	BASE, #2	6.	COLLECTOR, #3		
7.	COLLECTOR	7.	ANODE	7.	EMITTER, #2	7.	COLLECTOR, #4		
8.	COLLECTOR	8.	CATHODE	8.	COLLECTOR, #2	8.	COLLECTOR, #4		
9.	BASE	9.	CATHODE	9.	COLLECTOR, #3	9.	BASE, #4		
10.	EMITTER	10.	ANODE	10.	BASE, #3	10.	EMITTER, #4		
11.	NO CONNECTION	11.	NO CONNECTION	11.	EMITTER, #3	11.	BASE, #3		
12.	EMITTER	12.	CATHODE	12.	COLLECTOR, #3	12.	EMITTER, #3		
13.	BASE	13.	CATHODE	13.	COLLECTOR, #4	13.	BASE, #2	COL DEDING	FOOTPRINT
14.	COLLECTOR	14.	NO CONNECTION	14.	BASE, #4	14.	EMITTER, #2	SOLDERING	3 FOOTPRINT
15.	EMITTER	15.	ANODE	15.	EMITTER, #4	15.	BASE, #1		8X
16.	COLLECTOR	16.	CATHODE	16.	COLLECTOR, #4	16.	EMITTER, #1		5.40 <del>→</del>
								7	,.40
STYLE 5:		STYLE 6:		STYLE 7:					16X 1.12 <
PIN 1.	DRAIN, DYE #1		CATHODE	PIN 1.	SOURCE N-CH				
2.	DRAIN, #1		CATHODE	2.	COMMON DRAIN (OUTPU	T)		. 1	16
3.	DRAIN, #2	3.		3.	COMMON DRAIN (OUTPU			<b>↓ └──</b> ·	" 🗀
4.	DRAIN, #2	4.	CATHODE	4.	GATE P-CH	•,		<del>-</del> —	
5.	DRAIN, #3	5.	CATHODE	5.	COMMON DRAIN (OUTPU	T)	16	5X <b>T</b>	
6.	DRAIN, #3	6.	CATHODE	6.	COMMON DRAIN (OUTPU		0.5	iii I	' <u> </u>
7.	DRAIN, #4	7.	CATHODE	7.	COMMON DRAIN (OUTPU		0.0		
8.	DRAIN, #4	8.	CATHODE	8.	SOURCE P-CH	,			
9.	GATE, #4	9.	ANODE	9.	SOURCE P-CH				
10.	SOURCE, #4	10.	ANODE	10.	COMMON DRAIN (OUTPU	T)			
11.	GATE, #3	11.	ANODE	11.	COMMON DRAIN (OUTPU	T)			
12.	SOURCE, #3	12.	ANODE	12.	COMMON DRAIN (OUTPU	T)			
13.	GATE, #2	13.	ANODE	13.	GATE N-CH				
14.	SOURCE, #2	14.	ANODE	14.	COMMON DRAIN (OUTPU	T)			— V PITCH
15.	GATE, #1	15.	ANODE	15.	COMMON DRAIN (OUTPU				<u> </u>
16.	SOURCE, #1	16.	ANODE	16.	SOURCE N-CH				
								8	9 + - + -
								<del></del> •	_ <del>-</del> <del> </del> ↑
									DIMENSIONS: MILLIMETERS
									DIMENSIONS: MILLIMETERS

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☐ 0.10 (0.004)

D

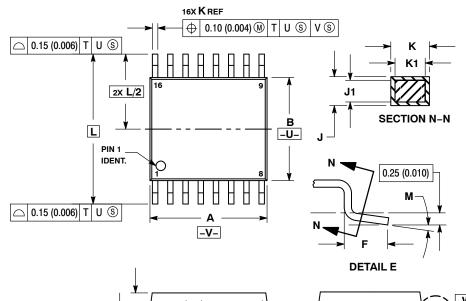
-T- SEATING PLANE





TSSOP-16 CASE 948F-01 ISSUE B

**DATE 19 OCT 2006** 



#### NOTES

- JIES:
  DIMENSIONING AND TOLERANCING PER
  ANSI Y14.5M, 1982.
  CONTROLLING DIMENSION: MILLIMETER.
  DIMENSION A DOES NOT INCLUDE MOLD
  FLASH. PROTRUSIONS OR GATE BURRS.
  MOLD EL ROLL OF GATE BURDS SUAL NO.
- MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
  INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION. TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.
- 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	4.90	5.10	0.193	0.200	
В	4.30	4.50	0.169	0.177	
C		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026 BSC		
Н	0.18	0.28	0.007	0.011	
7	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
Ы	6.40		0.252 BSC		
М	0 °	8 °	0 °	8 °	

## **SOLDERING FOOTPRINT**

G



## **GENERIC MARKING DIAGRAM\***

168888888 XXXX XXXX **ALYW** 1<del>88888888</del>

XXXX = Specific Device Code Α = Assembly Location

= Wafer Lot L Υ = Year W = Work Week = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present.

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