NCV47823

Dual High Side Switch with Adjustable Constant Current and Diagnostic Features

The NCV47823 is designed for using in harsh automotive environments providing dual mode operation depending on the load impedance: High Side Switch (HSS) or Constant Current Source (CCS). In both modes of operation the current limit can be set up to 350 mA per channel by external resistor. The device has a high peak input voltage tolerance and reverse input voltage, reverse bias, overcurrent and overtemperature protections. The integrated current sense feature (adjustable by resistor connected to CSO pin for each channel) provides diagnosis and system protection functionality. The CSO pin output current creates voltage drop across CSO resistor which is proportional to output current of each channel. Extended diagnostic features in OFF state are also available and controlled by dedicated input and output pins.

Features

- Reduced Inrush Current (current value set by external resistor only)
- Adjustable Constant Current: up to 350 mA
- Two Independent Enable Inputs (3.3 V Logic Compatible)
- PWM Function of Enable Inputs Available
- Protection Features:
  - Current Limitation
  - Thermal Shutdown
  - Reverse Input Voltage and Reverse Bias Voltage
  - Reduced Reverse Bias Current
- Diagnostic Features:
  - Short To Battery (STB) and Open Load (OL) in OFF State
  - Internal Components for OFF State Diagnostics
  - Open Collector Flag Output
  - Two Output Voltage Monitoring Outputs (Analog)
- AEC−Q100 Grade 1 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Audio and Infotainment System
- Active Safety System
- LED Lighting Systems

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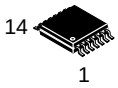
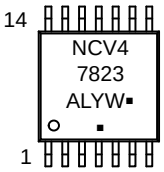


TSSOP−14
Exposed Pad
CASE 948AW

MARKING DIAGRAM



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 14 of sheet.

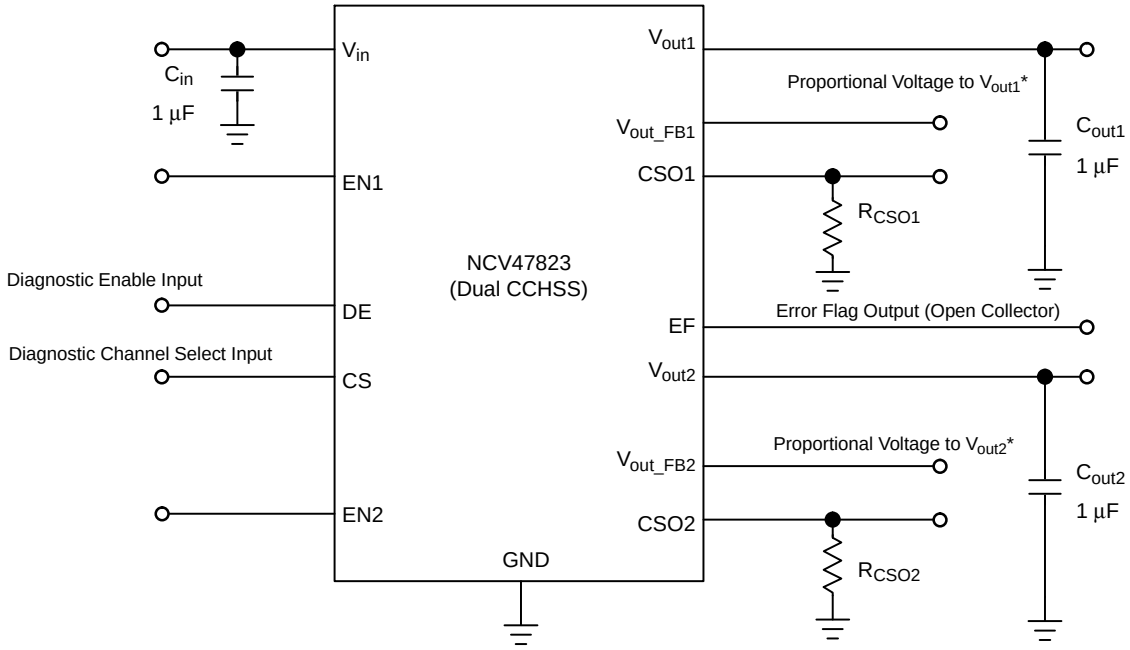
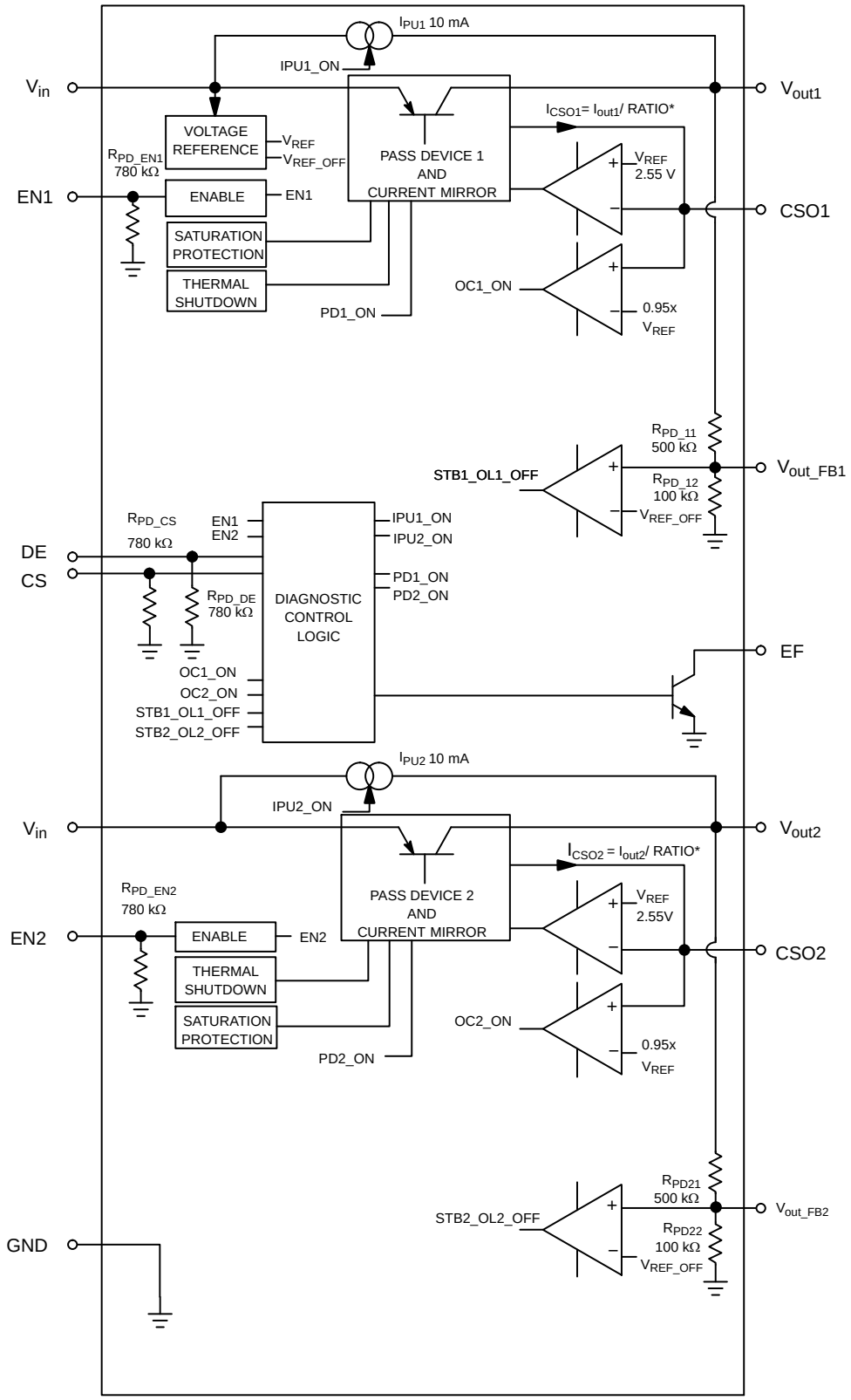


Figure 1. Application Schematic

* V_{out_FB1} and V_{out_FB2} are sensed V_{out1} and V_{out2} output voltages, respectively, via internal resistor dividers



* for current value of RATIO see into Electrical Characteristic Table

Figure 2. Simplified Block Diagram

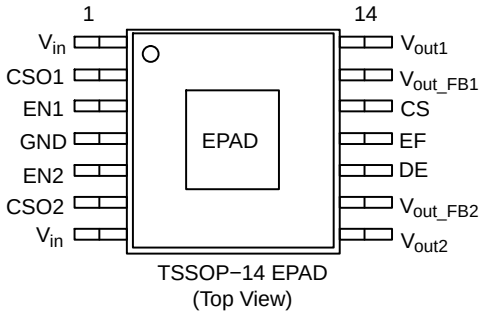


Figure 3. Pin Connections

Table 1. PIN FUNCTION DESCRIPTION

Pin No. TSSOP−14 EPAD	Pin Name	Description
1	V_{in}	Power Supply Input for Channel 1 and supply of control circuits of whole chip. At least 4.4 V power supply must be used for proper IC functionality.
2	CSO1	Current Sense Output 1, Current Limit setting and Output Current value information. See Application Section for more details.
3	EN1	Enable Input 1; low level disables the Channel 1. (Used also for OFF state diagnostics control for Channel 1)
4	GND	Power Supply Ground.
5	EN2	Enable Input 2; low level disables the Channel 2. (Used also for OFF state diagnostics control for Channel 2)
6	CSO2	Current Sense Output 2, Current Limit setting and Output Current value information. See Application Section for more details.
7	V_{in}	Power Supply Input for Channel 2. Connect to pin 1 or different power supply rail.
8	V_{out2}	Output Voltage 2.
9	V_{out_FB2}	Output Voltage 2 Analog Monitoring. See Application Section for more details.
10	DE	Diagnostic Enable Input.
11	EF	Error Flag (Open Collector) Output. Active Low.
12	CS	Channel Select Input for OFF state diagnostics. Set CS = Low for OFF state diagnostics of Channel 1. Set CS = High for OFF state diagnostics of Channel 2. Corresponding EN pin has to be used for diagnostics control (see Application Information section for more details).
13	V_{out_FB1}	Output Voltage 1 Analog Monitoring. See Application Section for more details.
14	V_{out1}	Output Voltage 1.
EPAD	EPAD	Exposed Pad is connected to Ground. Connect to GND plane on PCB.

Table 2. MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Input Voltage DC	V_{in}	−42	45	V
Input Voltage (Note 1) Load Dump − Suppressed	U_{S*}	−	60	V
Enable Input Voltage	$V_{EN1,2}$	−42	45	V
Output Voltage Monitoring	$V_{out\_FB1,2}$	−0.3	10	V
CSO Voltage	$V_{CSO1,2}$	−0.3	7	V
DE, CS and EF Voltages	V_{DE}, V_{CS}, V_{EF}	−0.3	7	V
Output Voltage	$V_{out1,2}$	−1	40	V
Junction Temperature	T_J	−40	150	°C
Storage Temperature	T_{STG}	−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Load Dump Test B (with centralized load dump suppression) according to ISO16750−2 standard. Guaranteed by design. Not tested in production. Passed Class A according to ISO16750−1.

Table 3. ESD CAPABILITY (Note 2)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	ESD_{HBM}	−2	2	kV

2. This device series incorporates ESD protection and is tested by the following methods.
   ESD Human Body Model tested per AEC−Q100−002 (JS−001−2010)
   Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes < 50 mm^2 due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS−002−2014.

Table 4. LEAD SOLDERING TEMPERATURE AND MSL (Note 3)

Rating	Symbol	Min	Max	Unit
Moisture Sensitivity Level	MSL	1		−

3. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

Table 5. THERMAL CHARACTERISTICS (Note 4)

Rating	Symbol	Value	Unit
Thermal Characteristics (single layer PCB) Thermal Resistance, Junction−to−Air (Note 5) Thermal Reference, Junction−to−Lead (Note 5)	 $R_{\theta JA}$ $R_{\psi JL}$	 52 9.0	°C/W
Thermal Characteristics (4 layers PCB) Thermal Resistance, Junction−to−Air (Note 5) Thermal Reference, Junction−to−Lead (Note 5)	 $R_{\theta JA}$ $R_{\psi JL}$	 31 10	°C/W

4. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
5. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate. Single layer − according to JEDEC51.3, 4 layers − according to JEDEC51.7

Table 6. RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 6)	V_{in}	4.4	40	V
Output Current Limit (Note 7)	$I_{LIM1,2}$	10	350	mA
Junction Temperature	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Minimum V_{in} = 4.4 V or ($V_{out1,2}$ + 0.5 V), whichever is higher.
7. Corresponding $R_{CSO1,2}$ is in range from 67.5 kΩ down to 2040 Ω

Table 7. ELECTRICAL CHARACTERISTICS V_{in} = 13.5 V, $V_{EN1,2}$ = 3.3 V, V_{DE} = 0 V, $R_{CSO1,2}$ = 0 Ω, C_{in} = 1 μF, $C_{out1,2}$ = 1 μF, Min and Max values are valid for temperature range −40°C ≤ T_J ≤ +150°C unless noted otherwise and are guaranteed by test, design or statistical correlation. Typical values are referenced to T_J = 25°C (Note 8)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
OUTPUTS						
Input to Output Differential Voltage	V_{in} = 8 V to 18 V $I_{out1,2}$ = 200 mA $I_{out1,2}$ = 250 mA	$V_{in-out1,2}$	–	 210 230	 350 400	mV
CURRENT LIMIT PROTECTION						
Current Limit	$V_{out1,2} = V_{in}$ – 1 V	$I_{LIM1,2}$	350	–	–	mA
DISABLE AND QUIESCENT CURRENTS						
Disable Current	$V_{EN1,2}$ = 0 V	I_{DIS}	–	5	20	μA
Quiescent Current, $I_q = I_{in} – (I_{out1} + I_{out2})$	$I_{out1} = I_{out2}$ = 500 μA, V_{in} = 8 V to 18 V	I_q	–	0.85	1.5	mA
Quiescent Current, $I_q = I_{in} – (I_{out1} + I_{out2})$	$I_{out1} = I_{out2}$ = 200 mA, V_{in} = 8 V to 18 V	I_q	–	15	25	mA
Quiescent Current, $I_q = I_{in} – (I_{out1} + I_{out2})$	$I_{out1} = I_{out2}$ = 250 mA, V_{in} = 8 V to 18 V	I_q	–	20	40	mA
ENABLE						
Enable Input Threshold Voltage Logic Low (OFF) Logic High (ON)	 $V_{out1,2} \le$ 0.1 V $V_{out1,2} \ge V_{in}$ – 1 V	$V_{th(EN1,2)}$	 0.99 –	 1.8 1.9	 – 2.31	V
Enable Input Current	$V_{EN1,2}$ = 3.3 V	$I_{EN1,2}$	2	7	20	μA
Turn On Time from from Enable ON to $V_{out1,2} = V_{in}$ – 1 V	$I_{out1,2}$ = 100 mA	t_{on}	–	25	–	μs
OUTPUT CURRENT SENSE						
CSO Voltage Level at Current Limit	$V_{out1,2} = V_{in}$ – 1 V $R_{CSO1,2}$ = 3.3 kΩ	$V_{CSO\_Ilim1,2}$	2.474 (−3 %)	2.55	2.626 (+3 %)	V
CSO Transient Voltage Level	$R_{CSO1,2}$ = 3.3 kΩ $I_{out1,2}$ pulse from 10 mA to 350 mA, t_r = 1μs	$V_{CSO1,2}$	–	–	3.3	V
Output Current to CSO Current Ratio	$V_{CSO1,2}$ = 2 V, $I_{out1,2}$ = 10 mA to 50 mA V_{in} = 8 V to 18 V, −40°C ≤ T_J ≤ +150°C	$I_{out1,2}/I_{CSO1,2}$	– (−15 %)	265	– (+15 %)	–
	$V_{CSO1,2}$ = 2 V, $I_{out1,2}$ = 50 mA to 200 mA V_{in} = 8 V to 18 V, −40°C ≤ T_J ≤ +150°C		– (−5 %)	285	– (+5 %)	
	$V_{CSO1,2}$ = 2 V, $I_{out1,2}$ = 200 mA to 350 mA V_{in} = 8 V to 18 V, −40°C ≤ T_J ≤ +150°C		– (−5 %)	280	– (+5 %)	
CSO Current at no Load Current	$V_{CSO1,2}$ = 0 V, $I_{out1,2}$ = 0 mA	$I_{CSO\_off1,2}$	–	–	15	μA
REVERSE BIAS CURRENT						
Reverse Current	V_{in} = 0 V, $V_{out1,2}$ = 18 V, $V_{EN1,2}$ = 0 V	$I_{out\_rev1,2}$	−2	−0.03	–	mA
DIAGNOSTICS						
Short to Ground (STG) Voltage Threshold in ON State	V_{in} = 4.4 V to 18 V $R_{CSO1,2}$ = 3.3 kΩ	$V_{STG1,2}$	2	3	4	V
Short To Battery (STB) Voltage Threshold in OFF state	V_{in} = 4.4 V to 18 V, $I_{out1} = I_{out2}$ = 0 mA V_{DE} = 3.3 V	$V_{STB1,2}$	2	3	4	V

Open Load (OL) Current Threshold in OFF state	V_{in} = 4.4 V to 18 V, V_{DE} = 3.3 V	$I_{OL1,2}$	5.0	10	25	mA
Output Voltage to Output Feedback Voltege Ratio	V_{in} = 4.4 V to 18 V	$V_{out1,2}/V_{out\_FB1,2}$	5.7	6.0	6.3	–
Diagnostics Enable Threshold Voltage Logic Low Logic High		$V_{th(DE)}$	 0.99 –	 1.8 1.9	 – 2.31	V
Channel Select Threshold Voltage Logic Low Logic High		$V_{th(CS)}$	 0.99 –	 1.8 1.9	 – 2.31	V
Error Flag Low Voltage	I_{EF} = −1 mA	V_{EF_Low}	–	0.04	0.4	V
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 9)	I_{out1} = I_{out2} = 90 mA, each channel measured separately	$T_{SD1,2}$	150	175	195	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible
9. Values based on design and/or characterization.

TYPICAL CHARACTERISTICS

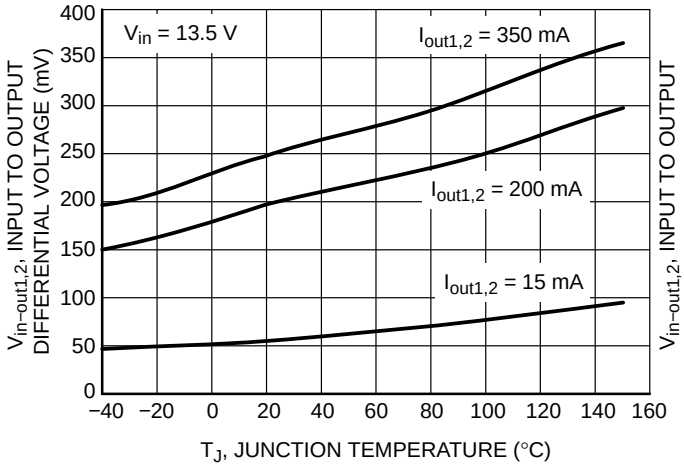


Figure 4. Input to Output Differential Voltage vs. Temperature

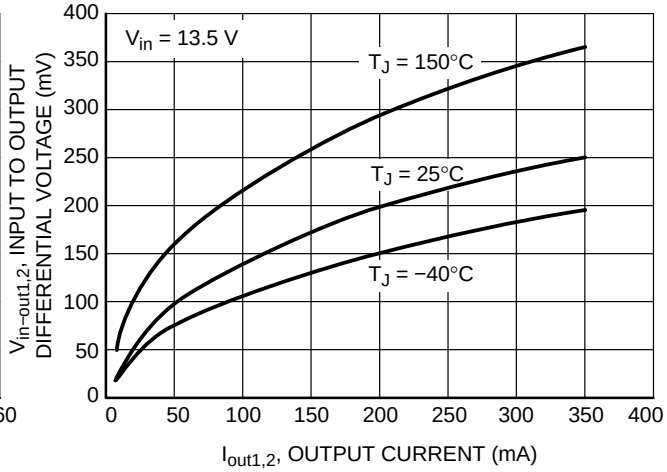


Figure 5. Input to Output Differential Voltage vs. Output Current

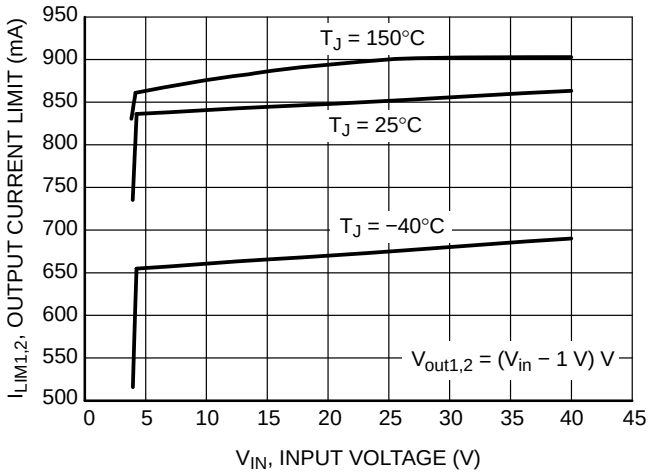


Figure 6. Output Current Limit vs. Input Voltage

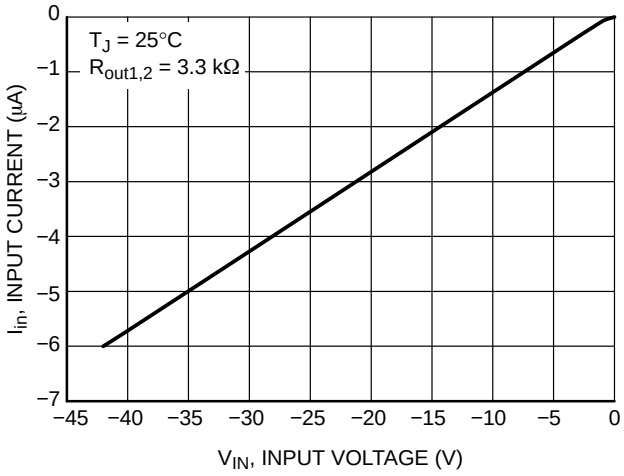


Figure 7. Input Current vs. Input Voltage (Reverse Input Voltage)

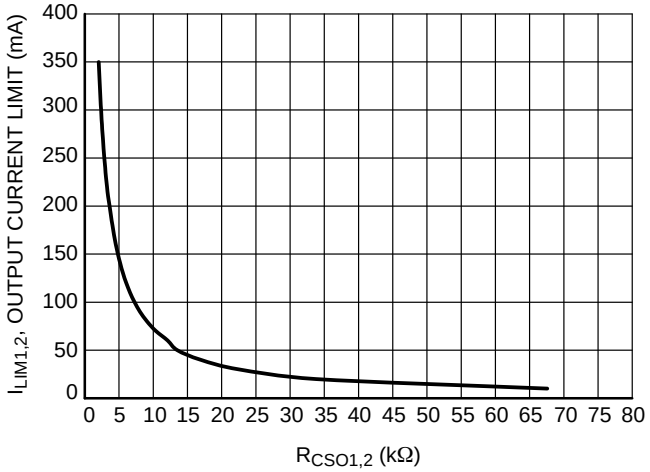


Figure 8. Output Current Limit vs. R_{CSO}

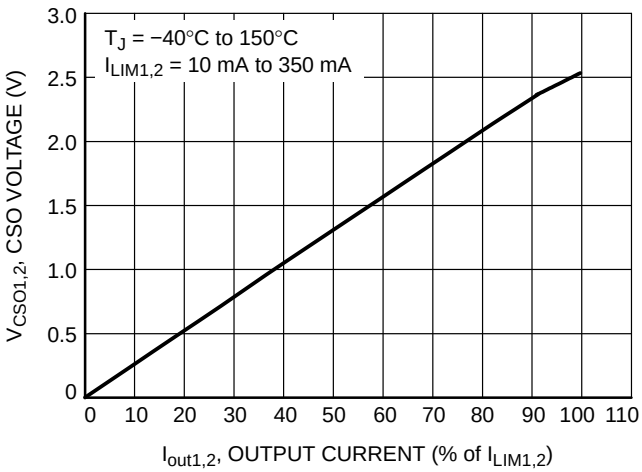


Figure 9. CSO Voltage vs. Output Current (% of I_{LIM})

TYPICAL CHARACTERISTICS

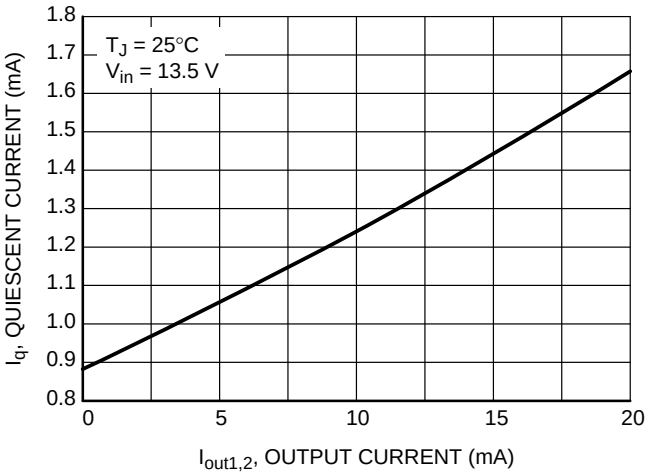


Figure 10. Quiescent Current vs. Output Current (Low Load)

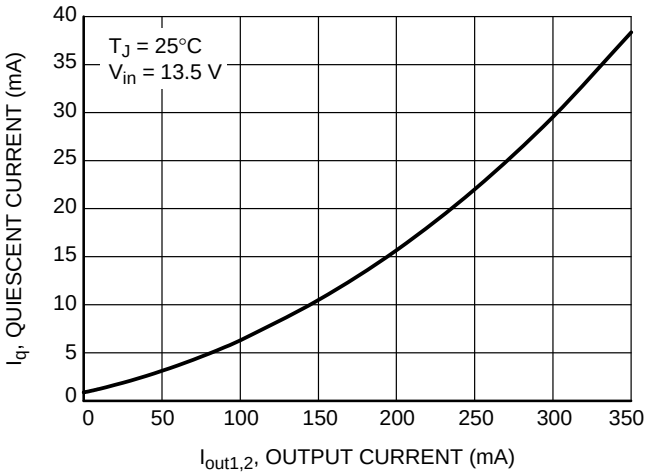


Figure 11. Quiescent Current vs. Output Current (High Load)

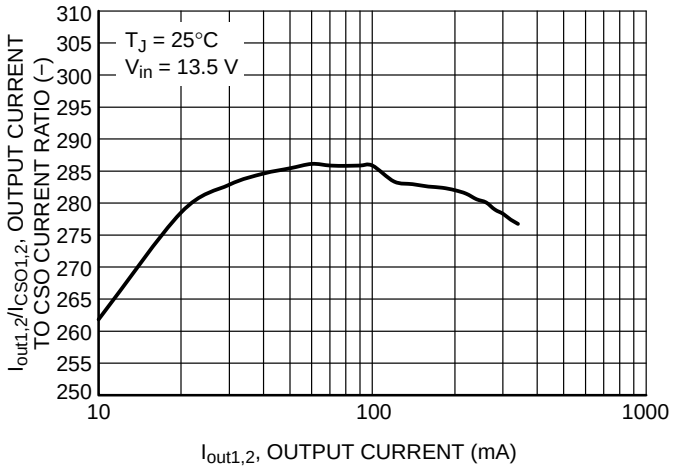


Figure 12. Output Current to CSO Current Ratio vs. Output Current

DEFINITIONS

General

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

Input to Output Differential Voltage

The Input to Output Differential Voltage parameter is defined for specific output current values and specified over Temperature range.

Quiescent and Disable Currents

Quiescent Current (I_q) is the difference between the input current (measured through the LDO input pin) and the output load current. If Enable pin is set to LOW the regulator reduces its internal bias and shuts off the output, this term is called the disable current (I_{DIS}).

Current Limit

Current Limit is value of output current by which output voltage drops to or below V_{in} − 1 V value.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 175°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

APPLICATIONS INFORMATION

Circuit Description

The NCV47823 is an integrated dual High Side Switch (HSS) with current limit up to 350 mA per channel able to operate in Constant Current Source (CCS) mode depending on the output current load. The operation mode can be expressed by equations as follows:

$$\text{HSSmode}: \frac{(V_{in} - V_{in-out1,2})}{R_{load1,2}} = I_{out1,2} < I_{LIM1,2} \quad \text{(eq. 1)}$$

or

$$\text{CCSmode}: \frac{(V_{in} - V_{in-out1,2})}{R_{load1,2}} = I_{out1,2} = I_{LIM1,2} \quad \text{(eq. 2)}$$

where $I_{LIM1,2}$ value is preset by $R_{CSO1,2}$. In HSS mode of operation (eq. 1) output current $I_{out1,2}$ may exceed $I_{LIM1,2}$ (reduced inrush current). Voltage on CSO pin is proportional to output current. The operation mode with PWM function of Enable inputs is provided by the circuit. The integrated current sense features diagnosis and system protection functionality. The HSS is protected by both current limit and thermal shutdown. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

Enable Inputs

An enable pin is used to turn the channel on or off. By holding the pin down to a voltage less than 0.99 V, the output of the channel will be turned off. When the voltage on the enable pin is greater than 2.31 V, the output of the channel will be enabled to power its output to the regulated output voltage. The enable pins may be connected directly to the input pin to give constant enable to the output channel. As mentioned above, the circuit allows using both Enable inputs to obtain PWM of output current.

Setting the Output Current Limit

The output current value can be set up to 350 mA by external resistor $R_{CSO1,2}$ (see Figure 1).

$$V_{CSO1,2} = I_{out1,2}\left(R_{CSO1,2} \times \frac{1}{RATIO}\right) \quad \text{(eq. 3)}$$

$$I_{LIM1,2} = \frac{RATIO}{1} \times \frac{2.55}{R_{CSO1,2}} \quad \text{(eq. 4)}$$

$$R_{CSO1,2} = \frac{RATIO}{1} \times \frac{2.55}{I_{LIM1,2}} \quad \text{(eq. 5)}$$

Diagnostic in OFF state

The NCV47823 contains also circuitry for OFF state diagnostics for Short to Battery (STB) and Open Load (OL). There are internal current sources and Pull Down resistors providing additional cost savings for overall application by excluding external components and their assembly cost and saving PCB space and safe control IOs of a Microcontroller Unit (MCU). Simplified functional schematic and truth table is shown in Figure 13 and related flowchart in Figure 14.

The diagnostics in OFF state shall be performed for each channel separately. For diagnostics of Channel 1 the input CS pin has to be put logic low, for diagnostics of Channel 2 the input CS pin has to be put logic high. Corresponding EN pin has to be used for control (EN1 for Channel 1 and EN2 for Channel 2).

where

$R_{CSO1,2}$ − current limit setting resistor

$V_{CSO1,2}$ − voltage at CSO pin proportional to $I_{out1,2}$

$I_{LIM1,2}$ − current limit value

$I_{out1,2}$ − output current actual value

RATIO − typical value of Output Current to CSO Current Ratio for particular output current range

CSO pin provides information about output current actual value. The CSO voltage is proportional to output current according to (eq. 3).

Once output current reaches its limit value ($I_{LIM1,2}$) set by external resistor R_{CSO} than voltage at CSO pin is typically 2.55 V. Calculations of $I_{LIM1,2}$ or $R_{CSO1,2}$ values can be done using (eq. 6) and (eq. 7).

$$I_{LIM1,2\_min} = RATIO_{min} \times \frac{V_{CSO1,2\_min}}{R_{CSO1,2\_max}} \quad \text{(eq. 6)}$$

$$I_{LIM1,2\_max} = RATIO_{max} \times \frac{V_{CSO1,2\_max}}{R_{CSO1,2\_min}} \quad \text{(eq. 7)}$$

where:

$RATIO_{min}$ – minimum value of Output Current to CSO Current Ratio from electrical characteristics table and particular output current range

$RATIO_{max}$ – maximum value of Output Current to CSO Current Ratio from electrical characteristics table and particular output current range

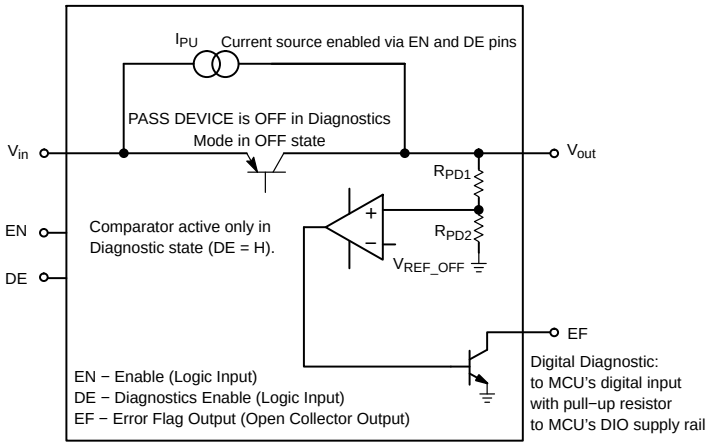
$V_{CSO1,2\_min}$ – minimum value of CSO Voltage Level at Current Limit from electrical characteristics table

$V_{CSO1,2\_max}$ – maximum value of CSO Voltage Level at Current Limit from electrical characteristics table

$R_{CSO1,2\_min}$ – minimum value of $R_{CSO1,2}$ with respect its accuracy

$R_{CSO1,2\_max}$ – maximum value of $R_{CSO1,2}$ with respect its accuracy

Designers should consider the tolerance of $R_{CSO1,2}$ during the design phase.



EN	DE	I_{PU}	EF	V_{out}	Diagnostic Status/Action
L	L	OFF	HZ	Unknown	None (Diagnostic OFF)
L	H	OFF	L	$V_{out}>V_{out\_OFF}$	Short to Battery (STB)
L	H	OFF	HZ	$V_{out}<V_{out\_OFF}$	Check for Open Load (OL)
H	H	ON	L	$V_{out}>V_{out\_OFF}$	Open Load (OL)
H	H	ON	HZ	$V_{out}<V_{out\_OFF}$	No Failure (V_{out} close to 0V)

Figure 13. Simplified Functional Diagram of OFF State Diagnostics (STB and OL)

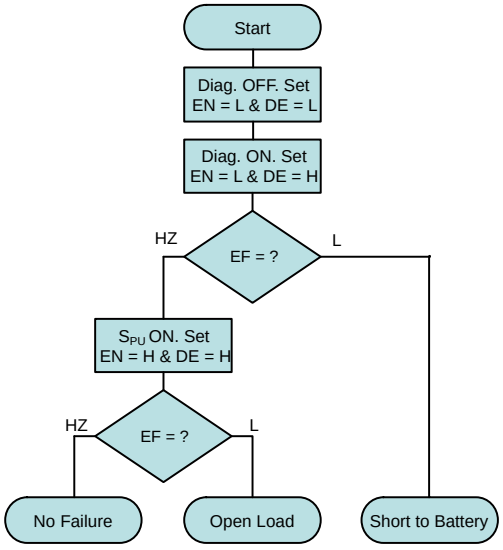


Figure 14. Flowchart for Diagnostics in OFF State

Diagnostic in ON state

Diagnostic in ON State provides information about Overcurrent or Short to Ground failures, during which the EF output is in logic low state. The diagnostics in ON state shall be performed for each channel separately. For diagnostics of Channel 1 the input CS pin has to be put logic low, for diagnostics of Channel 2 the input CS pin has to be put logic high. For detailed information see Diagnostic Features Truth Table in Table 8.

Output Voltage Monitoring

The Output Voltage net is connected to internal resistor divider. Output of the resistor divider is connected to $V_{out\_FB1,2}$ pin and provides information about Output Voltage Level according to (eq. 8).

$$V_{out\_FB1,2} = \frac{V_{out1,2}}{6} \qquad \text{(eq. 8)}$$

Table 8. DIAGNOSTIC FEATURES TRUTH TABLE

Operational Status	EN (note 10)	DE	CS	Output Channel (V_{out1} or V_{out2})	Diagnostic Output (CSO1 or CSO2)	Error Flag (EF)
Disabled	L	L	X	Low (~0 V)	Low (~0 V)	HZ
Short to Battery (OFF)	L	H	L/H (Note 13)	High(V_{out}~V_{in})	Low (~0 V)	L (Note 11)
Open Load (OFF)	H	H	L/H (Note 13)	High(V_{out}~V_{in})	Low (~0 V)	L (Note 12)
Normal (OFF)	H	H	L/H (Note 13)	Low (~0 V)	Low (~0 V)	HZ (Note 12)
Open Load (ON)	H	L	L/H (Note 13)	High(V_{out}~V_{in})	Low (~0 V)	HZ
Switch	H	L	L/H (Note 13)	I_{out}<I_{out_SET}	Proportional to I_{out} (± 5%) (Note 15)	HZ
Current Source	H	L	L/H (Note 13)	I_{out}=I_{out_SET}	High (~2.55 V)	HZ
Short to Ground	H	L	L/H (Note 13)	Low (~0 V)	High (~2.55 V)	L (Note 14)

10. State of EN pin of appropriate channel
11. Internal current source turned OFF (between V_{out} and V_{in} of appropriate channel)
12. Internal current source turned ON (between V_{out} and V_{in} of appropriate channel)
13. CS = L means CH1 diagnostics and CS = H means CH2 diagnostics (e.g. when CS = L and EF = L then failure at CH1 observed, when CS = H and EF = L then failure at CH2 observed)
14. STG is considered as fault when V_{out} < 3 V
15. Valid for I_{out} = 50 mA to 350 mA. For I_{out} = 10 mA to 50 mA range proportional to I_{out} (± 15%).

Thermal Considerations

As power in the device increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the device has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the device can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \qquad \text{(eq. 9)}$$

Since T_J is not recommended to exceed 150°C, then the device soldered on 645 mm^2, 1 oz copper area, FR4 can dissipate up to 2.38 W when the ambient temperature (T_A) is 25°C. See Figure 15 for $R_{\theta JA}$ versus PCB area. The power dissipated by the device can be calculated from the following equations:

$$P_D \approx V_{in}\left(I_q @ I_{out1,2}\right) + I_{out1}\left(V_{in} - V_{out1}\right) + I_{out2}\left(V_{in} - V_{out2}\right) \qquad \text{(eq. 10)}$$

or

$$V_{in(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{out1} \times I_{out1}\right) + \left(V_{out2} \times I_{out2}\right)}{I_{out1} + I_{out2} + I_q} \qquad \text{(eq. 11)}$$

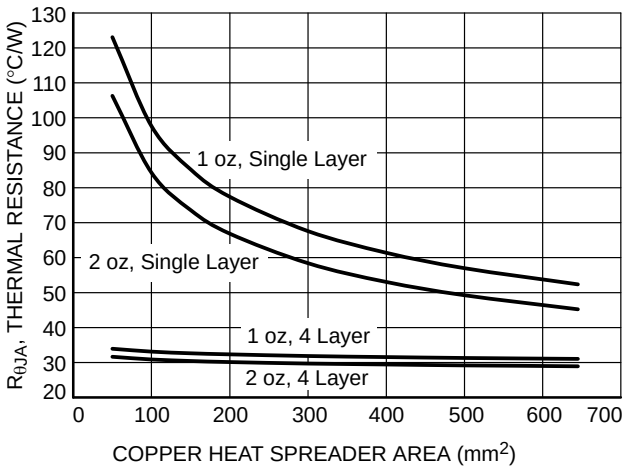


Figure 15. Thermal Resistance vs. PCB Copper Area

Hints

V_{in} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the device and make traces as short as possible.

The Output Voltage Monitoring Output is high impedance output (see Figure 2) and during OFF state diagnostics it may be prone to couple a noise via PCB track or wire. Disturbing may appear as Error Flag Output oscillation when Output Voltage Level is close to Short to Battery threshold. To improve robustness connect capacitor (typically 10 nF) between each $V_{out\_FB1,2}$ pin and GND as close as possible to the $V_{out\_FB1,2}$ pins.

The Current Sense Output is internally connected to an input of error amplifier and may be prone to couple a noise via long PCB track or wire (e.g. connection to an ADC). In case of long PCB track or wire connected to CSO pin it is recommended to use RC filter for noise suppression (see Figure 16 and Table 9) in cost of higher inrush current. The R value of the RC filter can be higher than value listed in Table 9, depending on acceptable of RC time constant. The higher is R value the lower is inrush current. Value of C = 10 nF is optimized for noise suppression and as low as possible inrush current.

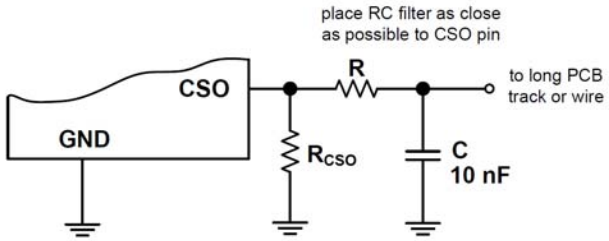


Figure 16. RF Filter Connection

Table 9. INRUSH CURRENT AND RECOMMENDED RC VALUES

(Test Conditions: V_{in} = 13.5 V, V_{out} = short to GND, V_{EN} = pulse from 0 V to 5 V)

Rcso (kΩ)	Calculated Current Limit (mA) (Note 16)	Inrush Current without RC (mA)	minimum R (kΩ)	C (nF)	Inrush Current with RC (mA) with minimum R
68	11	75	22	10	65
15	51	108	22	10	124
8.2	93	133	33	10	145
5.1	150	159	33	10	182
3.9	183	211	33	10	231
3.3	216	248	33	10	270
2.7	264	308	22	10	338
2.2	325	376	15	10	415

16. Calculated ILIM is for Vout = Vin − 1 V.

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCV47823PAAJR2G	Line1: NCV4 Line2: 7823	TSSOP−14 EP (Pb−Free)	2500 / Tape & Reel

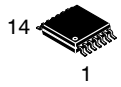
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

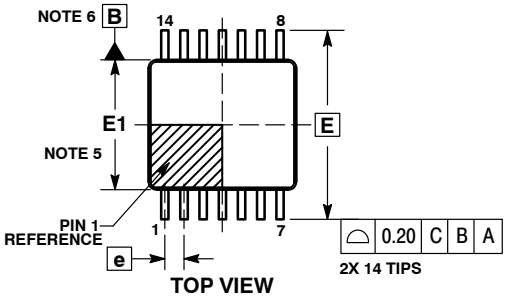
ON Semiconductor®

TSSOP−14 EP
CASE 948AW
ISSUE C

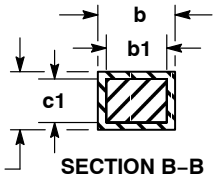
DATE 09 OCT 2012



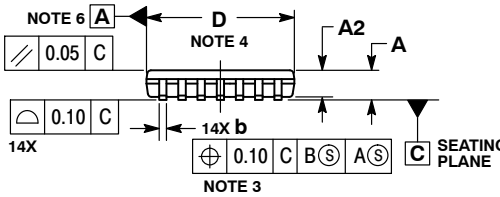
SCALE 1:1



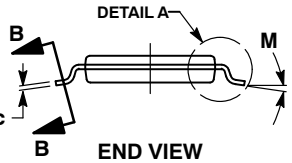
TOP VIEW



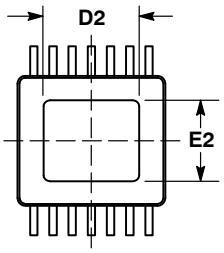
SECTION B−B
NOTE 8



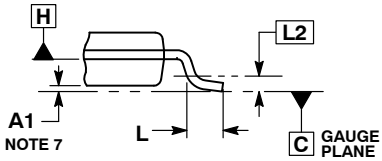
SIDE VIEW



END VIEW



BOTTOM VIEW

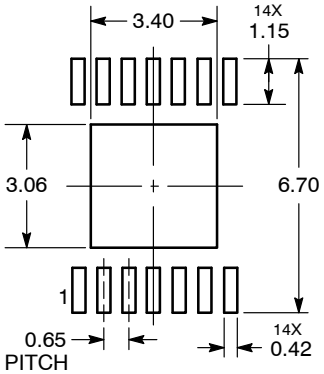


DETAIL A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.07 mm MAX. AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION D IS DETERMINED AT DATUM H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM H.
6. DATUMS A AND B ARE DETERMINED AT DATUM H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. SECTION B−B TO BE DETERMINED AT 0.10 TO 0.25 mm FROM THE LEAD TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	----	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
b1	0.19	0.25
c	0.09	0.20
c1	0.09	0.16
D	4.90	5.10
D2	3.09	3.62
E	6.40 BSC	
E1	4.30	4.50
E2	2.69	3.22
e	0.65 BSC	
L	0.45	0.75
L2	0.25 BSC	
M	0 °	8 °

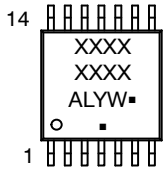
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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