NCP3066, NCV3066

Constant Current Buck Boost Inverting Switching Regulator for HB-LEDs with Enable

1.5 A

The NCP3066 is a monolithic switching regulator designed to deliver constant current for powering high brightness LEDs. The device has a very low feedback voltage of 235 mV (nominal) which is used to regulate the average current of the LED string. In addition, the NCP3066 has a wide input voltage up to 40 V to allow it to operate from a 12 Vac or a 12−36 Vdc supply, commonly used for lighting applications as well as unregulated supplies such as rechargeable batteries. The NCP3066 switching regulator can be configured in Step−Down (Buck), Step−Up (Boost) and Voltage−Inverting topologies with a minimum number of external components. The ON/$\overline{\text{OFF}}$ pin provides PWM dimming capability or a low power shutdown mode.

Features

- Integrated 1.5 A Switch
- Input Voltage Range from 3.0 V to 40 V
- Logic Level Shutdown Capability
- Low Feedback Voltage of 235 mV
- Cycle−by−Cycle Current Limit
- No Control Loop Compensation Required
- Frequency of Operation Adjustable up to 250 kHz
- Analog and Digital PWM Dimming Capability
- Internal Thermal Shutdown with Hysteresis
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes
- These are Pb−Free Devices

Applications

- Automotive and Marine Lighting
- Constant Current Source, High Brightness LED Driver
- Low Voltage and Landscape Lighting

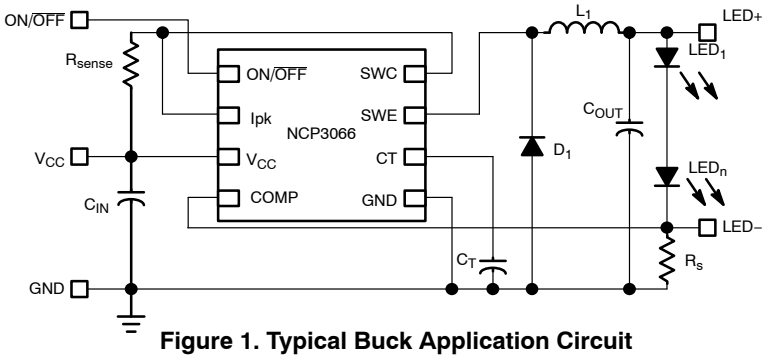

Figure 1. Typical Buck Application Circuit

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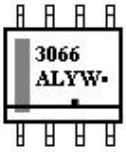
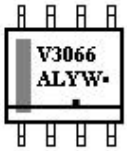
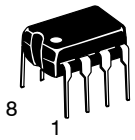
MARKING DIAGRAMS

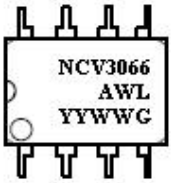
SOIC−8
D SUFFIX
CASE 751

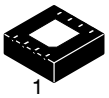






PDIP−8
P, P1 SUFFIX
CASE 626





DFN8
MN SUFFIX
CASE 488AF

NCP3066	=	Specific Device Code
A	=	Assembly Location
L, WL	=	Wafer Lot
Y, YY	=	Year
W, WW	=	Work Week
G or ▪	=	Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 17 of this data sheet.

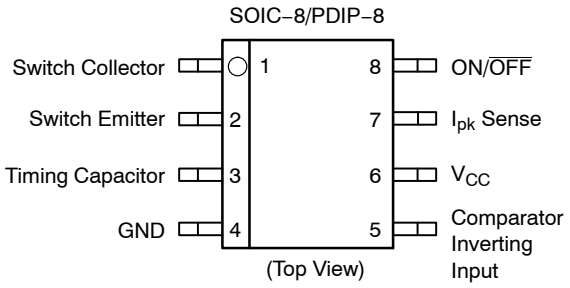
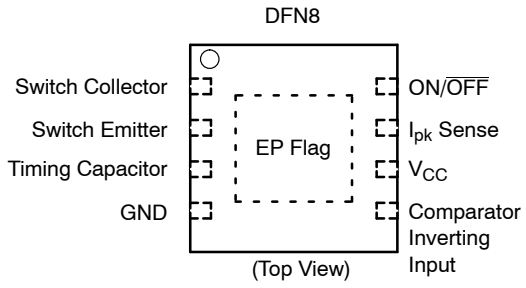


Figure 2. Pin Connections



NOTE: EP Flag must be tied to GND Pin 4 on PCB

Figure 3. Pin Connections

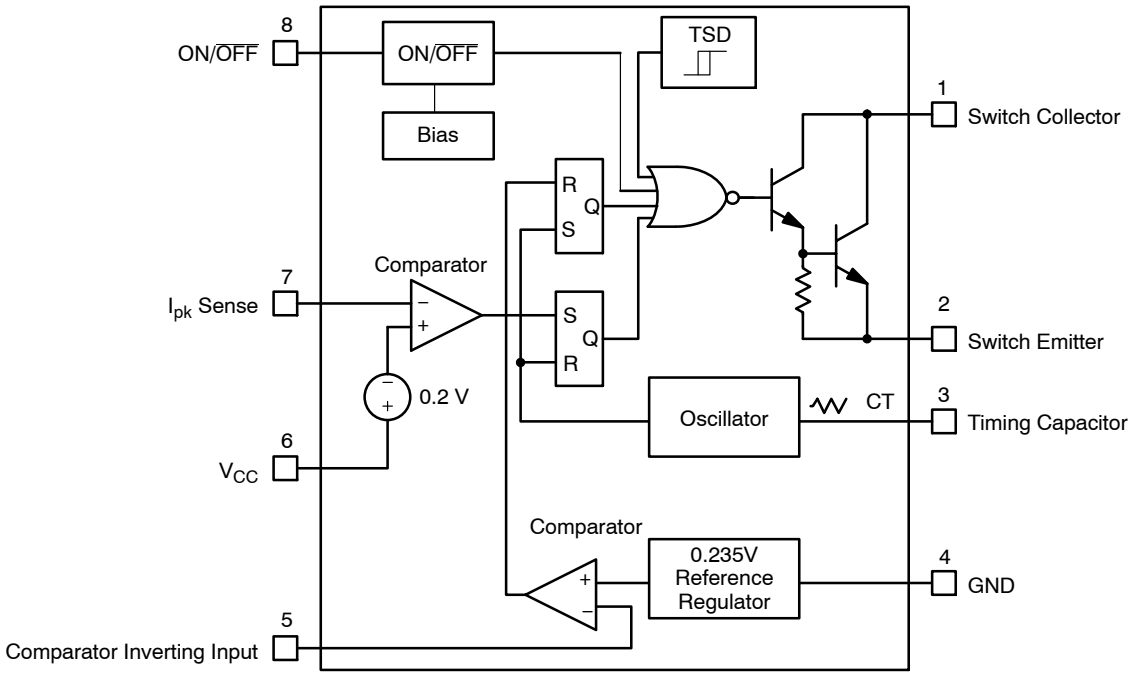


Figure 4. Block Diagram

PIN DESCRIPTION

Pin No.		Pin Name	Description
PDIP8	DFN8		
1	1	Switch Collector	Internal Darlington switch collector.
2	2	Switch Emitter	Internal Darlington switch emitter.
3	3	Timing Capacitor	Timing Capacitor to control the switching frequency.
4	4, EP Flag	GND	Ground pin for all internal circuits.
5	5	Comparator Inverting Input	Inverting input pin of internal comparator.
6	6	V_{CC}	Voltage Supply
7	7	I_{pk} Sense	Peak Current Sense Input to monitor the voltage drop across an external resistor to limit the peak current through the circuit.
8	8	ON/$\overline{OFF}$	ON/$\overline{OFF}$ Pin. To disable the device, this input should be pulled below 0.8 V. If the pin is left floating, it will be disabled.

MAXIMUM RATINGS (measured vs. Pin 4, unless otherwise noted)

Rating	Symbol	Value	Unit
VCC Pin 6	V_{CC}	0 to +42	V
Comparator Inverting Input Pin 5	V_{CII}	−0.3 to + V_{CC}	V
Darlington Switch Collector Pin 1	V_{SWC}	−0.3 to + 42	V
Darlington Switch Emitter Pin 2 (Transistor OFF)	V_{SWE}	−0.6 to + V_{CC}	V
Darlington Switch Collector to Emitter Pins 1−2	V_{SWCE}	−0.3 to + 42	V
Darlington Switch Current	I_{SW}	1.5	A
I_{pk} Sense Pin 7	V_{IPK}	−0.3 to V_{CC}+ 0.3	V
Timing Capacitor Pin Voltage (Pin 3)	V_{TC}	−0.2 to +1.4	V
Moisture Sensitivity Level	MSL	1	–
Lead Temperature Soldering	T_{SLD}	260	°C
ON/$\overline{OFF}$ Pin voltage	$V_{ON/OFF}$	(−0.3 to +25) < V_{CC}	V

POWER DISSIPATION AND THERMAL CHARACTERISTICS

PDIP−8 (Note 5) Thermal Resistance Junction−to−Air	$R_{\theta JA}$	100	°C/W
SOIC−8 (Note 5) Thermal Resistance Junction−to−Air	$R_{\theta JA}$	180	°C/W
DFN−8 (Note 5) Thermal Resistance Junction−to−Air Thermal Resistance Junction−to−Case	 $R_{\theta JA}$ $R_{\theta JC}$	 78 14	°C/W
Storage Temperature Range	T_{STG}	−65 to +150	°C
Maximum Junction Temperature	T_{JMAX}	+150	°C
Operating Junction Temperature Range (Note 3) NCP3066 NCV3066	T_J	 0 to +85 −40 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Pin 1−8: Human Body Model 2000 V per AEC Q100−002; 003 or JESD22/A114; A115
   Machine Model Method 200 V
2. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.
3. The relation between junction temperature, ambient temperature and Total Power dissipated in IC is $T_J = T_A + R_\theta \bullet P_D$.
4. The pins which are not defined may not be loaded by external signals.
5. 35 μm copper, 10 cm^2 copper area.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, −40°C < T_J < +125°C for NCV3066, 0°C < T_J < +85°C for NCP3066 unless otherwise specified)

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
OSCILLATOR						
f_{OSC}	Frequency	(V_{Pin5} = 0 V, C_T = 2.2 nF, T_J = 25°C)	110	150	190	kHz
I_{DISCHG}/I_{CHG}	Discharge to Charge Current Ratio	(Pin 7 to V_{CC}, T_J = 25°C)	5.5	6.0	6.5	–
I_{DISCHG}	Capacitor Discharging Current	(Pin 7 to V_{CC}, T_J = 25°C)		1650		μA
I_{CHG}	Capacitor Charging Current	(Pin 7 to V_{CC}, T_J = 25°C)		275		μA
$V_{IPK(Sense)}$	Current Limit Sense Voltage	(T_J = 25°C) (Note 7)	165	200	235	mV
OUTPUT SWITCH (Note 6)						
$V_{SWCE(DROP)}$	Darlington Switch Collector to Emitter Voltage Drop	(I_{SW} = 1.0 A, T_J = 25°C) (Note 6)		1.0	1.3	V
$I_{C(OFF)}$	Collector Off−State Current	(V_{CE} = 40 V)		1.0	10	μA
COMPARATOR						
V_{TH}	Threshold Voltage	T_J = 25°C		235		mV
		T_J = 0°C to 85°C	−5%	235	+5%	
		T_J = −40°C to +125°C	−10%	235	+10%	
REG_{LiNE}	Threshold Voltage Line Regulation	(V_{CC} = 3.0 V to 40 V)	−6.0	2.0	6.0	mV
$I_{CII\ in}$	Input Bias Current	(V_{in} = V_{th})	−1000	−100	1000	nA
ON/OFF FEATURE						
V_{IH}	ON/$\overline{OFF}$ Pin Logic Input Level High V_{OUT} = 0 V	T_J = 25°C T_J = 0°C to +85°C	2.2 2.4	– –	– –	V
V_{IL}	ON/$\overline{OFF}$ Pin Logic Input Level Low V_{OUT} = Nominal Output Voltage	$_J$ = 25°C T_J = 0°C to +85°C	– –	– –	1.0 0.8	V
I_{IH}	ON/$\overline{OFF}$ Pin Input Current ON/$\overline{OFF}$ Pin = 5 V (ON)	T_J = 25°C		15		μA
I_{IL}	ON/$\overline{OFF}$ Pin Input Current ON/$\overline{OFF}$ Pin = 0 V (OFF)	T_J = 25°C		1.0		μA
T_{ON_MIN}	ON/OFF Pin Minimum Width	T_J = 25°C		50		μs
TOTAL DEVICE						
I_{CC}	Supply Current	(V_{CC} = 5.0 V to 40 V, CT = 2.2 nF, Pin 7 = V_{CC}, V_{Pin} 5 > V_{th}, Pin 2 = GND, remaining pins open)			7.0	mA
I_{STBY}	Standby Quiescent Current	ON/$\overline{OFF}$ Pin = 5.0 V (OFF) T_J = 25°C T_J = −40°C to +125°C		85	 120 120	μA
T_{SHD}	Thermal Shutdown Threshold			160		°C
T_{SHDHYS}	Hysteresis			10		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
7. The V_{IPK} (Sense) Current Limit Sense Voltage is specified at static conditions. In dynamic operation the sensed current turn−off value depends on comparator response time and di/dt current slope. See the Operating Description section for details.
8. NCV prefix is for automotive and other applications requiring site and change control and extended operating temperature conditions.

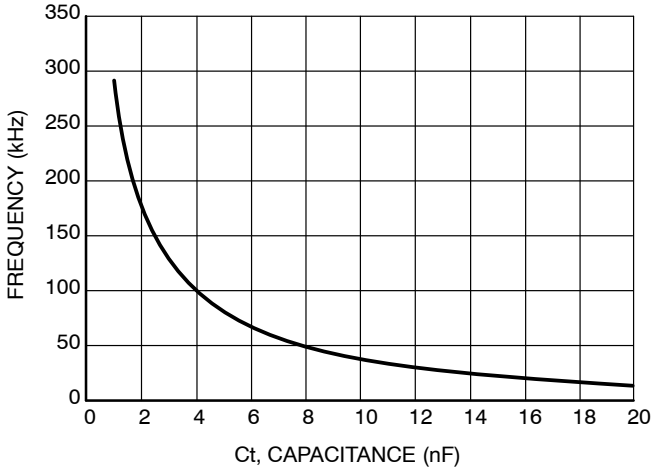


Figure 5. Oscillator Frequency vs. Timing Capacitor

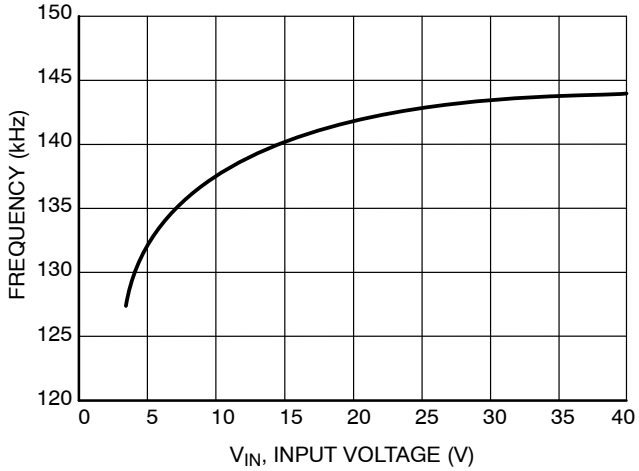


Figure 6. Oscillator Frequency vs. Supply Voltage

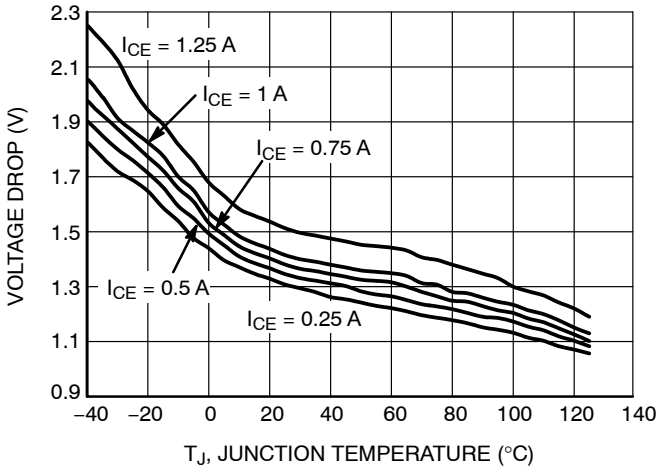


Figure 7. Voltage Drop in Emitter Follower Configuration

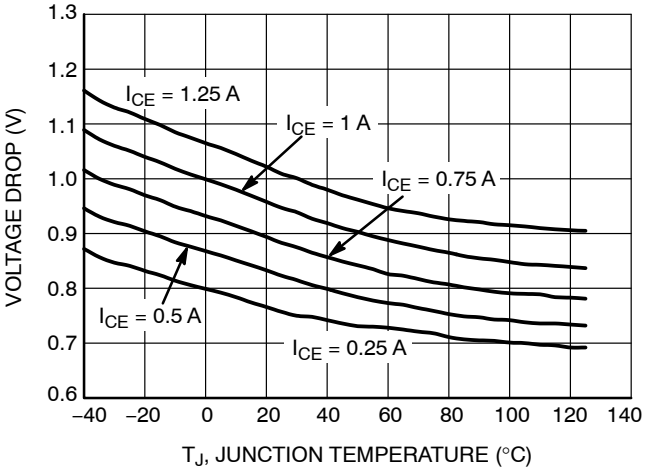


Figure 8. Common Emitter Configuration Output Darlington Switch Voltage Drop vs. Temperature

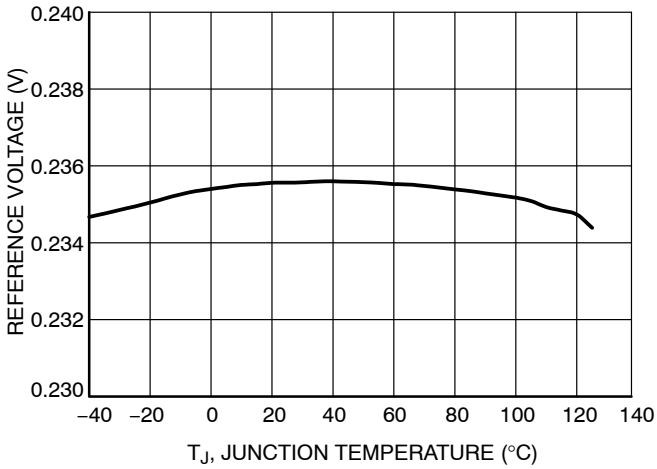


Figure 9. V_{th} vs. Temperature

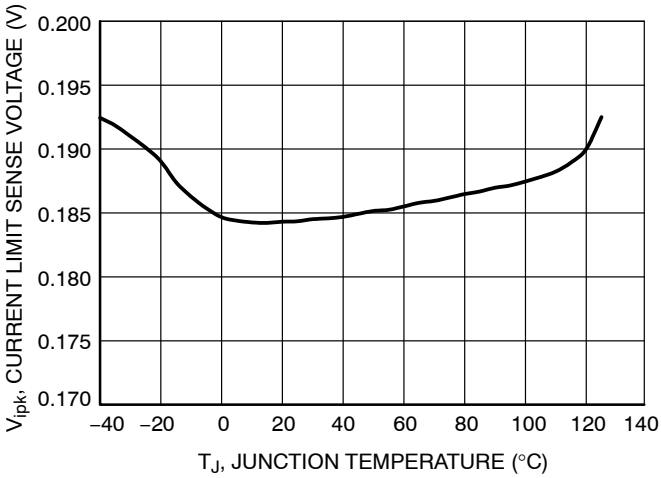


Figure 10. Current Limit Sense Voltage vs. Temperature

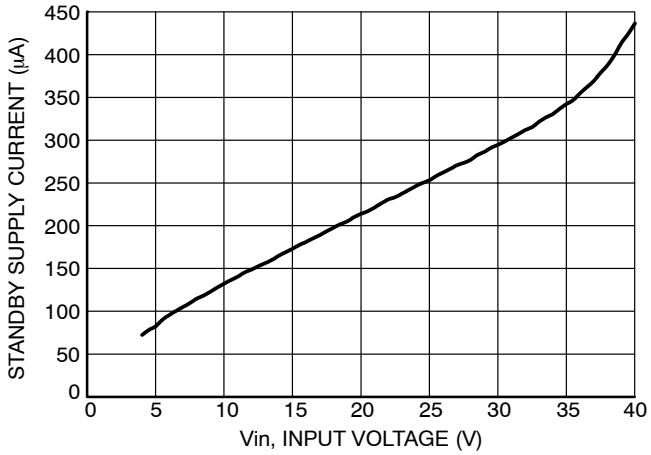


Figure 11. Standby Supply Current vs. Supply Voltage

INTRODUCTION

The NCP3066 is a monolithic power switching regulator optimized for LED Driver applications. Its flexible architecture enables the system designer to directly implement step−up, step−down, and voltage−inverting converters with a minimum number of external components for driving LEDs. A representative block diagram is shown in Figure 3.

Operating Description

The NCP3066 operates as a fixed oscillator frequency output voltage ripple gated regulator. In general, this mode of operation is somewhat analogous to a capacitor charge pump and does not require dominant pole loop compensation for converter stability. The typical operating waveforms are shown in Figure 12. The output voltage waveform is shown for a step−down converter with the ripple and phasing exaggerated for clarity. During initial converter startup, the feedback comparator senses that the output voltage level is below nominal. This causes the output switch to turn on and off at a frequency and duty cycle controlled by the oscillator, thus pumping up the output filter capacitor. When the output voltage level reaches nominal comparator value, the output switch cycle is inhibited. When the load current causes the output voltage to fall below the nominal value feedback comparator enables switching immediately. Under these conditions, the output switch conduction can be enabled for a partial oscillator cycle, a partial cycle plus a complete cycle, multiple cycles, or a partial cycle plus multiple cycles.

Oscillator

The oscillator frequency and off−time of the output switch are programmed by the value of the timing capacitor C_T. The capacitor C_T is charged and discharged by a 1 to 6 ratio internal current source and sink, generating a positive going sawtooth waveform at Pin 3. This ratio sets the maximum $t_{ON}/(t_{ON} + t_{OFF})$ of the switching converter as 6/(6+1) or 85.7% (typical). The oscillator peak and valley voltage difference is 500 mV typically. To calculate the C_T capacitor value for required oscillator frequency, use the equations found in Figure 15. An online NCP3066 design tool can be found at www.onsemi.com, which aids in selecting component values.

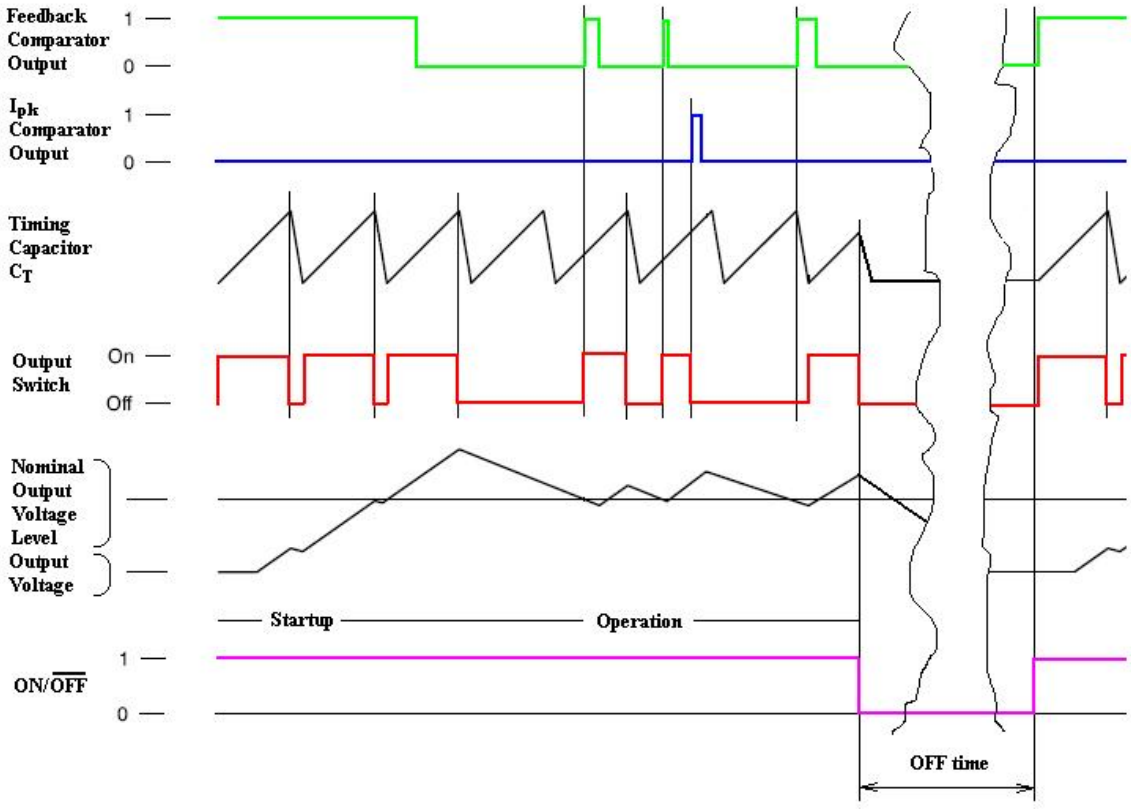


Figure 12. Typical Operating Waveforms

Peak Current Sense Comparator

Under normal conditions, the output switch conduction is initiated by the Voltage Feedback comparator and terminated by the oscillator. Abnormal operating conditions occur when the converter output is overloaded or when feedback voltage sensing is lost. Under these conditions, the I_{pk} Current Sense comparator will protect the Darlington output Switch. The switch current is converted to a voltage by inserting a fractional ohm resistor, R_{Sense}, in series with V_{CC} and Darlington output switch. The voltage drop across R_{Sense} is monitored by the Current Sense comparator. If the voltage drop exceeds 200 mV (nom) with respect to V_{CC}, the comparator will set the latch and terminate the output switch conduction on a cycle−by−cycle basis.

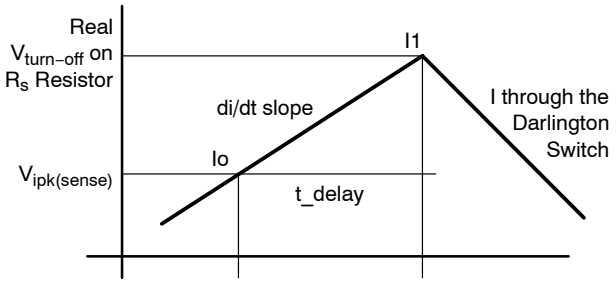


Figure 13. Current Sense Waveform

The $V_{IPK(Sense)}$ Current Limit Sense Voltage threshold is specified at static conditions. In dynamic operation the sensed current turn−off value depends on comparator response time and di/dt current slope.

Real $V_{turn-off}$ on R_{sc} resistor

$V_{turn\_off} = V_{ipk(sense)} + R_{Sense}*(t_{delay}*di/dt)$

Typical I_{pk} comparator response time t_{delay} is 350 ns. The di/dt current slope is dependent on the voltage difference across the inductor and the value of the inductor. Increasing the value of the inductor will reduce the di/dt slope.

It is recommended to verify the actual peak current in the application at worst conditions to be sure that the max peak current will never get over the 1.5 A Darlington Switch Current max rating.

Thermal Shutdown

Internal thermal shutdown circuitry is provided to protect the IC in the event that the maximum junction temperature is exceeded. When activated, typically at 160°C, the Darlington Output Switch is disabled. The temperature sensing circuit is designed with some hysteresis. The Darlington Switch is enabled again when the chip temperature decreases under the low threshold. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a replacement for proper heatsinking.

Output Switch

The output switch is designed in Darlington configuration. This allows the application designer to operate at all conditions at high switching speed and low voltage drop. The Darlington Output Switch is designed to switch a maximum of 40 V collector to emitter voltage and current up to 1.5 A.

ON/OFF Function

The ON/$\overline{\text{OFF}}$ function provides interruption of switching and puts the circuitry into the low consumption mode. This feature is applicable for digital dimming of the LEDs as well. The ON/OFF signal inhibits switching of the regulator and reduces the average current through the LEDs. The frequency of this pulse width−modulated signal with the duty cycle can range from less than 1% to 100% is limited by the value of 1 kHz.

Pulling this pin below 0.8 V or leaving it opened turns the regulator off. In this state the consumption of the device is reduced below 100 uA. Pulling this pin above 2.4 V (up to max. 25 V) allows the regulator running in normal state. If the ON/$\overline{\text{OFF}}$ feature is not needed, the ON/$\overline{\text{OFF}}$ pin can be wired to V_{CC}, provided this voltage does not exceed 25 V.

No Output Capacitor Operation

A traditional buck topology includes an inductor followed by an output capacitor which filters the ripple. The capacitor is placed in parallel with the LED or array of LEDs to lower the ripple current. A constant current buck regulator such as the NCP3066 focuses on the control of the current through the load, not the voltage across it. The switching frequency of the NCP3066 is in the range of 100−250 kHz which is much higher than the human eye can detect. By configuring the NCP3066 in a continuous conduction buck configuration with low peak to peak ripple the output filter capacitor can be eliminated. The important design parameter is to keep the peak current below the maximum current rating of the LED. Using 15−40% peak to peak ripple results in a good compromise between achieving max average output current without exceeding the maximum limit. This saves space and reduces part count for applications.

APPLICATIONS

Figures 15 through 24 show the simplicity and flexibility of the NCP3066. Two main converter topologies are demonstrated with actual test data shown below each of the circuit diagrams. The demo boards have an input for a digital dimming signal. You can provide a PWM signal to change the average output current and reduce the LED brightness. Figure 14 gives the relevant design equations for the key parameters. Additionally, a complete application design aid for the NCP3066 can be found at www.onsemi.com.

Parameter	Step−Down	Step−Up
$\left(\frac{t_{on}}{t_{off}}\right)$	$\frac{V_{out} + V_F}{V_{in} - V_{SWCE} - V_{out}}$	$\frac{V_{out} + V_F - V_{in}}{V_{in} - V_{SWCE}}$
t_{on}	$\frac{\frac{t_{on}}{t_{off}}}{f \times \left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f \times \left(\frac{t_{on}}{t_{off}} + 1\right)}$
C_T	$C_T = \frac{381.6 \cdot 10^{-6}}{f_{osc}} - 343 \times 10^{-12}$	
$I_{L(avg)}$	I_{out}	$I_{out} \times \left(\frac{t_{on}}{t_{off}} + 1\right)$
$I_{pk\ (Switch)}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$
R_{SC}	$\frac{0.20}{I_{pk\ (Switch)}}$	$\frac{0.20}{I_{pk\ (Switch)}}$
L	$\left(\frac{V_{in} - V_{SWCE} - V_{out}}{\Delta I_L}\right) \times t_{on}$	$\left(\frac{V_{in} - V_{SWCE}}{\Delta I_L}\right) \times t_{on}$
$V_{ripple(pp)}$	$\Delta I_L \sqrt{\left(\frac{1}{8 f C_O}\right)^2 + (ESR)^2}$	$\frac{t_{on}\, I_{out}}{C_O} + \Delta I_L \times ESR$
I_{out}	$\frac{V_{ref}}{R_s}$	$\frac{V_{ref}}{R_s}$

9. V_{SWCE} − Darlington Switch Collector to Emitter Voltage Drop, refer to Figures 7 and 8.
10. V_F − Output rectifier forward voltage drop. Typical value for 1N5819 Schottky barrier rectifier is 0.4 V.
11. The calculated t_{on}/t_{off} must not exceed the minimum guaranteed oscillator charge to discharge ratio.

Figure 14. Design Equations

The Following Converter Characteristics Must Be Chosen:

V_{in} − Nominal operating input voltage.

V_{out} − Desired output voltage.

I_{out} − Desired output current.

ΔI_L − Desired peak−to−peak inductor ripple current. For maximum output current it is suggested that ΔI_L be chosen to be less than 10% of the average inductor current $I_{L(avg)}$. This will help prevent $I_{pk\ (Switch)}$ from reaching the current limit threshold set by R_{SC}. If the design goal is to use a minimum inductance value, let $\Delta I_L = 2(I_{L(avg)})$. This will proportionally reduce converter output current capability.

f − Maximum output switch frequency.

$V_{ripple(pp)}$ − Desired peak−to−peak output ripple voltage. For best performance the ripple voltage should be kept to a low value since it will directly affect line and load regulation. Capacitor C_O should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

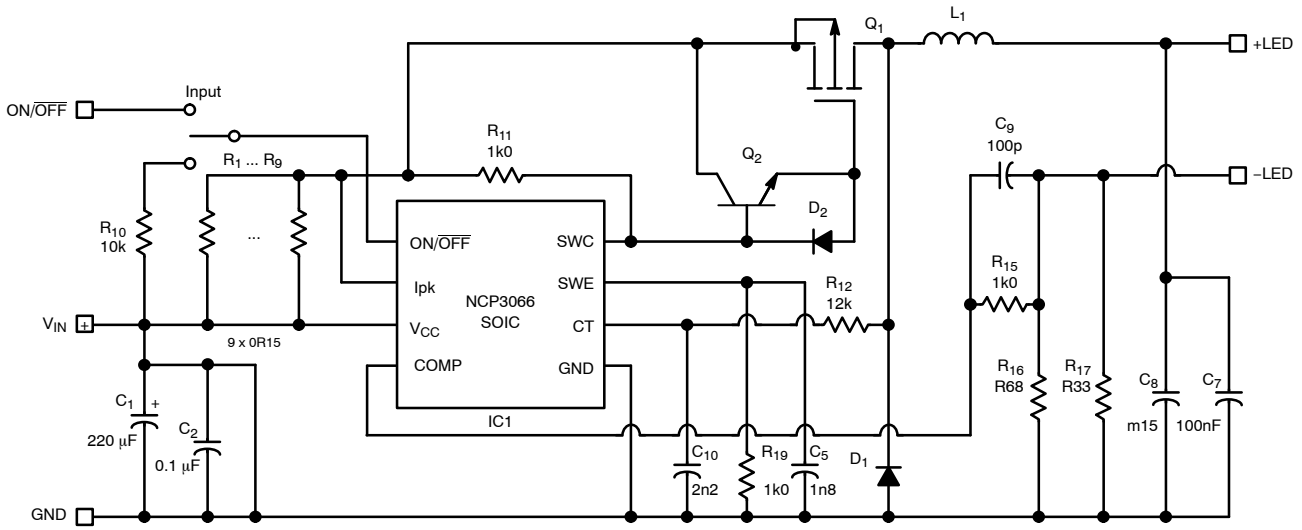


Figure 15. Buck Demoboard with External Switch Application Schematic

Table 1. BILL OF MATERIALS

Desig-nator	Qty	Description	Value	Toler-ance	Footprint	Manufacturer	Manufacturer Part Number
R1;R2; R3;R4	4	Resistor	0.15R	1%	1206	Susumu	RL1632R-R150-F
R10	1	Resisitor	10k	1%	1206	Rohm	MCR18EZHF1002
R11; R15	2	Resisitor	1k	1%	1206	Rohm	MCR18EZPF1001
R12	NU	Resistor	12k	1%	1206	Rohm	MCR18EZHF1202
R16	1	Resistor	0.68R	5%	1210	Panasonic - ECG	ERJ-14RQJR68U
R17	OPTION	Resistor	0.33R	5%	1210	Panasonic - ECG	ERJ-14RQJR33U
R19	1	Resistor	1k	5%	1210	Panasonic - ECG	ERJ-14YJ102U
C1	1	Capacitor	220µF/35V	20%	10x12.5	Panasonic	EEUFC1V221
C2;C7	2	Capacitor	100nF	10%	1206	Kemet	C1206C104K5RACTU
C5	1	Capacitor	1.8nF	10%	1206	Kemet	C1206C182K5RACTU
C8	1	Capacitor	150µF/16V	20%	F8	SANYO	16SP150M
C9	1	Capacitor	100pF	10%	1206	Vishay/Vitramon	VJ1206Y101KXEAT5Z
C10	1	Capacitor	2.2nF	10%	1206	Kemet	C1206C222K5RACTU
Q1	1	Power MOSFET –25A, -30V	NTD18P03L	-	DPAK	ON Semiconductor	NTD18P03L
Q2	1	Switching NPN Transistor	MMBT489LT1G	-	SOT-23	ON Semiconductor	MMBT489LT1G
D2	1	1A, 30V Schottky Rectifier	MBR130T1G	-	SOD123	ON Semiconductor	MBR130T1G
IC1	1	Switching Regulator	NCP3066DR2G	-	SOIC-8	ON Semiconductor	NCP3066DR2G
D1	1	3A, 30V Schottky Rectifier	MBRS330T3G	-	SMC	ON Semiconductor	MBRS330T3G
L1	1	Inductor	47 µH	20%	Wurth Elektronik	Wurth Elektronik	WE–PD4 74457147

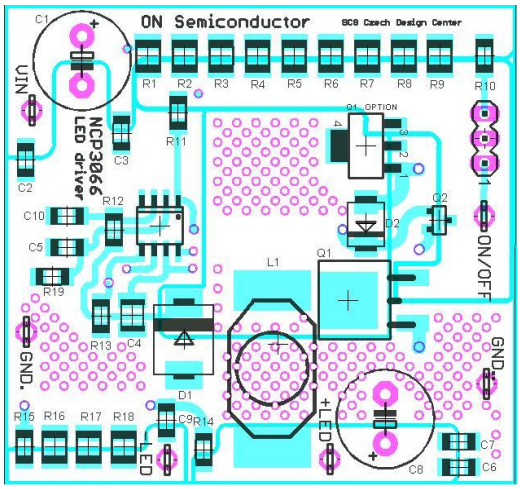


Figure 16. Buck with External Switch Demoboard Layout

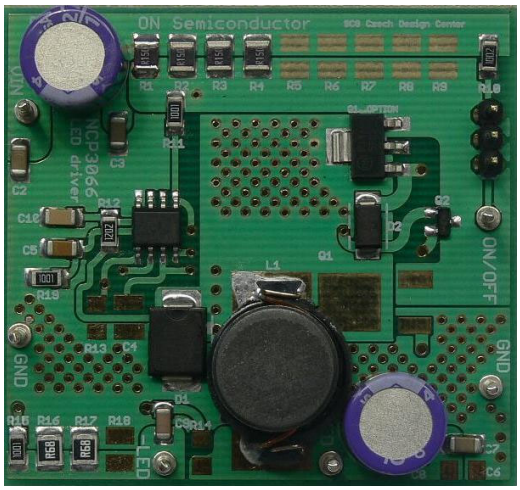


Figure 17. Buck with External Switch Demoboard Photo

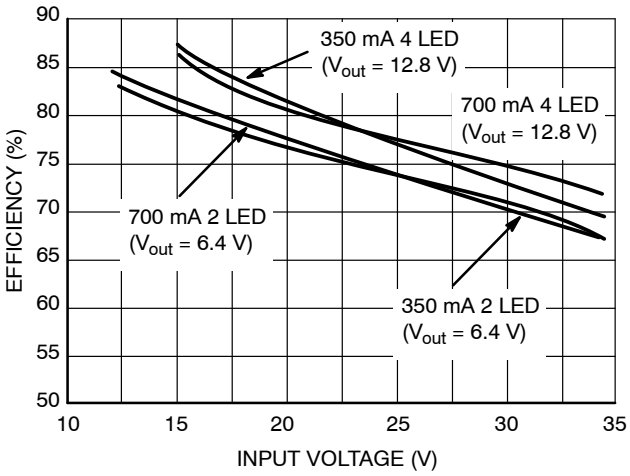


Figure 18. Efficiency of Buck LED Driver

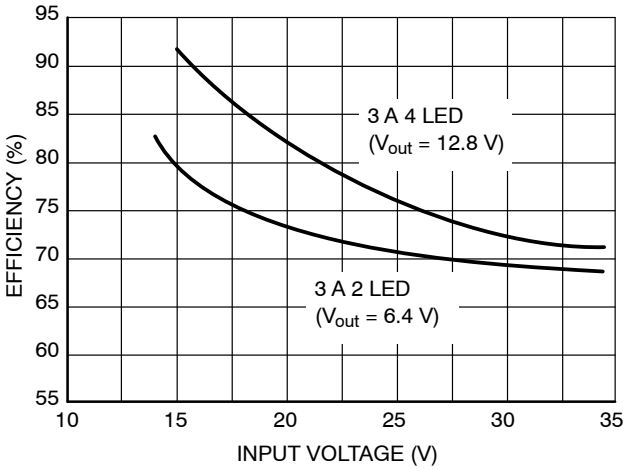


Figure 19. Efficiency of Buck LED Driver at I_{out} = 3 A

Figure 15, Buck Demoboard With External Switch Application Schematic illustrates the NCP3066 being used as a PFET controller. Table 1. Bill Of Materials shows the small number of additional parts which are necessary to assemble mentioned demoboard. The demoboard based on two layer PCB and the layout is mentioned in Figure 16. Buck Demoboard Layout. The Line regulation is mentioned in Figure 20, Line Regulation. The Figure 21, Dimming characteristic shows behavior of circuitry in case the square wave signal with 5 V amplitude and 300 Hz frequency was delivered into ON/OFF pin of device.

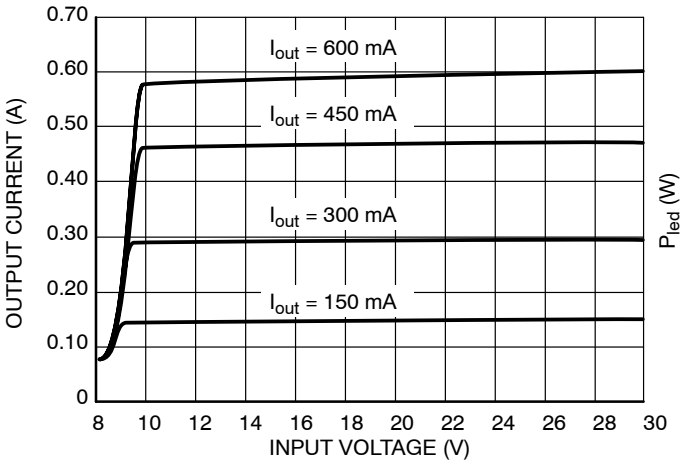


Figure 20. Line Regulation

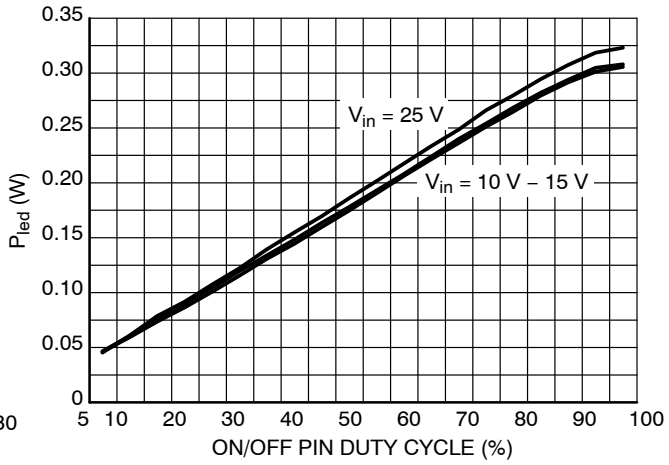


Figure 21. Dimming Characteristic

Table 2. TEST RESULTS

Line Regulation	Vin = 12 V to 35 V, Iout = 3000 mA	250 mA
Output Ripple	Vin = 12 V, Iout = 3000 mA	320 mA
Efficiency	Vin = 12 V, Iout = 3000 mA	80%

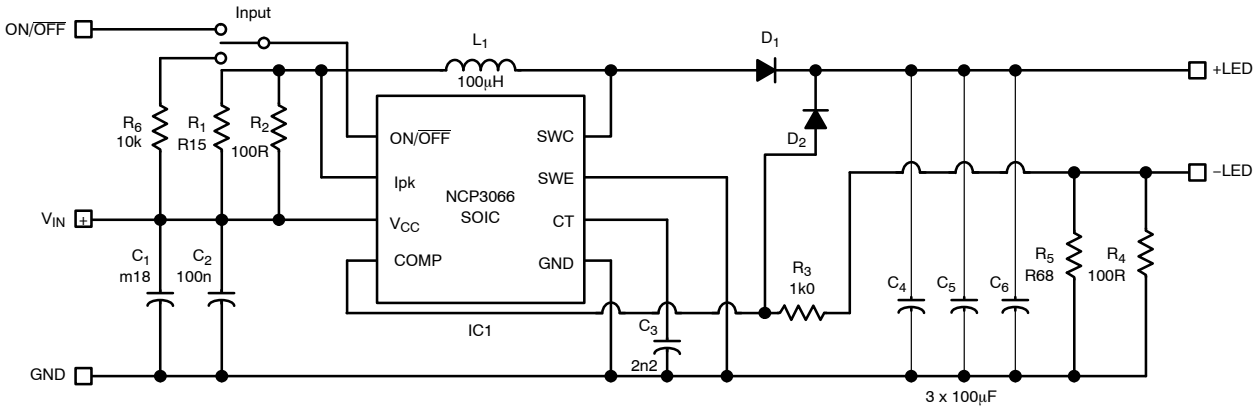


Figure 22. Boost demoboard Application Schematic

Table 3. BILL OF MATERIALS

Designator	Qty	Description	Value	Toler-ance	Foot-print	Manufacturer	Manufacturer Part Number
R1	1	Resistor	0.15R	1%	1206	Susumu	RL1632R-R150-F
R2;R4	NU	Resisitor	100R	1%	1206	Vishay/Dale	CRCW1206100RFKEA
R3	1	Resisitor	1k	1%	1206	Rohm	MCR18EZPF1001
R5	1	Resistor	0.68R	5%	1210	Panasonic - ECG	ERJ-14RQJR68U
R6	1	Resistor	10k	1%	1206	Rohm	MCR18EZHF1002
C1	1	Capacitor	180μF	20%	F8	SANYO	16SVPS180M
C2	1	Capacitor	100nF	10%	1206	Kemet	C1206C104K5RACTU
C3	1	Capacitor	2.2nF	10%	1206	Kemet	C1206C222K5RACTU
C4,C5,C6	3	Capacitor	100μF	20%	1210	TDK	C4532Y5V1A107Z
C10	1	Capacitor	2.2nF	10%	1206	Kemet	C1206C222K5RACTU
IC1	1	Switching Regulator	NCP3066DR2G	-	SOIC-8	ON Semiconductor	NCP3066DR2G
D1	1	Diode	MBRS1540T3G	-	SMB	ON Semiconductor	MBRS1540T3G
D2	1	Zener Diode	BZX84B18VLT1G	-	SOT-23	ON Semiconductor	BZX84B18VLT1G
L2	1	Inductor	100μH	20%	Coilcraft	Coilcraft	DO3316P-104MLB

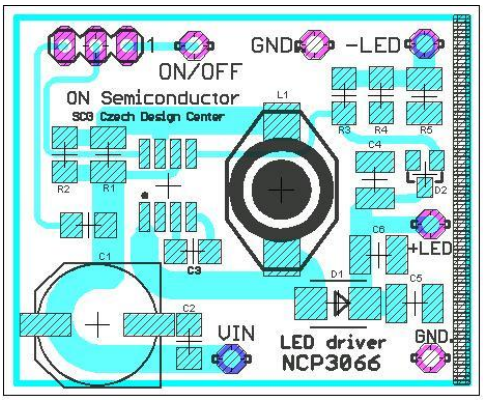


Figure 23. Boost Demoboard Layout

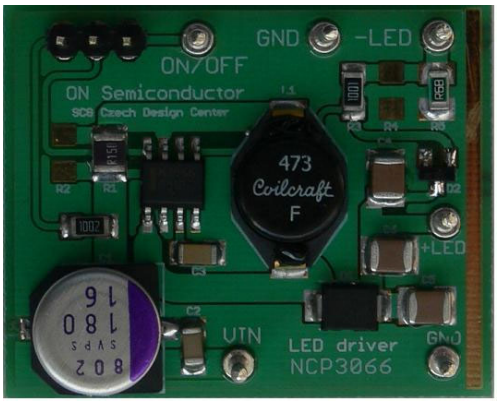


Figure 24. Boost Demonstration Photo

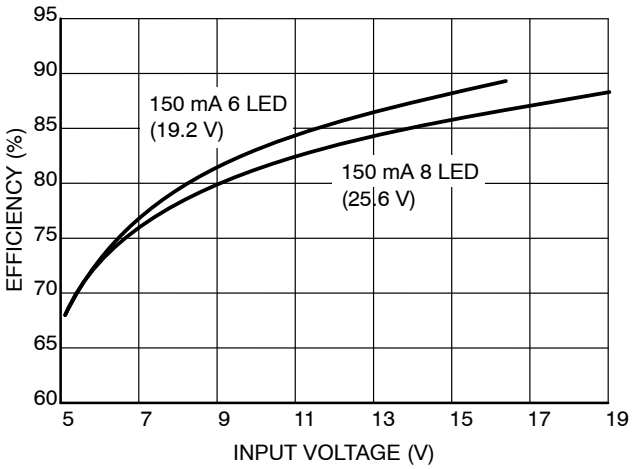


Figure 25. Boost LED Driver Efficiency

Figure 22, Boost Demoboard Application Schematic, illustrates the basic circuitry in boost topology, which allows supplying string up to eight LEDs up to 150 mA consumption. Table 3, Bill of Materials shows the small number of additional parts which are necessary to assembly mentioned demoboard. The demoboard based on one layer PCB and the layout is shown in Figure 23, Buck Demoboard Layout. The photo of this demoboard is mentioned in Figure 24, Boost Demoboard Photo. Figure 26, Dimming Characteristic shows behavior of circuitry in case the square wave signal with 5 V amplitude and 300 Hz frequency was delivered into ON/OFF pin of device. There was tested eight LEDs string with 150 mA consumption and V_{IN} = 10 V at room temperature.

The efficiency of this demoboard is mentioned in Figure 25. Efficiency of Boost LED Driver.

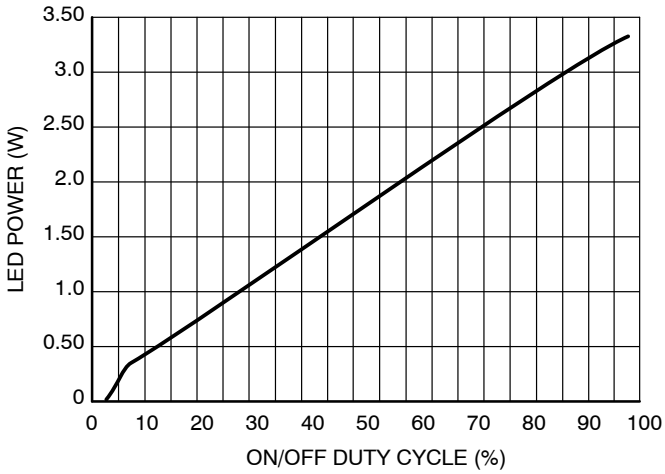


Figure 26. Dimming Characteristic

Table 4. TEST RESULTS

Line Regulation	Vin = 10 V to 20 V, Vout = 19.2 V, Iout = 350 mA	25 mA
Output Ripple	Vin = 10 V to 20 V, Vout = 19.2 V, Iout = 350 mA	55 mA
Efficiency	Vin = 12 V, Vout = 19.2 V, Iout = 350 mA	85%

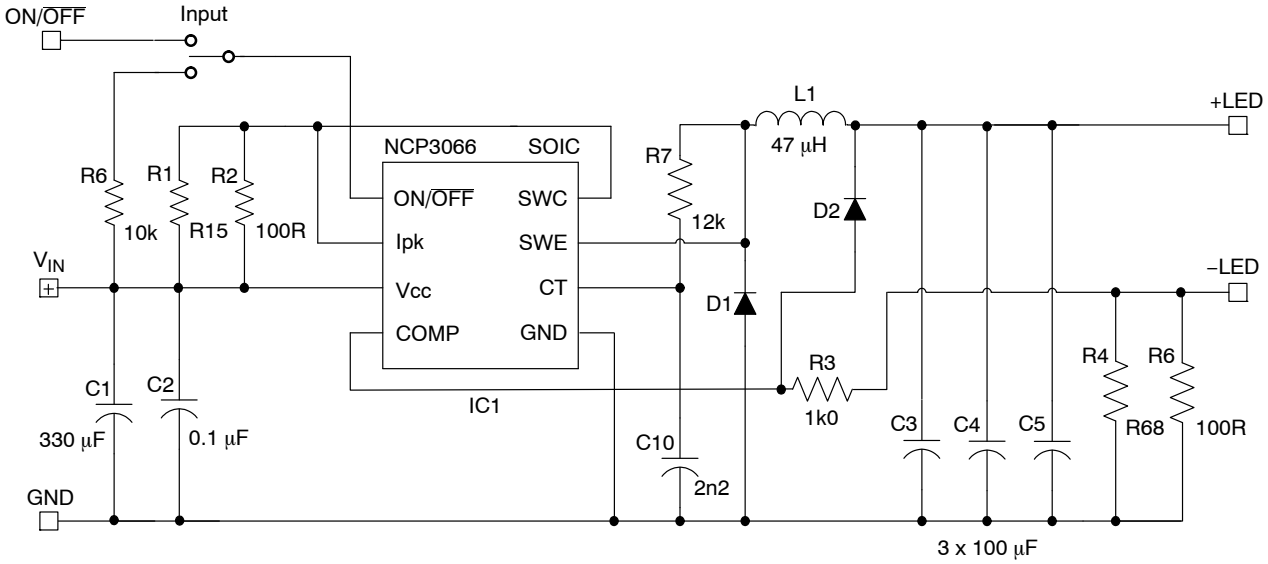


Figure 27. Buck Demoboard Application Schematic

Table 5. BILL OF MATERIALS

Designator	Qty.	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number
R1	1	Resistor	0.15R	1%	1206	Susumu	RL1632R-R150-F
R2; R5	NU	Resisitor	100R	1%	1206	Vishay/Dale	CRCW1206100RFKEA
R3	1	Resisitor	1 k	1%	1206	Rohm	MCR18EZPF1001
R4	1	Resistor	0.68R	5%	1210	Panasonic - ECG	ERJ-14RQJR68U
R6	1	Resisitor	10 k	1%	1206	Rohm	MCR18EZHF1002
R7	NU	Resisitor	12 k	1%	1206	Rohm	MCR18EZPF1202
C1	1	Capacitor	330 μF	20%	F8	PANASONIC	EEEFK1E331GP
C2	1	Capacitor	100 nF	10%	1206	Kemet	C1206C104K5RACTU
C3	1	Capacitor	2.2 nF	10%	1206	Kemet	C1206C222K5RACTU
C4, C5, C6	3	Capacitor	100 μF	20%	1210	TDK	C4532Y5V1A107Z
IC1	1	Switching Regulator	NCP3066	-	SOIC8	ON Semiconductor	NCP3066DR2G
D1	1	Diode	MBRS1504	-	SMB	ON Semiconductor	MBRS1504T3G
D2	1	Zener Diode	BZX84C8V2	-	SOT23	ON Semiconductor	BZX84C8V2LT1G
L1	1	Inductor	47 μH	20%	DO3316	CoilCraft	DO3316P-473MLB

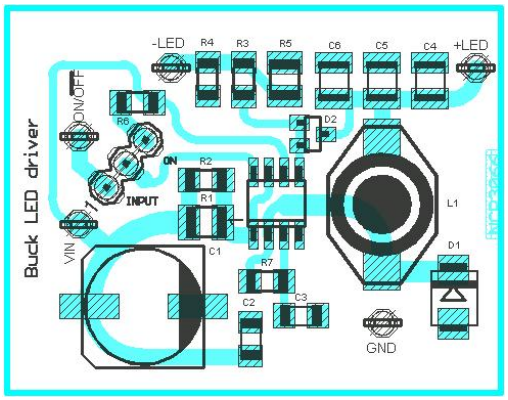


Figure 28. Buck Demoboard Layout

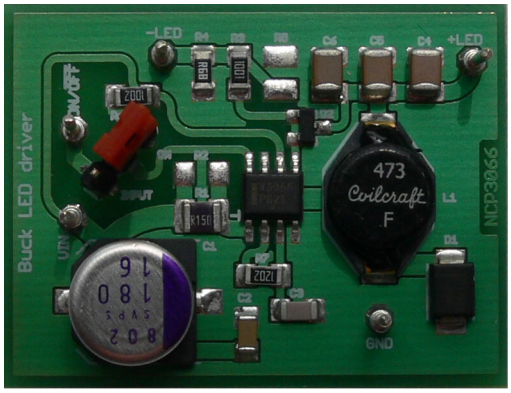


Figure 29. Buck Demonstration Photo

The Figure 27 Buck demoboard Application schematic illustrates the basic circuitry in buck topology, which allows supplying one or two LEDs up to 350 mA consumption. The TABLE 5 BILL OF MATERIALS shows the small number of additional parts which are necessary to assembly mentioned demoboard. The demoboard based on one layer PCB and the layout is mentioned in Figure 28 Buck Demoboard Layout. The Line regulation is mentioned in Figure 30 Line Regulation. The Figure 31 shows efficiency of Buck LED Driver.

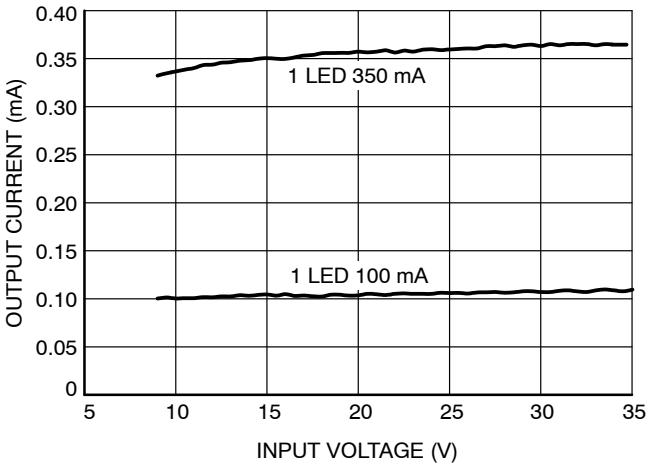


Figure 30. Line Regulation

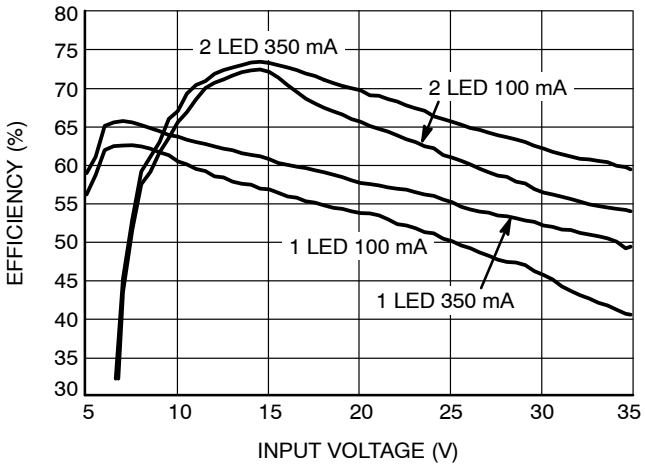


Figure 31. Efficiency of Buck LED Driver

Table 6. TEST RESULTS

Line Regulation	Vin = 8 V to 20 V, Vout = 3.2 V, Iout = 350 mA	19 mA
Output Ripple	Vin = 8 V to 20 V, Vout = 3.2 V, Iout = 350 mA	32 mA
Efficiency	Vin = 12 V, Vout = 3.2 V, Iout = 350 mA	62%

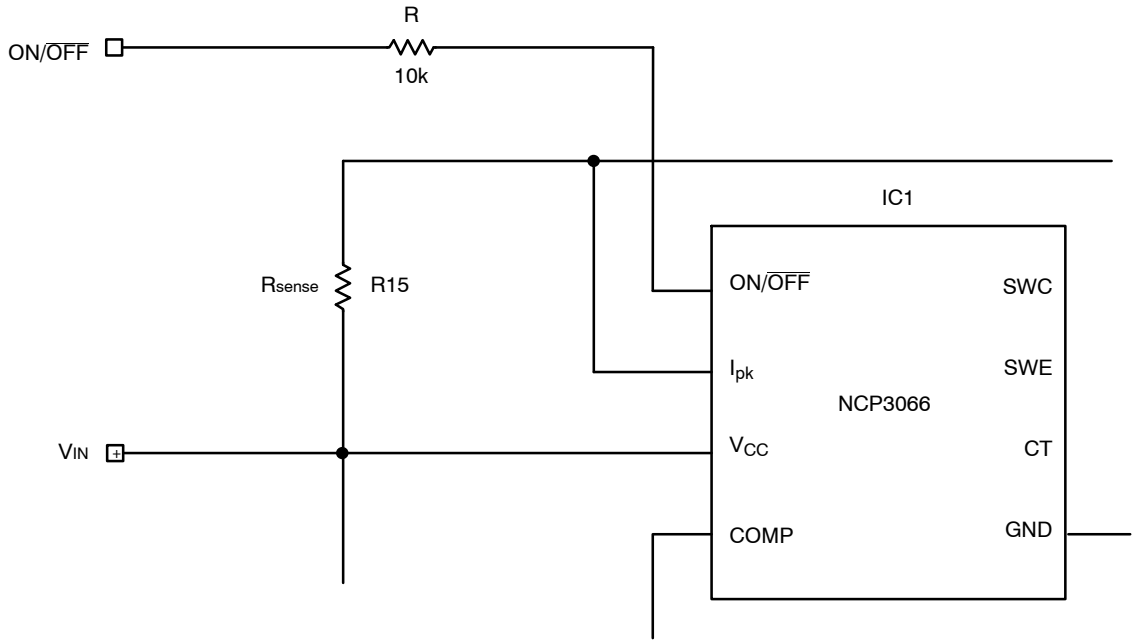


Figure 32. ON/OFF Serial Resistor Connection

If the application allows ON/$\overline{\text{OFF}}$ pin to be biased by voltage and the power supply is not connected to Vcc pin at the same time, then it is recommended to limit ON/OFF current by resistor with value 10 kΩ to protect the NCP3066 device. This situation is mentioned in Figure 32, ON/$\overline{\text{OFF}}$ Serial Resistor Connection.

This resistor shifts the ON/$\overline{\text{OFF}}$ threshold by about 200 mV to higher value, but the TTL logic compatibility is kept in full range of input voltage and operating temperature range.

ORDERING INFORMATION

Device	Package	Shipping†
NCP3066MNTXG	DFN−8 (Pb−Free)	4000 / Tape & Reel
NCP3066PG	PDIP−8 (Pb−Free)	50 Units / Rail
NCP3066DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV3066MNTXG	DFN−8 (Pb−Free)	4000 / Tape & Reel
NCV3066PG	PDIP−8 (Pb−Free)	50 Units / Rail
NCV3066DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

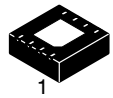
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

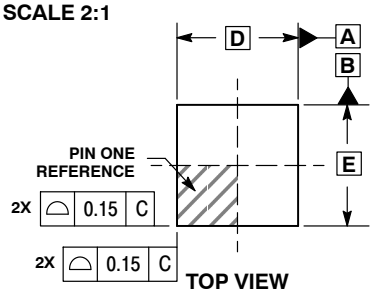
ON Semiconductor®

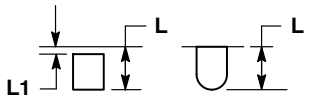
DFN8, 4x4
CASE 488AF−01
ISSUE C

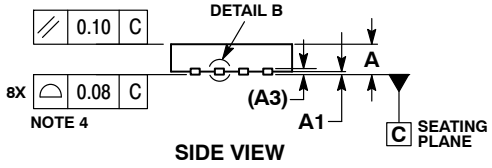
DATE 15 JAN 2009

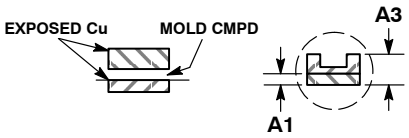


SCALE 2:1



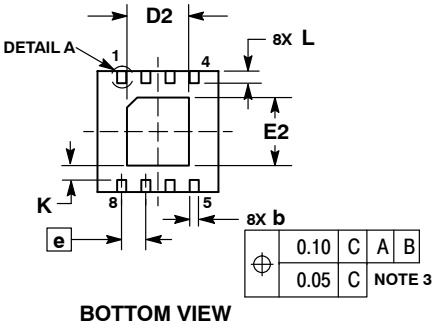




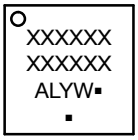


NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DETAILS A AND B SHOW OPTIONAL CONSTRUCTIONS FOR TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	4.00 BSC	
D2	1.91	2.21
E	4.00 BSC	
E2	2.09	2.39
e	0.80 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15



GENERIC MARKING DIAGRAM*

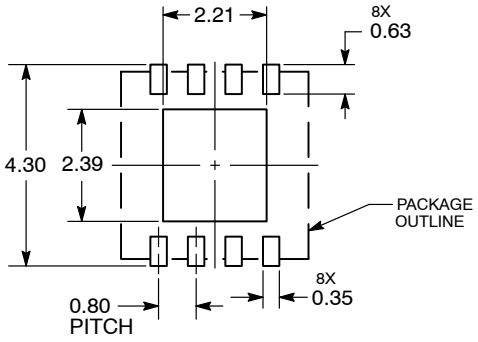


XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON15232D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	DFN8, 4X4, 0.8P	PAGE 1 OF 1

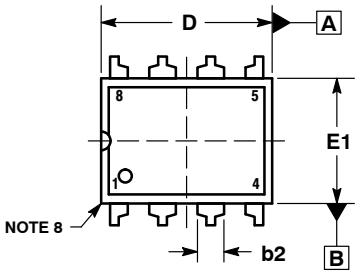
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

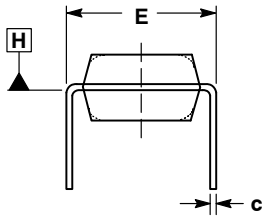
SCALE 1:1

PDIP–8
CASE 626–05
ISSUE P

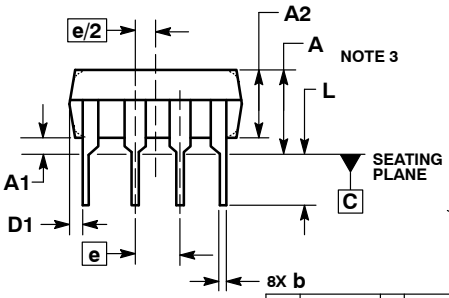
DATE 22 APR 2015



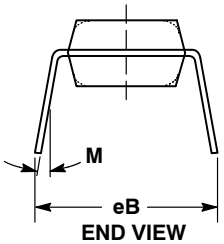
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



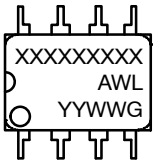
END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	PDIP–8	PAGE 1 OF 1

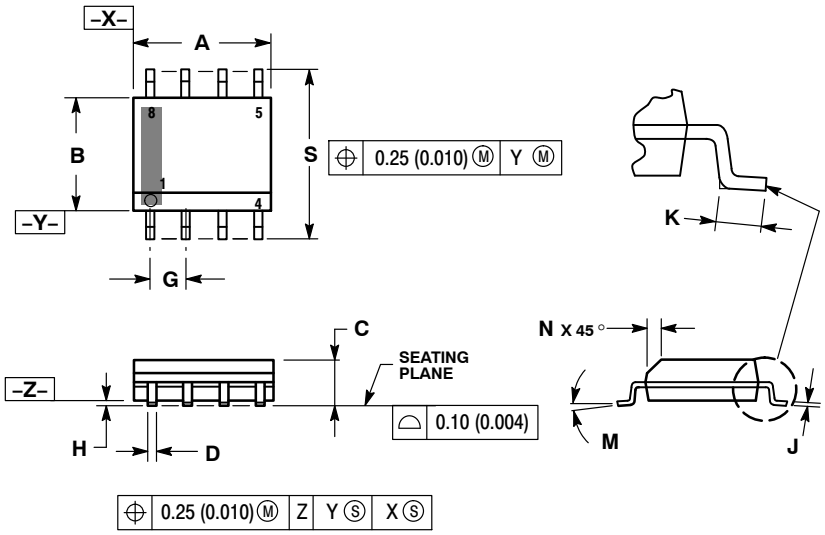
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

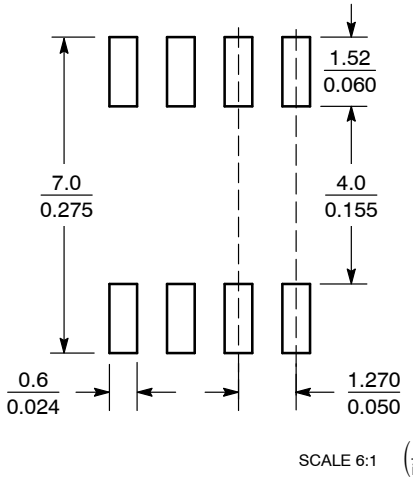
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

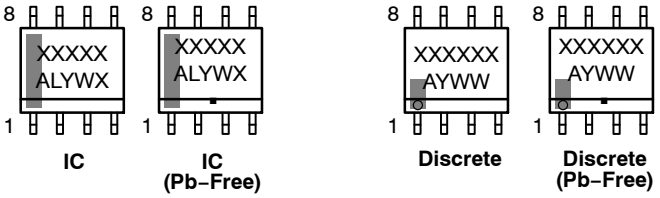
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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