

# 1-Mbit (128K x 8) Industrial Grade Low-Voltage Paged Parallel EEPROM

#### **Features**

- · Fast Read Access Time: 200 ns
- · Automatic Page Write Operation:
  - Internally organized as 131,072 x 8 (1M)
  - Internal address and data latches for 128 bytes
  - Internal control timer
- · Fast Write Cycle Time:
  - Page Write cycle time: 10 ms maximum
  - 1 to 128-byte Page Write operation
- · Low-Power Dissipation:
  - 15 mA active current
  - 50 μA CMOS standby current
- · Hardware and Software Data Protection
- DATA Polling for End of Write Detection
- High Reliability CMOS Technology:
  - Endurance: 100,000 cycles
  - Data retention: 10 years
- Single 3.3V ± 10% Supply
- JEDEC<sup>®</sup> Approved Byte-Wide Pinout
- Industrial Temperature Range
- Green (Pb/Halide-free) Packaging Option

# **Packages**

· 32-Lead PLCC, 32-Lead TSOP

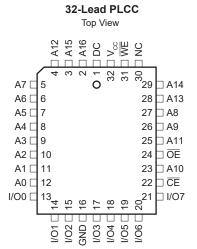
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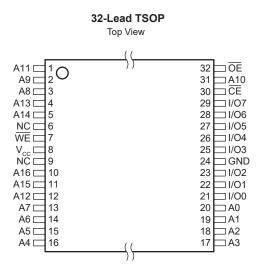
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# 1. Package Types (not to scale)





# 2. Pin Descriptions

The descriptions of the pins are listed in Table 2-1.

Table 2-1. Pin Function Table

Name	32-Lead PLCC	32-Lead TSOP	Function
DC	1	<del>_</del>	Don't Connect
A16	2	10	Address
A15	3	11	Address
A12	4	12	Address
A7	5	13	Address
A6	6	14	Address
A5	7	15	Address
A4	8	16	Address
A3	9	17	Address
A2	10	18	Address
A1	11	19	Address
A0	12	20	Address
I/O0	13	21	Data Input/Output
I/O1	14	22	Data Input/Output
I/O2	15	23	Data Input/Output
GND	16	24	Ground
I/O3	17	25	Data Input/Output
I/O4	18	26	Data Input/Output
I/O5	19	27	Data Input/Output
I/O6	20	28	Data Input/Output
I/O7	21	29	Data Input/Output
CE	22	30	Chip Enable
A10	23	31	Address
ŌĒ	24	32	Output Enable
A11	25	1	Address
A9	26	2	Address
A8	27	3	Address
A13	28	4	Address
A14	29	5	Address
NC	30	6, 9	No Connect
WE	31	7	Write Enable
V <sub>CC</sub>	32	8	Device Power Supply

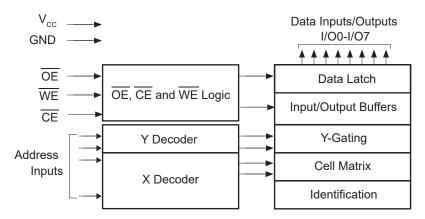
# 3. Description

The AT28LV010 is a high-performance 3-volt only Electrically Erasable and Programmable Read-Only Memory (EEPROM). Its 1-Mb memory is organized as 131,072 words by 8 bits. Manufactured with Microchip's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation of just 54 mW. When the device is deselected, the CMOS standby current is less than 50  $\mu$ A.

The AT28LV010 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte page register to allow writing of up to 128 bytes simultaneously. During a write cycle, the address and 1 to 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by  $\overline{DATA}$  Polling of I/O7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

The AT28LV010 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. A software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 128 bytes of EEPROM for device identification or tracking.

#### 3.1 Block Diagram



### 4. Electrical Characteristics

### 4.1 Absolute Maximum Ratings

Temperature under bias  $-55^{\circ}\text{C to } +125^{\circ}\text{C}$  Storage temperature  $-65^{\circ}\text{C to } +150^{\circ}\text{C}$  All input voltages (including NC pins) with respect to ground -0.6V to +6.25V All output voltages with respect to ground  $-0.6\text{V to } \text{V}_{\text{CC}} + 0.6\text{V}$  Voltage on  $\overline{\text{OE}}$  and A9 with respect to ground -0.6V to +13.5V

**Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### 4.2 DC and AC Operating Range

Table 4-1. DC and AC Operating Range

		AT28LV010-20
Operating Temperature (Case)	Industrial	-40°C to +85°C
V <sub>CC</sub> Power Supply		3.3V ± 10%

#### 4.3 DC Characteristics

#### Table 4-2. DC Characteristics

Parameter	Symbol	Minimum	Maximum	Units	Test Conditions
Input Load Current	ILI	_	1	μA	V <sub>IN</sub> = 0V to V <sub>CC</sub>
Output Leakage Current	I <sub>LO</sub>	_	1	μA	$V_{I/O} = 0V \text{ to } V_{CC}$
V <sub>CC</sub> Standby Current CMOS	I <sub>SB</sub>	_	50	μA	$\overline{CE} = V_{CC} - 0.3V$ to $V_{CC} + 1V$
V <sub>CC</sub> Active Current	I <sub>CC</sub>	_	15	mA	$f = 5 \text{ MHz}; I_{OUT} = 0 \text{ mA},$ $V_{CC} = 3.6V$
Input Low Voltage	V <sub>IL</sub>	_	0.8	V	
Input High Voltage	V <sub>IH</sub>	2.0	_	V	
Output Low Voltage	V <sub>OL</sub>	_	0.45	V	I <sub>OL</sub> = 1.6 mA, V <sub>CC</sub> = 3.0V
Output High Voltage	V <sub>OH1</sub>	2.4	_	V	$I_{OH} = -100 \mu A, V_{CC} = 3.0V$

# 4.4 Pin Capacitance

## Table 4-3. Pin Capacitance<sup>(1,2)</sup>

Symb	ol	Typical	Maximum	Units	Conditions
C <sub>IN</sub>		4	6	pF	V <sub>IN</sub> = 0V
C <sub>OU1</sub>	-	8	12	pF	V <sub>OUT</sub> = 0V

#### Notes:

- 1. This parameter is characterized but is not 100% tested in production.
- 2.  $f = 1 \text{ MHz}, T_A = 25^{\circ}\text{C}$

## 5. Device Operation

**READ**: The AT28LV010 is accessed like a Static RAM. When  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  are low and  $\overline{\text{WE}}$  is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high-impedance state when either  $\overline{\text{CE}}$  or  $\overline{\text{OE}}$  is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

**WRITE**: The write operation of the AT28LV010 allows 1 to 128 bytes of data to be written into the device during a single internal programming period. Each write operation must be preceded by the software data protection (SDP) command sequence. This sequence is a series of three unique write command operations that enable the internal write circuitry. The command sequence and the data to be written must conform to the software protected write cycle timing. Addresses are latched on the falling edge of  $\overline{WE}$  or  $\overline{CE}$ , whichever occurs last and data is latched on the rising edge of  $\overline{WE}$  or  $\overline{CE}$ , whichever occurs first. Each successive byte must be written within 150  $\mu$ s ( $t_{BLC}$ ) of the previous byte. If the  $t_{BLC}$  limit is exceeded, the AT28LV010 will cease accepting data and commence the internal programming operation. If more than one data byte is to be written during a single programming operation, they must reside on the same page as defined by the state of the A7-A16 inputs. For each  $\overline{WE}$  high-to-low transition during the page write operation, A7-A16 must be the same. The A0 to A6 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

**DATA POLLING**: The AT28LV010 features DATA Polling to indicate the end of a write cycle. During a byte or page write cycle, an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs and the next write cycle may begin. DATA Polling may begin at any time during the write cycle.

**TOGGLE BIT**: In addition to DATA Polling, the AT28LV010 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

**DATA PROTECTION**: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Hardware and software features that will protect the memory against inadvertent writes are incorporated.

**HARDWARE PROTECTION**: Hardware features protect against inadvertent writes to the AT28LV010 in the following ways:

- V<sub>CC</sub> power-on delay once V<sub>CC</sub> has reached 2.0V, the device will automatically time out 5 ms (typical) before allowing a write
- Write inhibit holding any one of  $\overline{OE}$  low,  $\overline{CE}$  high or  $\overline{WE}$  high inhibits write cycles
- Noise filter pulses of less than 15 ns (typical) on the WE or CE inputs will not initiate a write cycle

**SOFTWARE DATA PROTECTION**: The AT28LV010 incorporates the industry standard software data protection (SDP) function. Unlike standard 5-volt only EEPROM's, the AT28LV010 has SDP enabled at all times. Therefore, all write operations must be preceded by the SDP command sequence.

The data in the 3-byte command sequence is not written to the device; the addresses in the command sequence can be utilized just like any other location in the device. Any attempt to write to the device without the 3-byte sequence will start the internal timers. No data will be written to the device; however, for the duration of  $t_{WC}$ , read operations will effectively be polling operations.

### 5.1 Operating Modes

Table 5-1. Operating Modes

Mode	CE	ŌĒ	WE	I/O
Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	D <sub>OUT</sub>
Write <sup>(1)</sup>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	D <sub>IN</sub>
Standby/Write Inhibit	V <sub>IH</sub>	X <sup>(2)</sup>	X	High-Z

continued							
Mode	CE	ŌĒ	WE	I/O			
Write Inhibit	X	X	V <sub>IH</sub>				
Write Inhibit	X	V <sub>IL</sub>	X				
Output Disable	X	V <sub>IH</sub>	X	High-Z			

#### Notes:

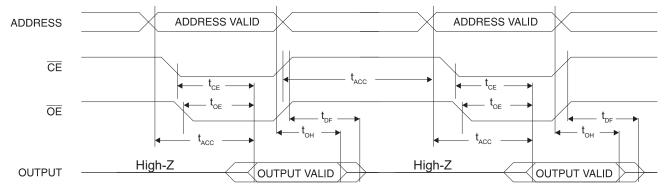
- 1. Refer to AC Programming Waveforms.
- 2. X can be  $V_{IL}$  or  $V_{IH}$ .

### 5.2 AC Read Characteristics

Table 5-2. AC Read Characteristics

Parameter	Symbol	AT28L\	Units	
		Min.	Max.	
Address to Output Delay	t <sub>ACC</sub>	_	200	ns
CE to Output Delay	t <sub>CE</sub> <sup>(1)</sup>	_	200	ns
OE to Output Delay	t <sub>OE</sub> <sup>(2)</sup>	0	80	ns
CE or OE to Output Float	t <sub>DF</sub> (3,4)	0	55	ns
Output Hold from $\overline{OE}$ , $\overline{CE}$ or Address, whichever occurred first	t <sub>OH</sub>	0	_	ns
CE Pulse High Time	t <sub>CEPH</sub> <sup>(5)</sup>	50	<u> </u>	ns

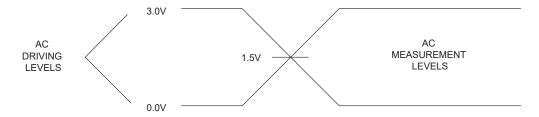
#### 5.3 AC Read Waveforms



#### Notes:

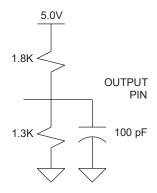
- 1.  $\overline{\text{CE}}$  may be delayed up to  $t_{ACC}$ - $t_{CE}$  after the address transition without impact on  $t_{ACC}$ .
- OE may be delayed up to t<sub>CE</sub>-t<sub>OE</sub> after the falling edge of CE without impact on t<sub>CE</sub> or by t<sub>ACC</sub>-t<sub>OE</sub> after an address change without impact in t<sub>ACC</sub>.
- 3.  $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs first (C<sub>L</sub> = 5 pF).
- 4. This parameter is characterized and is not 100% tested.
- 5. If  $\overline{\text{CE}}$  is de-asserted, it must remain de-asserted for at least 50 ns during read operations otherwise incorrect data may be read.

# 5.4 Input Test Waveforms and Measurement Level



**Note:**  $t_R$ ,  $t_F < 5$  ns.

## 5.5 Output Test Load



### 5.6 AC Write Characteristics

Table 5-3. AC Write Characteristics<sup>(1)</sup>

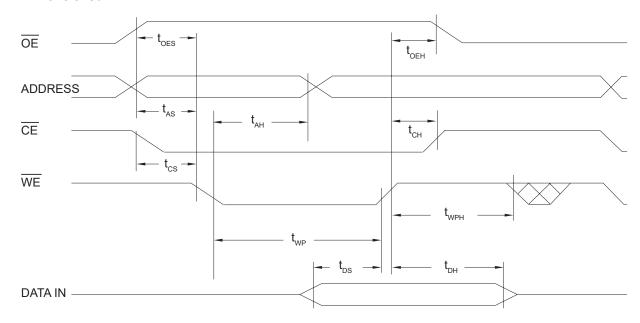
Parameter	Symbol	Minimum	Maximum	Units
Address, OE Setup Time	t <sub>AS</sub> , t <sub>OES</sub>	0	_	ns
Address Hold Time	t <sub>AH</sub>	100	_	ns
Chip Select Setup Time	t <sub>CS</sub>	0	_	ns
Chip Select Hold Time	t <sub>CH</sub>	0	<del>_</del>	ns
Write Pulse Width (WE or CE)	t <sub>WP</sub>	200	<del>_</del>	ns
Data Setup Time	t <sub>DS</sub>	100	<del>_</del>	ns
Data, OE Hold Time	t <sub>DH</sub> , t <sub>OEH</sub>	10	_	ns

#### Note:

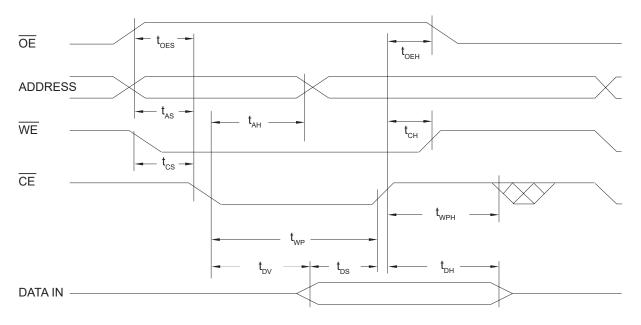
1. All write operations must be preceded by the SDP command sequence.

## 5.7 AC Write Waveforms

### 5.7.1 WE Controlled



### 5.7.2 **CE** Controlled

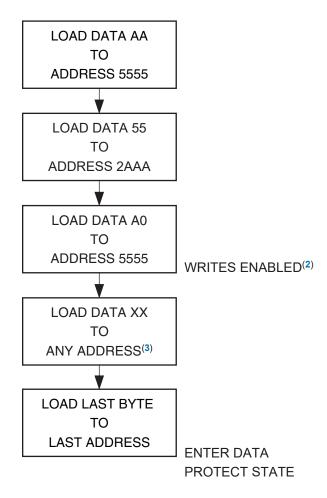


### 5.8 Software Protected Write Characteristics

**Table 5-4. Software Protected Write Characteristics** 

Parameter	Symbol	Minimum	Maximum	Units
Write Cycle Time	t <sub>WC</sub>	_	10	ms
Address Setup Time	t <sub>AS</sub>	0	_	ns
Address Hold Time	t <sub>AH</sub>	100	_	ns
Data Setup Time	t <sub>DS</sub>	100	_	ns
Data Hold Time	t <sub>DH</sub>	10	_	ns
Write Pulse Width	t <sub>WP</sub>	200	_	ns
Byte Load Cycle Time	t <sub>BLC</sub>	_	150	μs
Write Pulse Width High	t <sub>WPH</sub>	100	_	ns

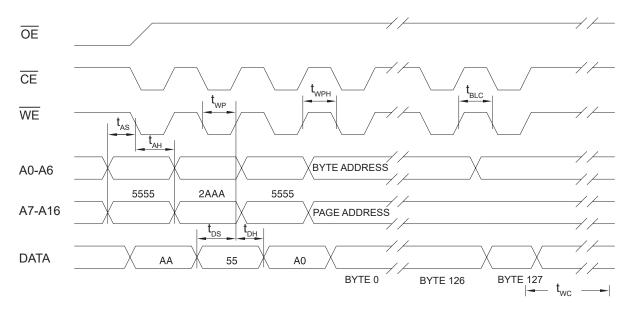
# 5.9 Programming Algorithm<sup>(1)</sup>



#### Notes:

- Data format: I/O7-I/O0 (Hex); Address format: A16-A0 (Hex). 1.
- Data Protect state will be re-activated at the end of program cycle.
- 1 to 128 bytes of data are loaded.

#### 5.10 Software Protected Program Cycle Waveform (1,2,3)



#### Notes:

- 1. A0-A16 must conform to the addressing sequence for the first 3 bytes as shown above.
- After the command sequence has been issued and a page write operation follows, the page address inputs (A7-A16) must be the same for each high-to-low transition of WE (or CE).
- $\overline{\text{OE}}$  must be high only when  $\overline{\text{WE}}$  and  $\overline{\text{CE}}$  are both low.

#### Data Polling Characteristics<sup>(1)</sup> 5.11

Table 5-5. Data Polling Characteristics

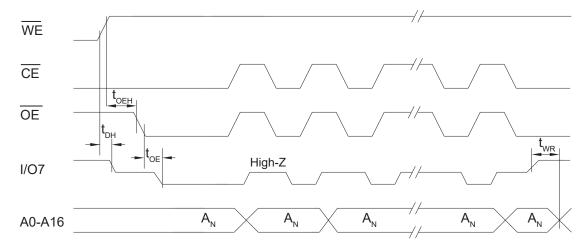
Parameter	Symbol	Minimum	Typical	Maximum	Units
Data Hold Time	t <sub>DH</sub>	10	_	_	ns
OE Hold Time	t <sub>OEH</sub>	10	_	<del></del>	ns
OE to Output Delay <sup>(2)</sup>	t <sub>OE</sub>	_	_	<del>-</del>	ns
Write Recovery Time	t <sub>WR</sub>	0	<del></del>	<del></del>	ns

#### Notes:

- 1. These parameters are characterized and not 100% tested.
- 2. See AC Read Characteristics.

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# 5.12 Data Polling Waveforms



# 5.13 Toggle Bit Characteristics<sup>(1)</sup>

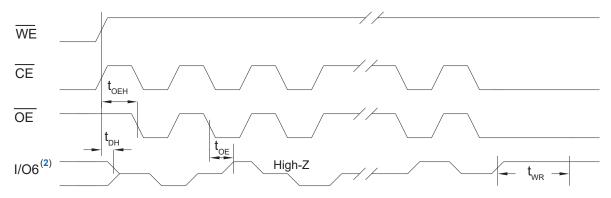
Table 5-6. Toggle Bit Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
Data Hold Time	t <sub>DH</sub>	10	<u> </u>	_	ns
OE Hold Time	t <sub>OEH</sub>	10	_	_	ns
OE to Output Delay <sup>(2)</sup>	t <sub>OE</sub>	_	<del>-</del>	<del>-</del>	ns
OE High Pulse <sup>(2)</sup>	t <sub>OEHP</sub>	150	<del></del>	<del>-</del>	ns
Write Recovery Time	t <sub>WR</sub>	0	<del>_</del>	<del>_</del>	ns

#### Notes:

- 1. These parameters are characterized and not 100% tested.
- 2. See AC Read Characteristics.

## 5.14 Toggle Bit Waveforms



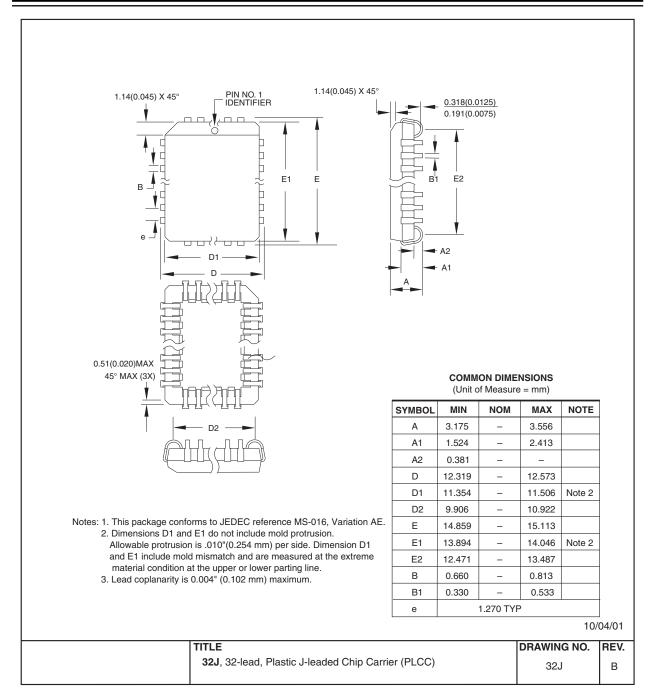
#### Notes:

- 1. Toggling either  $\overline{OE}$  or  $\overline{CE}$  or both  $\overline{OE}$  and  $\overline{CE}$  will operate toggle bit.
- 2. Beginning and ending state of I/O6 will vary.
- 3. Any address location may be used but the address should not vary.

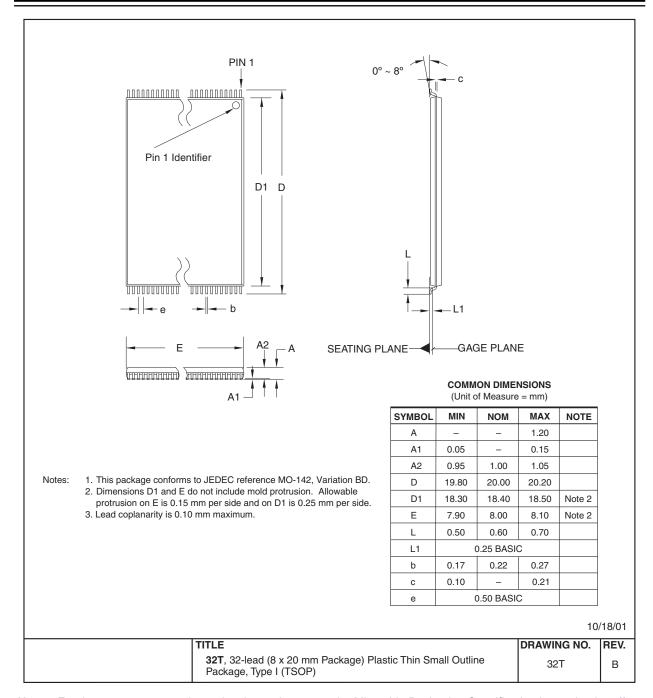
# 6. Packaging Information

## 6.1 Package Marking Information

32-lea	d TSOP	32-lead	PLCC
Topside	Backside	Topside	Backside
ATMEL AT28LV010 20U-19506V YYWWNNN	those device perkages	ATMEL AT28LV010 20U-19506V YYWWNNN	
Note. No backside marking of	Titlese device packages.		
Note. No backside marking of	Titlese device packages.		
Note: No backside marking of	Lot Trace	e Code	
Note. No backside marking of		ce Code Week,	



**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.



**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

# 7. Revision History

#### Revision A (August 2020)

Updated to Microchip template. Microchip DS20006405 replaces Atmel document 0395. Added updated Part Markings to include new trace code format.

#### Atmel Document 0395 Revision F (August 2009)

Added Revision History section. Updated AC Characteristics and ordering information.

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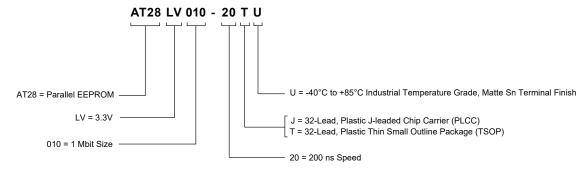
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- · Local Sales Office
- Embedded Solutions Engineer (ESE)
- · Technical Support

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#### Examples

Table 11-1. AT28LV010 Ordering Information

Ordering Code	Package Number	t <sub>ACC</sub> (ns)	Quantity	Operating Range
AT28LV010-20JU	32J		Tube 32	
AT28LV010-20JU-T	32J	200	Reel 750	Industrial
AT28LV010-20TU	32T	200	Tray 156	(-40°C to 85°C)
AT28LV010-20TU-T	32T		Reel 1500	

Package Types				
32J	32-Lead, Plastic J-Leaded Carrier (PLCC)			
32T	32-Lead, Plastic Thin Small Outline Package (TSOP)			

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Detroit	Fax: 972-818-2924	China - Suzhou	Taiwan - Taipei	Italy - Milan
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