N-Channel Enhancement Mode MOSFET TDM3482C

DESCRIPTION

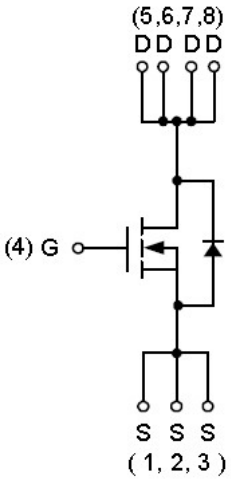
The TDM3482C uses advanced trench technology to provide excellent RDS(ON) and low gate charge. This device is suitable for use as a load switch or in PWM applications.

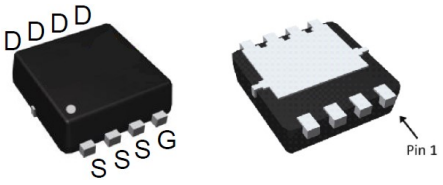
GENERAL FEATURES

- RDS(ON) < 8.5mΩ @ VGS=10V
  RDS(ON) < 15mΩ @ VGS=4.5V
- High Power and current handling capability
- Lead free product is available
- Surface Mount Package

Application

- PWM applications
- Load switch
- Power management





PPAK-3*3-8

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current @ Continuous (Note 1)	I_D (T_C=25℃)	50	A
	I_D (T_C=100℃)	33	A
Drain Current @ Current-Pulsed (Note 2)	I_{DM}	125	A
Maximum Power Dissipation (Note 3)	P_D (T_C=25℃)	39	W
Maximum Operating Junction Temperature	T_J	150	℃
Storage Temperature Range	T_{STG}	-55 To 150	℃

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$ (Steady State)	60	℃/W
Thermal Resistance-Junction to Case (Note 1)	$R_{\theta JC}$ (Steady State)	3.2	℃/W

ELECTRICAL CHARACTERISTICS (T_A=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=32V, V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=VGS, I_D=250μA	1.35	-	3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=12A	-	6.9	8.5	mΩ
		V_{GS}=4.5V, I_D=10A	-	10.5	15	mΩ
DYNAMIC CHARACTERISTICS (Note5)						
Gate Resistance	R_G	V_{DS}=0V, V_{GS}=0V, F=1.0MHz	-	1.7	-	Ω
Input Capacitance	C_{iss}	V_{DS}=15V, V_{GS}=0V, F=1.0MHz	-	690	-	PF
Output Capacitance	C_{oss}		-	193	-	PF
Reverse Transfer Capacitance	C_{rss}		-	38	-	PF
SWITCHING CHARACTERISTICS (Note5)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=15V, V_{GS}=10V, R_G=3.3Ω I_D=1A	-	14.3	-	nS
Turn-on Rise Time	t_r		-	5.6	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	20	-	nS
Turn-Off Fall Time	t_f		-	11	-	nS
Total Gate Charge	Q_g	V_{DS}=20V, I_D=12A, V_{GS}=4.5V	-	5.8	-	nC
Gate-Source Charge	Q_{gs}		-	3	-	nC
Gate-Drain Charge	Q_{gd}		-	1.2	-	nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
Continuous Source Current (Note 1,4)	I_S	V_G=V_D=0V, Force Current	-	-	30	A
Diode Forward Voltage (Note 2)	V_{SD}	V_{GS}=0V, I_S=20A	-	0.8	1.1	V

NOTES:

1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%. Pulse width limited by max. junction temperature.
3. The power dissipation is limited by 150℃ junction temperature.
4. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.
5. Guaranteed by design, not subject to production testing.

Typical Operating Characteristics

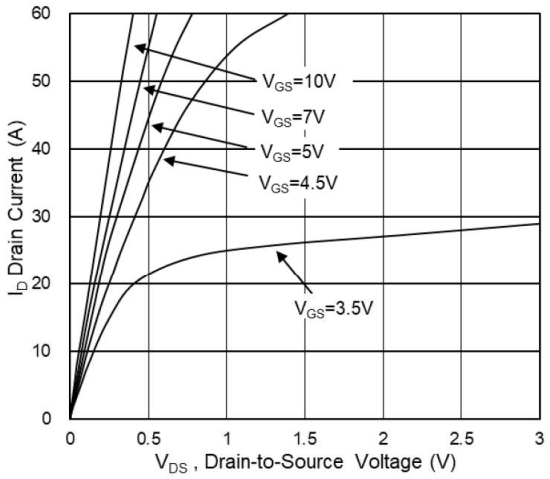


Fig.1 Typical Output Characteristics

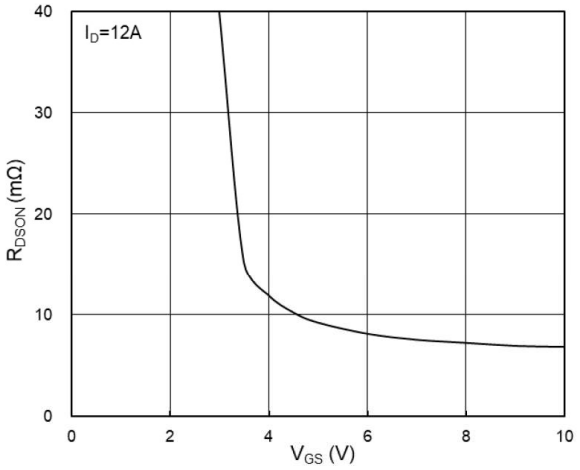


Fig.2 On-Resistance vs G-S Voltage

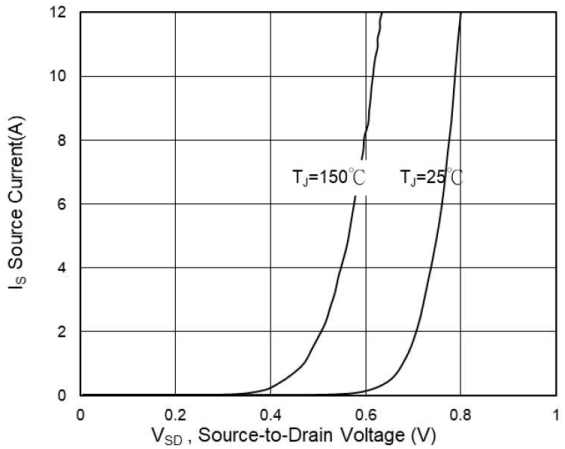


Fig.3 Source Drain Forward Characteristics

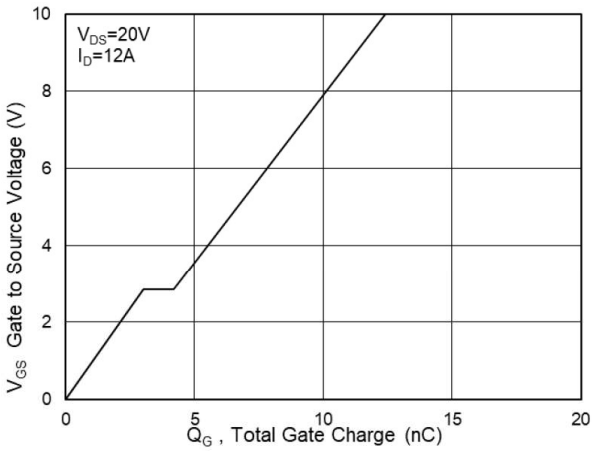


Fig.4 Gate-Charge Characteristics

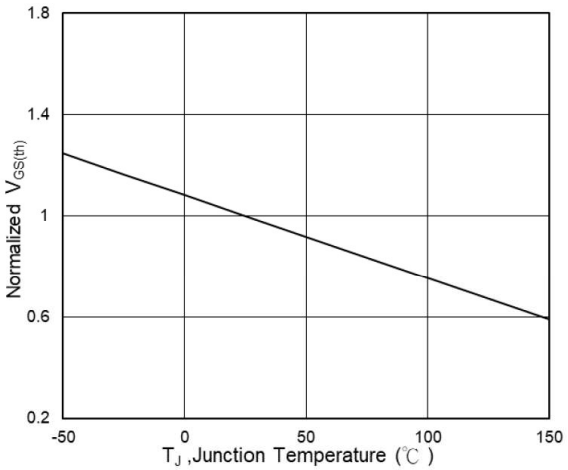


Fig.5 Normalized $V_{GS(th)}$ vs T_J

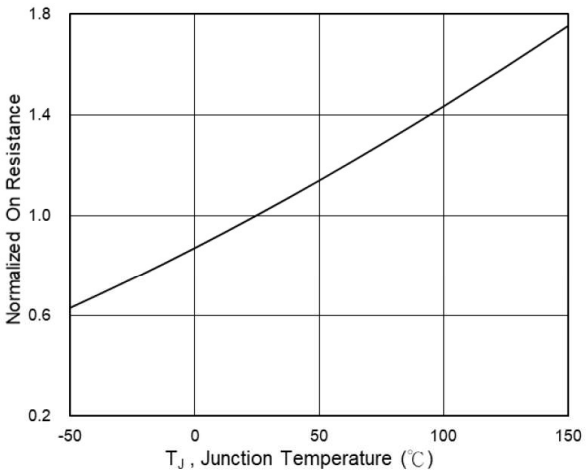


Fig.6 Normalized R_{DSON} vs T_J

Typical Operating Characteristics (Cont.)

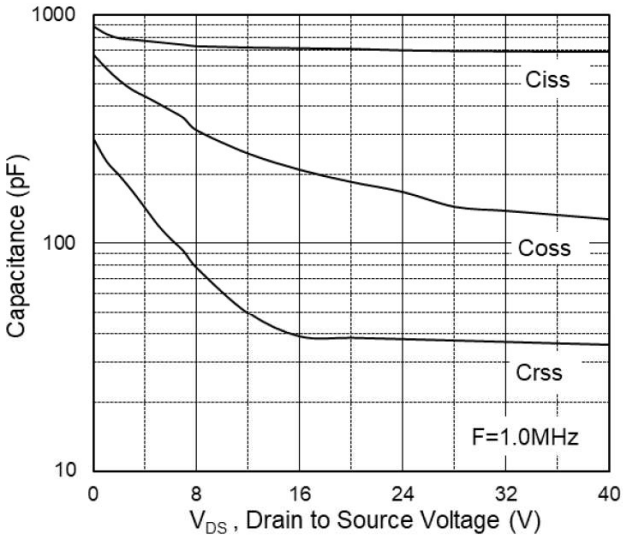


Fig.7 Capacitance

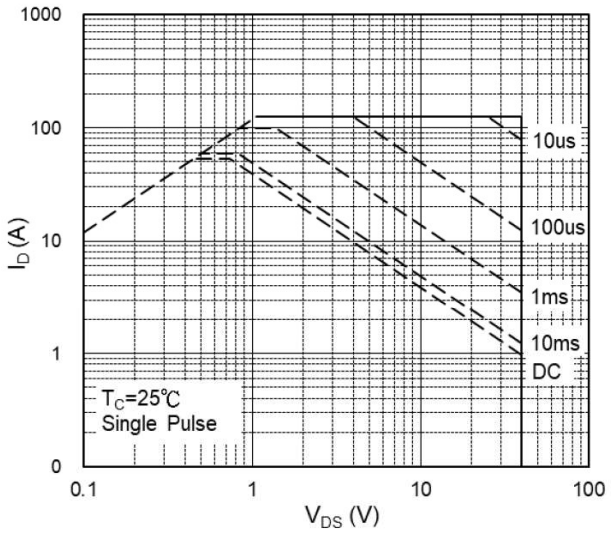


Fig.8 Safe Operating Area

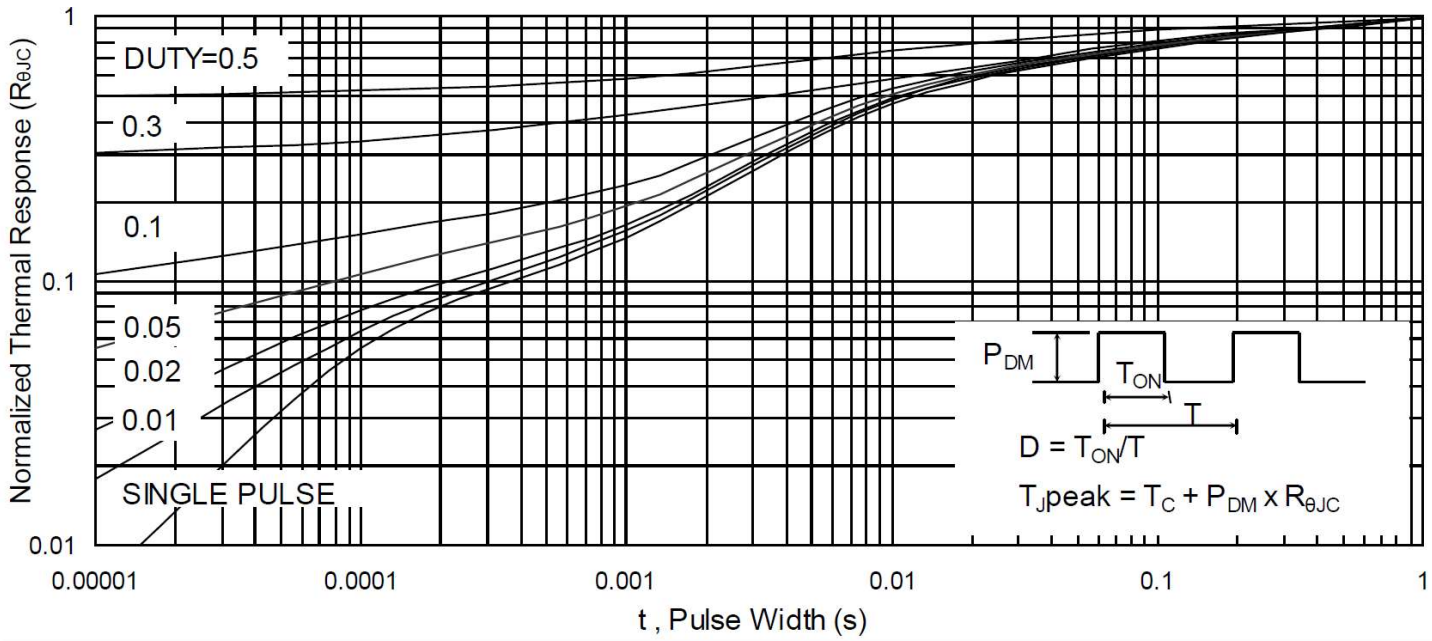
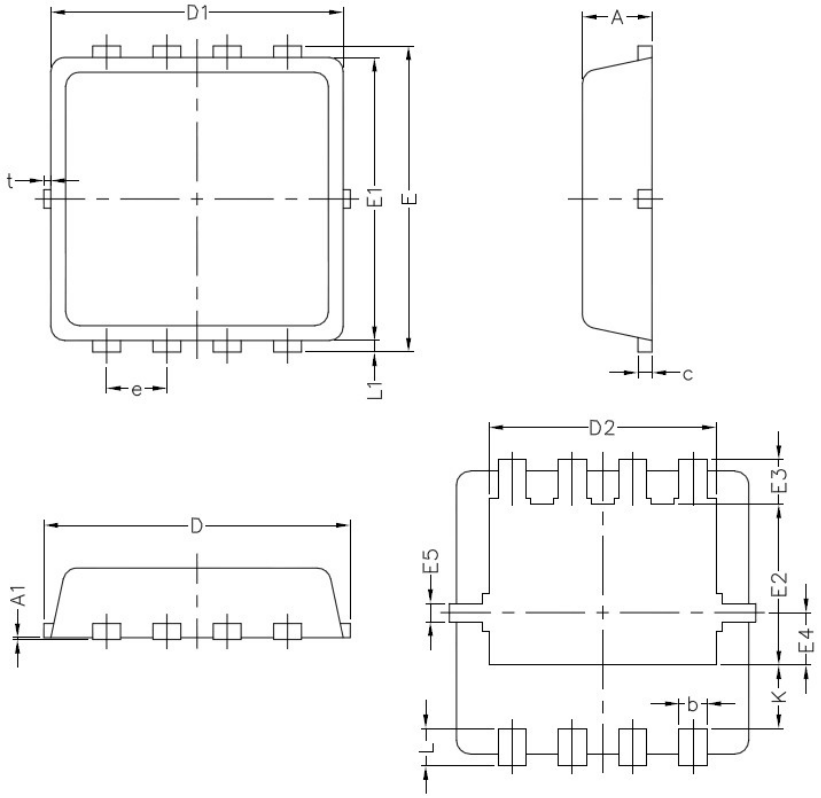


Fig.9 Normalized Maximum Transient Thermal Impedance

Package Information

PPAK-3*3-8 Package



Symbol	PPAK-3*3-8(mm)		
	Min	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.3	3.45
D1	3.00	3.15	3.30
D2	2.25	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.68
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.49	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	/	/	0.13

Design Notes