

# LPM9017 - -30V/4A P-Channel Enhancement Mode Field Effect Transistor

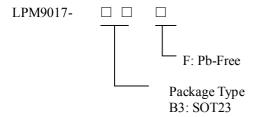
### **General Description**

The LPM9017 is the P-channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

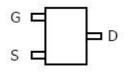
These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.

### **Ordering Information**



# **Pin Configurations**

TO-236 (SOT-23) Top View



#### **Features**

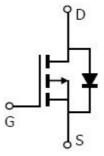
- -30V/-4A,RDS(ON) $<58m\Omega(typ.)@VGS=-10V$
- -30V/-3.0A,RDS(ON)  $\leq 68m\Omega(typ.)@VGS=-4.5V$
- Super high density cell design for extremely low RDS(ON)
- SOT23 Package

### **Applications**

- ♦ Portable Media Players
- ♦ Cellular and Smart mobile phone
- ♦ LCD
- ♦ DSC Sensor
- ♦ Wireless Card

### **Marking Information**

Please see website.



SOT23L(Top View)



# **Functional Pin Description**

Absolute Maximum Ratings T <sub>A</sub> =25°C unless otherwise noted					
Parameter		Symbol	Maximum	Units	
Drain-Source Voltage		V <sub>DS</sub>	-30	V	
Gate-Source Voltage		V <sub>GS</sub>	±20	V	
Continuous Drain	T <sub>A</sub> =25°C		-4.1	2-1	
Current	T <sub>A</sub> =70°C		-3.5	A	
Pulsed Drain Current <sup>c</sup>		I <sub>DM</sub>	-25		
Power Dissipation <sup>B</sup>	T <sub>A</sub> =25°C	D	1.4	147	
	T <sub>A</sub> =70°C	P <sub>D</sub>	0.9	W	
Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	°C	

Thermal Characteristics							
Parameter	Symbol	Тур	Max	Units			
Maximum Junction-to-Ambient <sup>A</sup>	t ≤ 10s	D	70	90	°C/W		
Maximum Junction-to-Ambient AD	Steady-State	R <sub>eja</sub>	100	125	°C/W		
Maximum Junction-to-Lead	Steady-State	R <sub>eJL</sub>	63	80	°C/W		



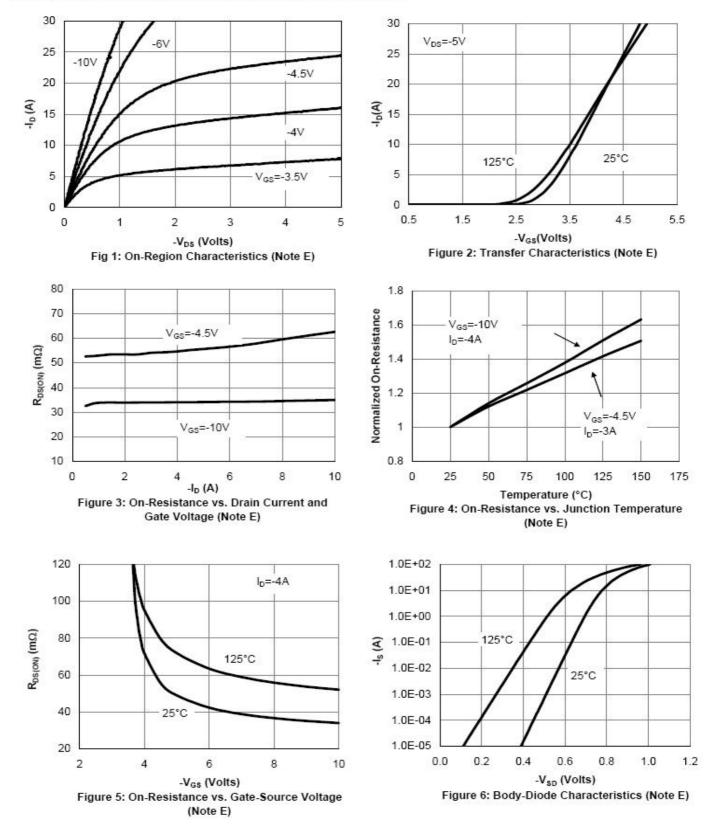
LPM9017

Symbol	Parameter	Condition	Min	Тур	Max	Unit
Static Paran	neters					
V(BR)DSS	Drain-Source Breakdown Voltage	Vas=0V,Io=-250µA	-20			v
VG8(th)	Gate Threshold Voltage	Vos=Vos, lo=-250µA	-0.6		-1.2	V
lass	Gate Leakage Current	V <sub>D8</sub> =0V,V <sub>G8</sub> =±12V			±100	nA
loss	Zero Gate Voltage Drain	Vos=-24V,Vos=0V			-1	μA
	Current	Vos=-24V,Vos=0V Tu=55°C			-10	
Rds(on)	Drain-source On-Resistance	V <sub>98</sub> =-10V,I <sub>D</sub> =-4.0A V98=-4.5V,Ib=-3.0A V <sub>98</sub> =-2.5V,I <sub>D</sub> =-2.0A		55 64 85	58 68 95	mΩ
G	Forward Transconductance	Vos=-5V,lo=-4.0A		10		Ś
Source-Drai	in Doide					
Vso	Diode Forward Voltage	I <sub>S</sub> =-1.0A,V <sub>GS</sub> =0V		-0.7	-1.0	V
Dynamic Pa	rameters					
Q,	Total Gate Charge	Vns=-15V		7		nC
Qgs	Gate-Source Charge	Vos=-10V		13		
Qgd	Gate-Drain Charge	I <sub>D</sub> ≡-4.0A		1.8		
Clss	Input Capacitance	Vos=-15V		680		pF
Coss	Output Capacitance	Vgs=DV		320		
Crss	Reverse Transfer Capacitance	f=1MHz		65		
td(an)	T 0 T	Voo=-15V		12	18	nS
tr	Turn-On Time	RL=15Ω		3	7	
td(off)	Turn-Off Time	ID=-1A Vgen=-10V		34	42	
tr	Turn-Off Time	Ro=6Ω		3	7	





#### TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS





### LPM9017

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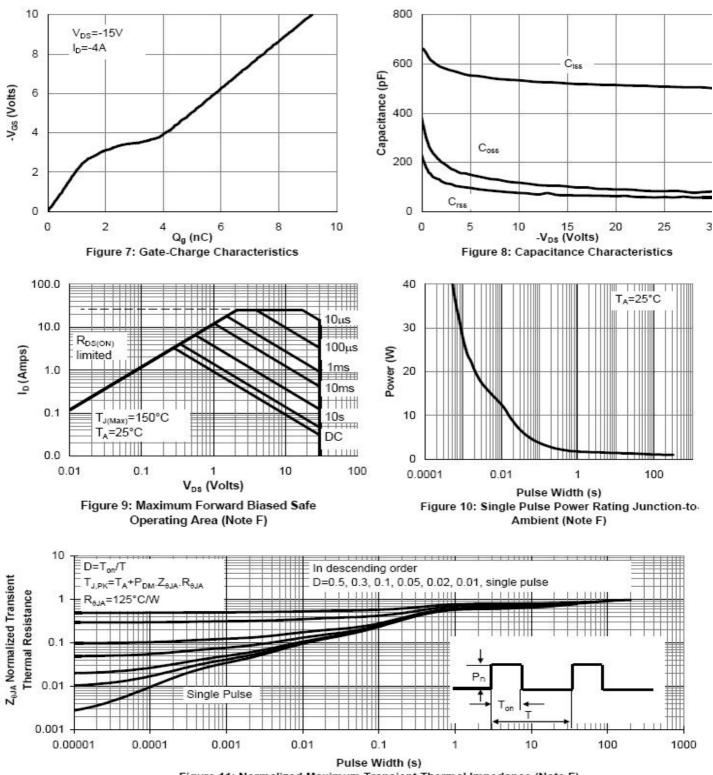
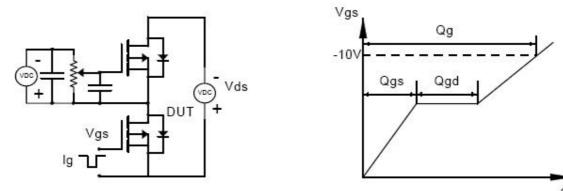


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

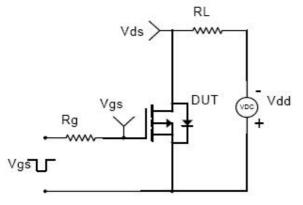


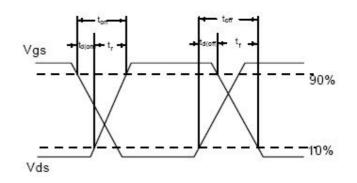
#### Gate Charge Test Circuit & Waveform



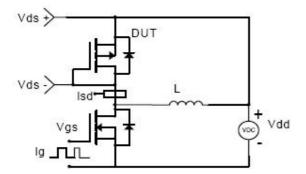
Charge

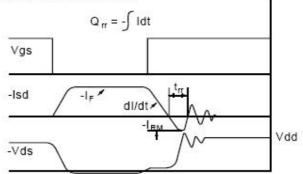
Resistive Switching Test Circuit & Waveforms





#### Diode Recovery Test Circuit & Waveforms

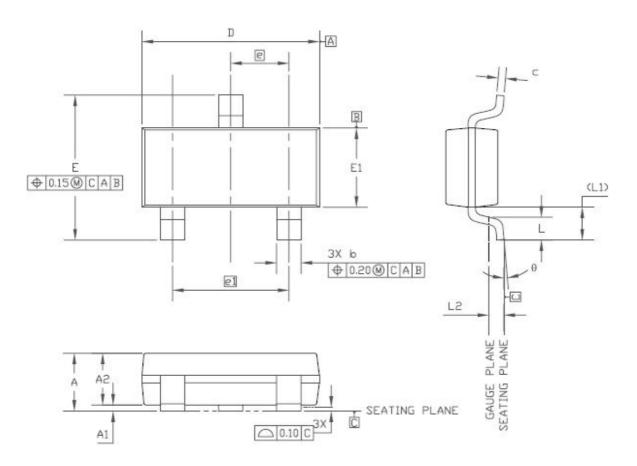




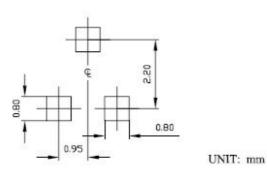


**Packaging Information** 

### SOT-23 STANDARD PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



L2	0.25			0.010			
L1	0.54 REF			0.021REF			
L	0.40	0.50	0.60	0.016	0.020	0.024	
el	1.90 BSC			0.075 BSC			
e	0.95 BSC			0.037 BSC			
E1	1.20	1.30	1.40	0.047	0.051	0.055	
E	2.10		2.64	0.083		0.104	
D	2.80	2.90	3.04	0.110	0.114	0.120	
C	0.08		0.20	0.003		0.008	
b	0.30		0.50	0.012		0.020	
A2	0.70	0.85	1.02	0.028	0.033	0.040	
A1	0.05		0.15	0.002		0.006	
A	0.75		1.17	0.030		0.046	
013009000	MIN	NOM	MAX	MIN	NOM	MAX	
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES			