



## DP3415

P-Channel Enhancement Mode Field Effect Transistor

## **General description**

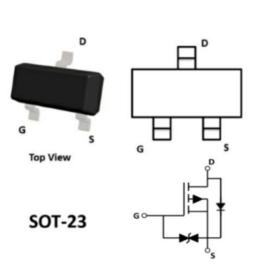
P-Channel Enhancement Mode Field Effect Transistor

#### Features:

- V<sub>DS</sub> (V) =-20V
- I<sub>D</sub> =-5 A (V<sub>GS</sub> =-4.5V)
- $R_{DS(ON)} < 42m\Omega (V_{GS} = -4.5V)$
- $R_{DS(ON)} < 60m\Omega (V_{GS}$  =-2.5V)
- $R_{DS(ON)} < 120 m\Omega (V_{GS} = -1.8V)$
- ESD Protected UP to 2.0KV(HBM)
- Trench Power LV MOSFET technology
- High Density Cell Design for Low RDS(ON)
- High Speed switching

#### Applications

- Battery protection
- Load switch
- Power management



#### **Device Marking:**

Device Type	Marking		
DP3415	3415E or AFXL*		

#### Absolute Maximum Ratings (TA=25°Cunless otherwise noted)

Parameter		Symbol	Rating	Unit	
Drain-Source Voltage		Vds	-20		
Gate-Source Voltage		Vgs	±12	V	
Quatiences Decis Queent	TA=25°C	1-	-5		
Continuous Drain Current	Ta=70°C	lo	-4.2	A	
Pulsed Drain Current		Ідм	-23	~	
Power Dissipation	Ta=25°C	Po	1.3	w	
Thermal Resistance.Junction- to-Ambient	Steady-State	R <sub>thJA</sub>	96	°C/W	
Junction Temperature		TJ	150	ĉ	
Junction Storage Temperature Range		Tstg	-55 to 150	C	



#### Electrical Characteristics (T\_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Тур	Мах	Units
Static Parameter			-			
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =-250µA	-20			V
Zero Gate Voltage Drain Current	IDSS	$V_{\text{DS}}\text{=-20V,} V_{\text{GS}}\text{=}0\text{V,} T_{\text{C}}\text{=}25^\circ\!\!\mathbb{C}$			-1	μA
		$V_{GS}\text{=}\pm10\text{V}, \text{V}_{DS}\text{=}0\text{V}$		±2.5	±10	μA
Gate-Body Leakage Current	lcss	$V_{\text{GS}}\text{=}\pm8\text{V}, \text{V}_{\text{DS}}\text{=}0\text{V}$		±900	±2000	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS}$ = $V_{GS}$ , $I_D$ =-250 $\mu$ A	-0.50	-0.67	-0.95	V
Static Drain-Source On-Resistance		V <sub>GS</sub> = -4.5V, I <sub>D</sub> =-4.0A		35	42	mΩ
	Rds(on)	V <sub>GS</sub> = -2.5V, I <sub>D</sub> =-3.0A		47	60	
		V <sub>GS</sub> = -1.8V, I <sub>D</sub> =-1.5A		64	120	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-5A,V <sub>GS</sub> =0V		-0.8	-1.2	V
Maximum Body-Diode Continuous Current	Is				-5	А
Dynamic Parameters			_	1		
Input Capacitance	C <sub>iss</sub>			940		
Output Capacitance	C <sub>oss</sub>	$V_{DS}$ =-10V, $V_{GS}$ =0V,f=1MHZ		219		pF
Reverse Transfer Capacitance	Crss			116		
Switching Parameters			-			
Total Gate Charge	Qg			7.2		
Gate Source Charge	Qgs	V <sub>GS</sub> =-4.5V,V <sub>DD</sub> =-10V,I <sub>D</sub> =-4A		1.2		nC
Gate Drain Charge	Q <sub>gd</sub>			1.6		
Turn-on Delay Time	tD(on)	$V_{GS}$ =-4.5V, $V_{DD}$ =-10V, R <sub>L</sub> =2.5 $\Omega$ ,		15		<b></b> -
Turn-on Rise Time	tr	$R_{GEN}=3\Omega$		63		ns
Turn-off Delay Time	tD(off)			21		
Turn-off Fall Time	t <sub>f</sub>			12		

A. Pulse Test: Pulse Width $\leq$ 300us,Duty cycle  $\leq$ 2%.

B. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch.



### **Typical Performance Characteristics**

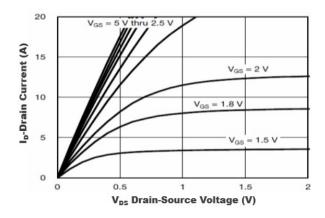


Figure1. Output Characteristics

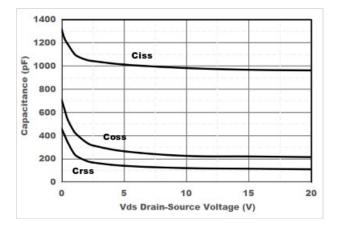


Figure3. Capacitance Characteristics

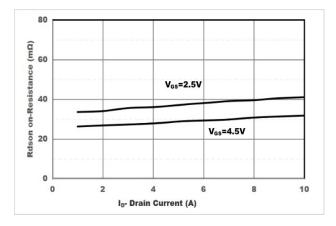


Figure5. Drain-Source on Resistance

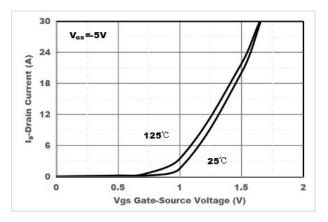


Figure2. Transfer Characteristics

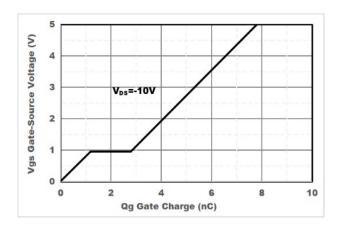


Figure4. Gate Charge

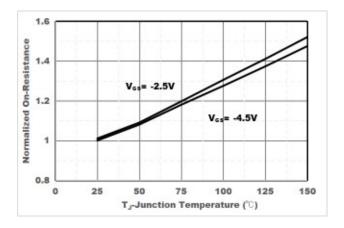
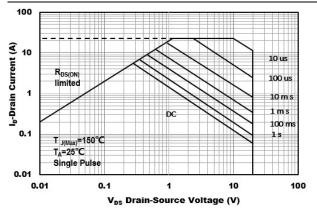


Figure6. Drain-Source on Resistance

# DP3415







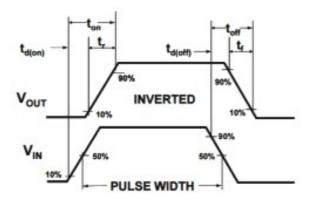
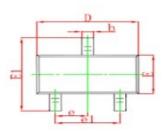
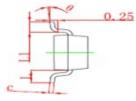
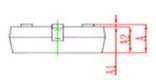


Figure8. Switching wave



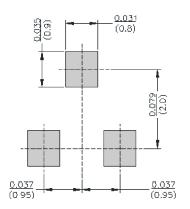






Cumhal	Dimentions in Millimeter		Dimentions in Inches		
Symbol	Min	Max	Min	Max	
Α	0.900	1.150	0.035	0.045	
A1	0.000	0.100	0.000	0.004	
A2	0.900	1.050	0.035	0.041	
b	0.300	0.500	0.012	0.020	
с	0.100	0.200	0.004	0.008	
D	2.800	3.000	0.110	0.118	
E	1.200	1.400	0.047	0.055	
E1	2.250	2.550	0.089	0.100	
е	0.950Type		0.037Type		
e1	1.800	2.000	0.071	0.079	
Ľ	0.550REF		0.220REF		
L1	0.300	0.500	0.012	0.020	
θ	0 °	8 °	0 °	8 °	

## SOT-23 Suggested Pad Layout





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