

FH8810

N- Channel Enhancement Mode Power MOSFET

Description

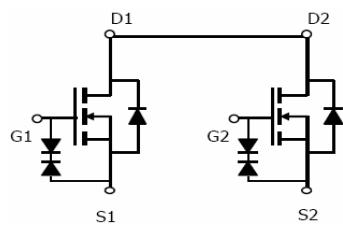
The FH8810 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 1.8V. This device is suitable for use as a load switch or in PWM applications. It is ESD protected.

Application

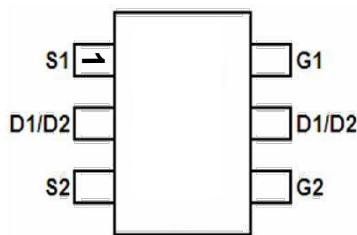
- Uni-directional load switch
- Bi-directional load switch

General Features

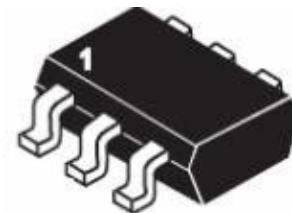
- $V_{DS} = 20V$, $I_D = 8A$
- $R_{DS(ON)} < 18 \text{ m}\Omega$ (MAX) @ $V_{GS} = 4.5V$
- $R_{DS(ON)} < 23 \text{ m}\Omega$ (MAX) @ $V_{GS} = 2.5V$
- ESD Rating : 2000V HBM
- High power and current handling capability
- Lead free product is acquired
- Surface mount package



Schematic diagram



Marking and pin Assignment



SOT23-6 top view

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain Source Voltage	V_{DS}	20	V
Gate Source Voltage	V_{GS}	± 8	V
Drain Current Continuous	I_D	8	A
Drain Current-Pulsed ^(Note 1)	I_{DM}	30	A
Maximum Power Dissipation	P_D	1.25	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	83	°C/W
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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	20			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=20\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm 8\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 10	μA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	0.4	0.7	1.0	V
Drain-Source On-State Resistance	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=4\text{A}$		15	18	$\text{m}\Omega$
		$V_{\text{GS}}=2.5\text{V}, I_{\text{D}}=3\text{A}$	-	19	23	$\text{m}\Omega$
		$V_{\text{GS}}=1.8\text{V}, I_{\text{D}}=3\text{A}$	-	23	29	$\text{m}\Omega$
Forward Transconductance	g_{FS}	$V_{\text{DS}}=5\text{V}, I_{\text{D}}=8\text{A}$	-	35	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{\text{DS}}=10\text{V}, V_{\text{GS}}=0\text{V}, F=1.0\text{MHz}$		1180		PF
Output Capacitance	C_{oiss}		-	230	-	PF
Reverse Transfer Capacitance	C_{rss}			200		PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{\text{d(on)}}$	$V_{\text{DD}}=10\text{V}, R_{\text{L}}=1.2\Omega, V_{\text{GS}}=8\text{V}, R_{\text{GEN}}=3\Omega$	-	2.5		nS
Turn-on Rise Time	t_r		-	7.2		nS
Turn-Off Delay Time	$t_{\text{d(off)}}$		-	49		nS
Turn Off Fall Time	t_f		-	10.8		nS
Total Gate Charge	Q_g	$V_{\text{DS}}=10\text{V}, I_{\text{D}}=8\text{A}, V_{\text{GS}}=4.5\text{V}$	-	17.9		nC
Gate-Source Charge	Q_{gs}		-	1.5	-	nC
Gate-Drain Charge	Q_{gd}		-	4.7	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{\text{GS}}=0\text{V}, I_{\text{s}}=1\text{A}$	-	-	1.2	V
Diode Forward Current ^(Note 2)	I_{s}		-	-	3	A

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

Typical Electrical and Thermal Characteristics

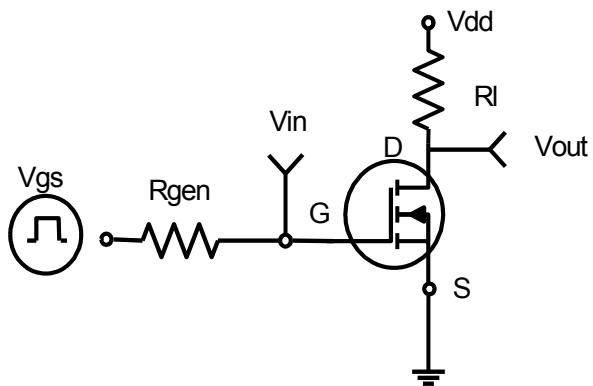


Figure 1:Switching Test Circuit

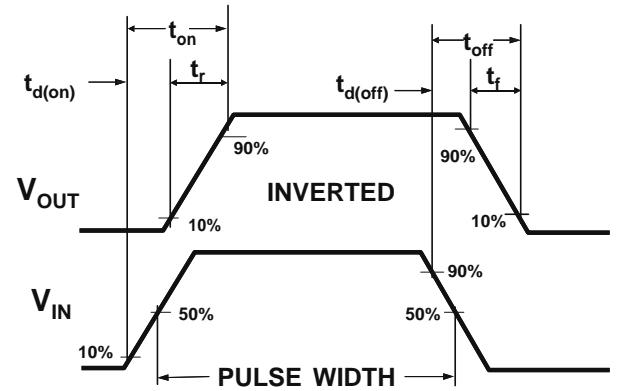


Figure 2:Switching Waveforms

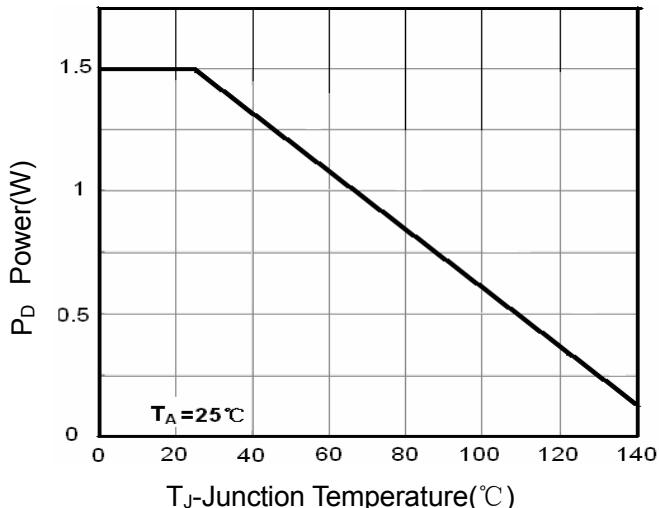


Figure 3 Power Dissipation

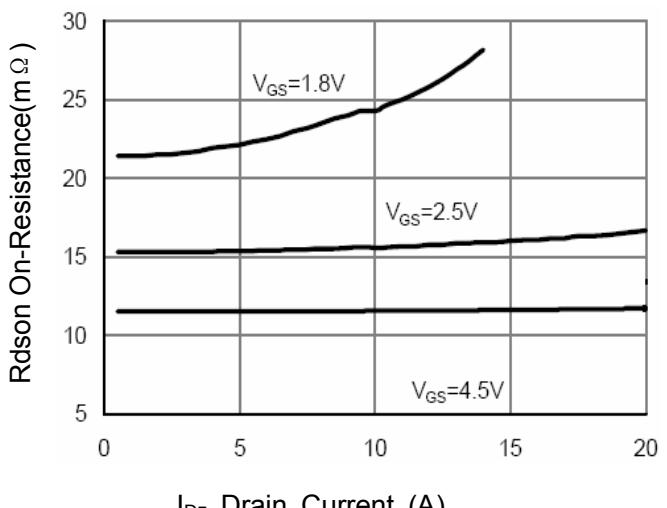


Figure 6 Drain-Source On-Resistance

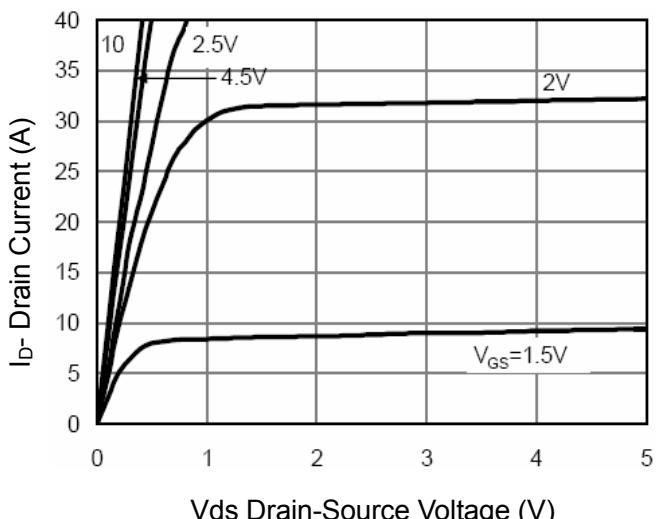


Figure 5 Output Characteristics

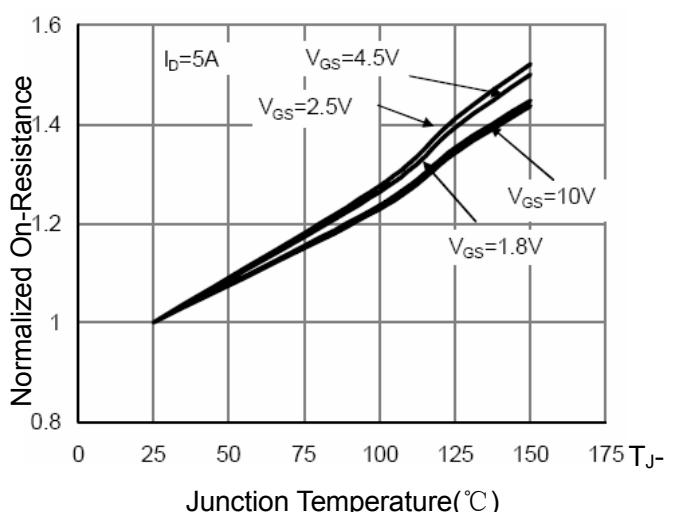


Figure 8 Drain-Source On-Resistance

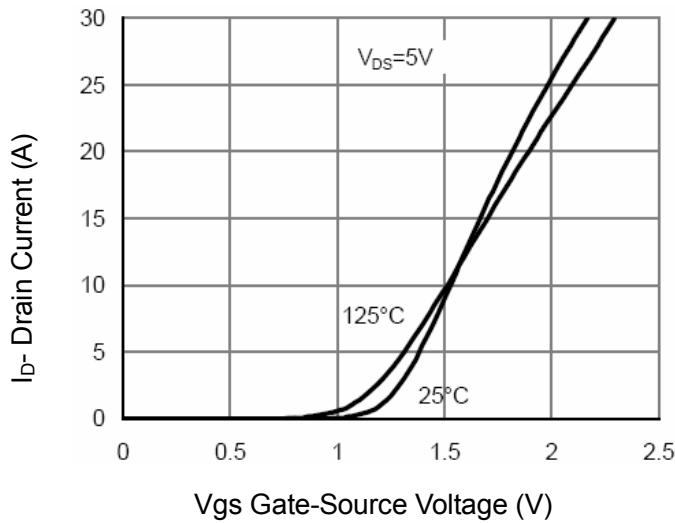
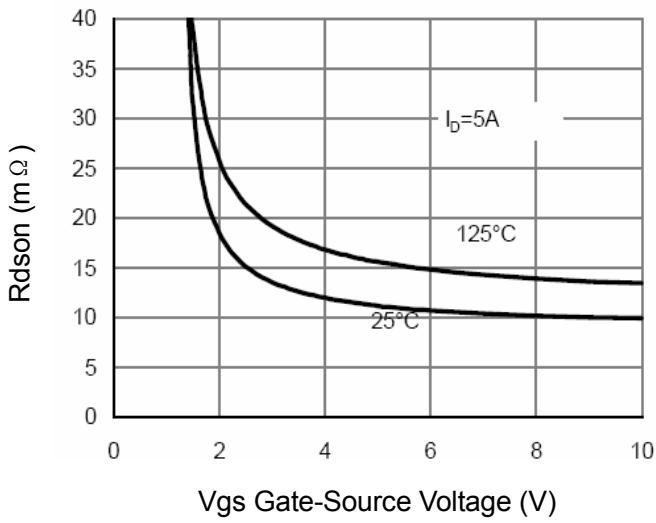
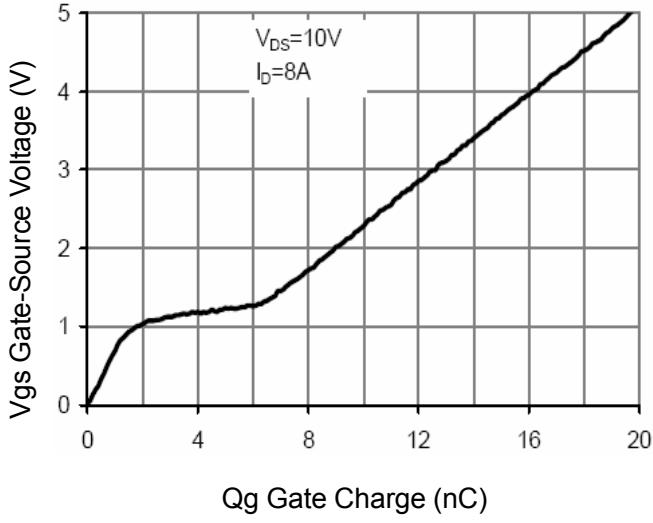


Figure 7 Transfer Characteristics



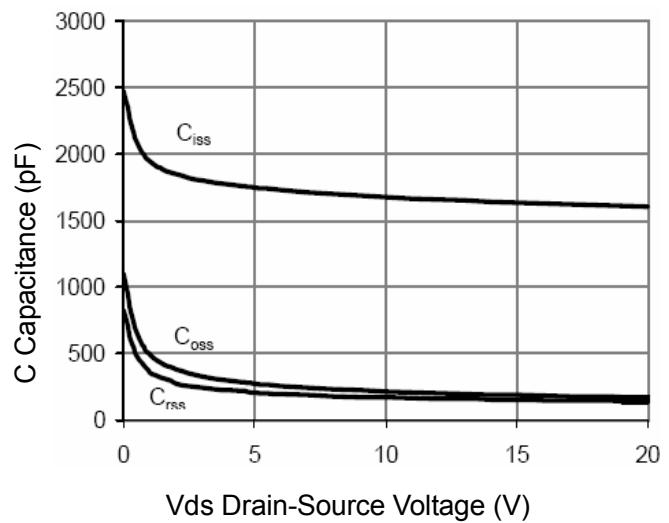
Vgs Gate-Source Voltage (V)

Figure 9 $R_{DS(on)}$ vs V_{GS}



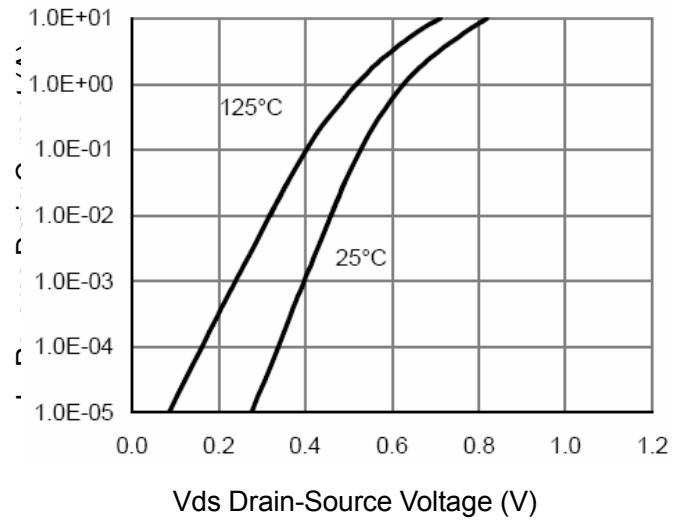
Qg Gate Charge (nC)

Figure 11 Gate Charge



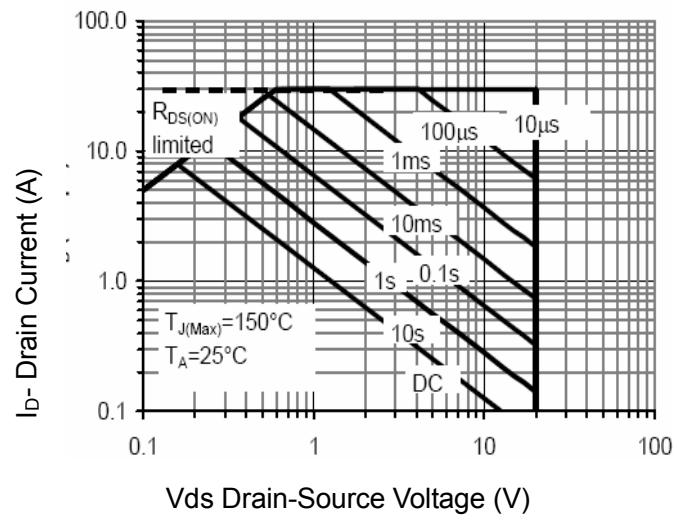
Vds Drain-Source Voltage (V)

Figure 8 Capacitance vs V_{DS}



Vds Drain-Source Voltage (V)

Figure 10 Capacitance vs V_{DS}



Vds Drain-Source Voltage (V)

Figure 13 Safe Operation Area

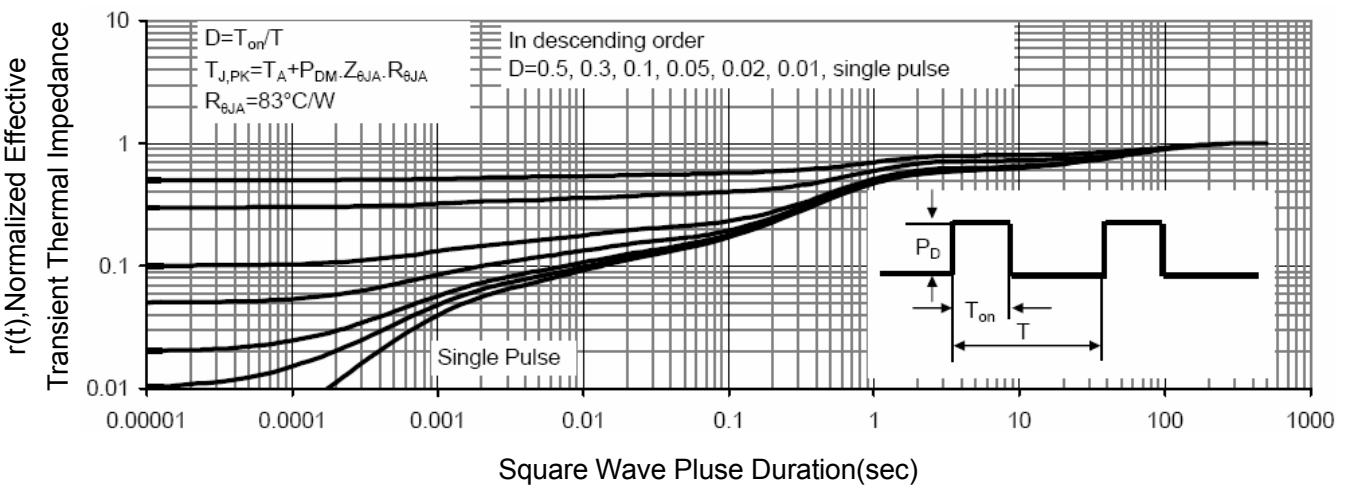
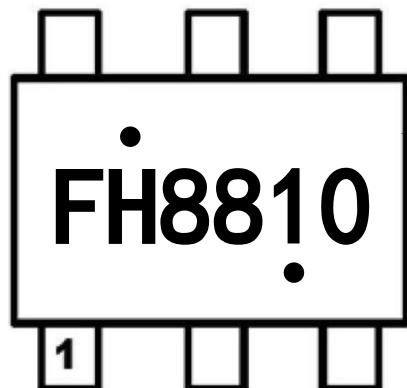


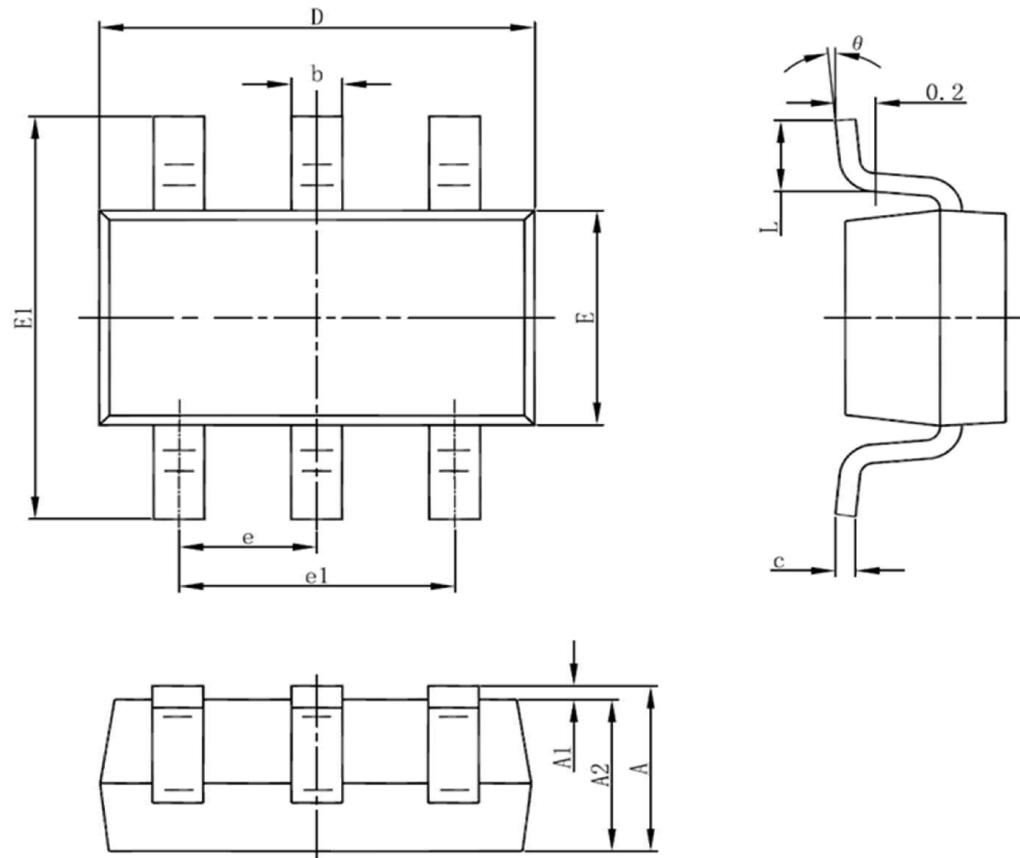
Figure 14 Normalized Maximum Transient Thermal Impedance

MARKING DESCRIPTION

SOT23-6



Note: The printing points above and below the product model are the internal identification of the company. Each batch of products may be in different locations.

Package Information : SOT23-6

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°