

FEATURES

- **CMOS DUAL CHANNEL 8bit 40MHz DAC**
- **LOW POWER DISSIPATION: 180mW(+3V)**
- **DIFFERENTIAL NONLINEARITY ERROR: 0.5LSB**
- **SIGNAL-to-NOISE RATIO: 51dB**
- **SPURIOUS-FREE DYNAMIC RANGE:68dB**
- **BUILD-IN DIGITAL ENGINE for VIDEO PERFORMANCE ENHANCEMENT**
- **SINGLE 3.3V POWER SUPPLY**
- **PIN COMPATIBLE WITH SC9766**
- **24-PIN SSOP PB-FREE PACKAGE**

DESCRIPTION

The SC9767 is a dual channel 8bit 40MHz digital to analog converter with digital video engine. The two channels of SC9767 are close matching for the communication application with I/Q channel data transmission. The SC9767 integrates dual 8-bit, 40MHz, DACs, a digital video engine, a voltage reference and the digital input latches.

The I and Q input are combined to only 8 pins for pin count reduction. The digital input latches of SC9767 are used to split the 8bit input to original I and Q data. The output of latches serves as the input of digital filters and the 8-bit DACs convert the output of filters to analog current output.

Combined with a proprietary switching technique and segmented current source architecture, the DACs

dramatically reduce spurious components and enhance dynamic performance. Coming with the integrated StediChips' 4th generation Digital Video Engine (DVE), The SC9767 along with SC9207(ADC) and SC6362(SD video filter) provide Video Transceiver designers a great choice to achieve superior video indicator, especially lower and stable noise performance.

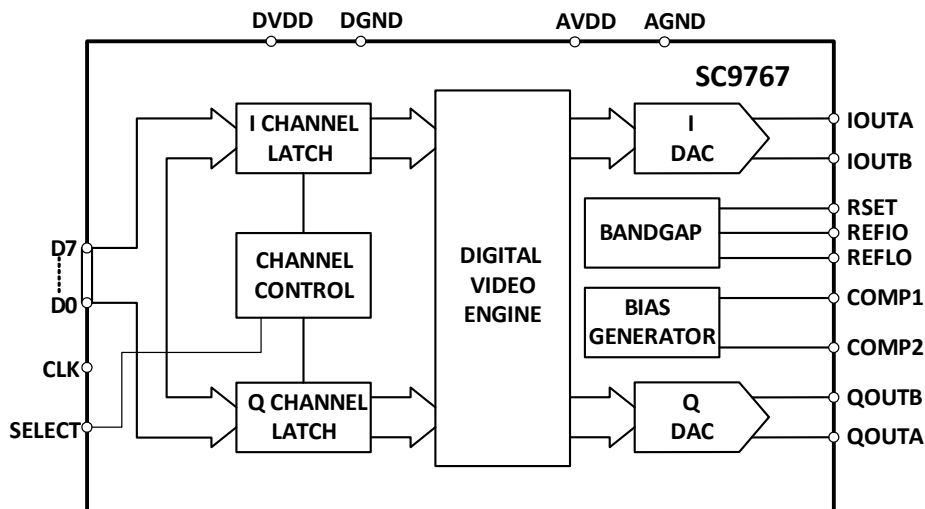
A built-in 1.2V temperature compensated bandgap reference provides the costumers an easy and cost-saving choice.

The SC9767 operates at single power supply from 2.7V to 3.6V. The power dissipation of SC9767 is only 180mW at 3V voltage supply and less than 3mW when power down.

The SC9767 is developed for high performance low-voltage applications. It's specified over the industrial (-40°C to +85°C) or commercial (0°C to +70°C) temperature ranges.

PRODUCT HIGHLIGHTS

- **DUAL 8BIT 40MHz DACS WITH EXCELENT PERFORMANCE**
- **PIN COMPATIBLE WITH SC9766**
- **ENHANCED VIDEO PERFORMANCE FOR OPTIC TRANSMISSION SYSTEM**
- **ON-CHIP REFERENCE**
- **LOW POWER DISSIPATION: 180mW (3V SUPPLY)**
- **HIGH ESD CAPABILITY (>8000V HBM)**

FUNCTIONAL BLOCK DIAGRAM


REV. 1.0.1

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DC ELECTRICAL CHARACTERISTICS

(AVDD = 3.3 V, DVDD=3.3V, I_{OUTFS}=10mA, Internal Reference, T_A = +25°C)

| PARAMETER | MIN | TYP | MAX | UNITS |
|--|---|-------|-------|----------|
| RESOLUTION | | | 8 | Bits |
| MONOTONICITY | GUARANTEED OVER SPECIFIED TEMPERATURE RANGE | | | |
| DC ACCURACY | | | | |
| Differential Nonlinearity (DNL) | -1 | ±0.25 | +1 | LSB |
| Integral Nonlinearity (INL) | -1 | ±0.3 | +1 | LSB |
| ANALOG OUTPUT | | | | |
| Offset Error | -1.5 | ±0.5 | +1.5 | % of FSR |
| Gain Error(Without Internal Reference) | -5 | ±1.2 | +5 | % of FSR |
| Gain Error(With Internal Reference) | -5 | ±1.2 | +5 | % of FSR |
| Gain Matching between DACs | -1.0 | ±0.4 | +1.0 | % of FSR |
| Full-Scale Output Current | 1 | 10 | | mA |
| Output Compliance Range | -1.0 | | +1.24 | V |
| Output Resistor | | 100 | | kΩ |
| Output Capacitance | | 5 | | pF |
| REFERENCE OUTPUT | | | | |
| Reference Voltage | 1.1 | 1.2 | 1.3 | V |
| Reference Output Current | | 100 | | nA |
| REFERENCE INPUT | | | | |
| Input Compliance Range | 0.1 | | 1.25 | V |
| Reference Input Resistance (Ext. Ref) | | 1 | | MΩ |
| Small Signal Bandwidth | | 1.5 | | MHz |
| POWER SUPPLY | | | | |
| Operating Voltage — AVDD | 2.7 | 3 | 3.6 | V |
| Operating Voltage — DVDD | 2.7 | 3 | 3.6 | V |
| Analog Supply Current(I _{AVDD}) ¹ | | 23 | 27 | mA |
| Digital Supply Current (I _{DVDD}) ² | | 37 | 40 | mA |
| Supply Current Sleep Mode (I _{AVDD}) | | | 1 | mA |
| Power Consumption—P _D | | 180 | 201 | mW |
| Power Supply Rejection Ratio | | 1 | | % of FSR |
| OPERATING RANGE | -40 | | +85 | °C |

NOTES

¹AVDD=3V DVDD=3V

²Measured at F_{clk}=40MHz and F_{out}=1MHz

DYNAMIC SPECIFICATIONS

(AVDD = 3.3 V, DVDD=3.3V, F_{CLK}=40MSPS, I_{OUTFS}=10mA, T_A = +25°C)

| PARAMETER | MIN | TYP | MAX | UNITS |
|---|-----|------|-----|--------|
| DYNAMIC PERFORMANCE | | | | |
| Maximum Output Update Rate | | 40 | | MHz |
| Output Settling Time (t _{ST}) | | 30 | | ns |
| Glitch Impulse | | 5 | | pV-s |
| Output Rise Time (10% to 90%) | | 2.5 | | ns |
| Output Fall Time (90% to 10%) | | 2.5 | | ns |
| AC LINEARITY | | | | |
| Signal-to-Noise and Distortion Ratio (SINAD) | | | | |
| f = 1.01MHz | | 49.5 | | dB |
| Signal-to-Noise Ratio (SNR) | | | | |
| f = 1.01MHz | | 51 | | dB |
| Spurious Free Dynamic Range (SFDR) | | | | |
| f = 1.01MHz | | 68 | | dBc |
| Total Harmonic Distortion (THD) | | | | |
| f = 1.01MHz | | -66 | | dBc |
| Differential Phase | | 0.2 | | Degree |
| Differential Gain | | 0.1 | | % |
| DIGITAL INPUT | | | | |
| High Input Voltage | 2.4 | | | V |
| Low Input Voltage | | | 1 | V |
| Logic 1 Current | -10 | | +10 | μA |
| Logic 0 Current | -10 | | +10 | μA |
| Input Capacitance | | 5 | | pF |
| Data Input Setup Time (t _{SD}) | | 3 | | ns |
| Data Input Hold Time (t _{HD}) | | 2 | | ns |
| Select Input Setup Time (t _{SS}) | | 4 | | ns |
| Select Input Hold Time (t _{HS}) | | 2 | | ns |

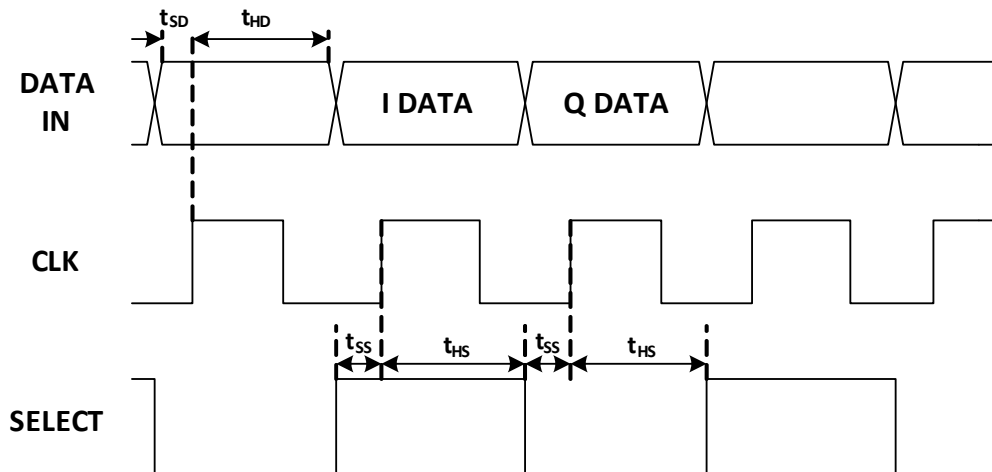


Figure 1. DAC Timing

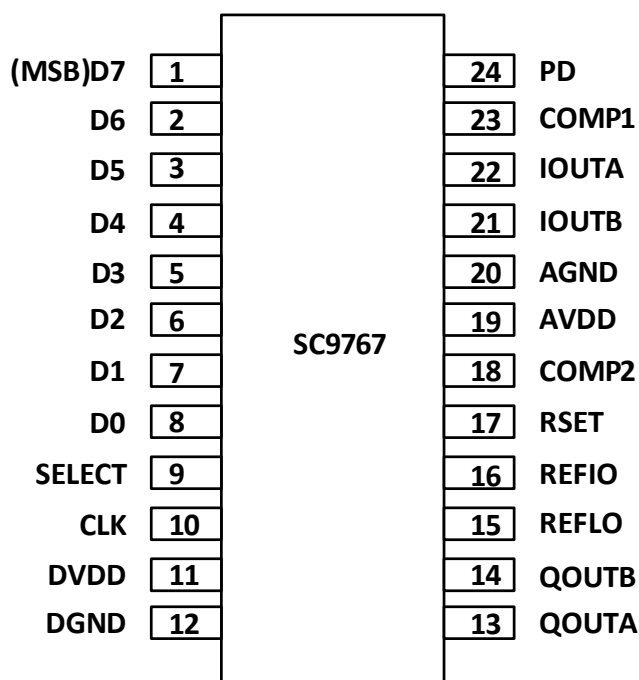
PIN CONFIGURATION


Figure2. Pin Configuration

Table 1. Pin Function Descriptions

| Pin No. | Name | Function Description |
|---------|---------------|--|
| 1 | D7 | Most Significant Data Bit (MSB) |
| 2-7 | D6-D1 | Data Bits 1-6 |
| 8 | D0 | Least Significant Data Bit (LSB) |
| 9 | SELECT | Select Input. Select high routes input data to I DAC; select low routes data to Q DAC |
| 10 | CLK | Clock Input. DAC input registers latched on positive edge of clk |
| 11 | DVDD | Digital Supply Voltage (normal 3.3V) |
| 12 | DGND | Digital Ground |
| 13 | QOUTA | Q DAC Current Output. Full-scale current when all data bits are 1s |
| 14 | QOUTB | Q DAC Complementary Current Output. Full-scale current when all data bits are 0s |
| 15 | REFLO | Reference Ground when Internal 1.2V Reference Used. Connect to AVDD to disable internal reference |
| 16 | REFIO | Reference Input/ Output. Acts as 1.2V reference output when internal reference activated. Requires 0.1μF capacitor to AGND when internal reference activated. Acts as reference input when internal reference disabled |
| 17 | RSET | Full-Scale Current Output Adjust. Resistance to AGND sets full-scale output current |
| 18 | COMP2 | Bandwidth/Noise Reduction Node. Add 0.1μF capacitor to AVDD for optimum performance |
| 19 | AVDD | Analog Supply Voltage (normal 3.3V) |
| 20 | AGND | Analog Ground |
| 21 | IOUTB | I DAC Complementary Current Output. Full-scale current when all data bits are 0s |
| 22 | IOUTA | I DAC Current Output. Full-scale current when all data bits are 1s |
| 23 | COMP1 | Internal Bias Node for Switch Driver Circuitry. Decouple to AGND with 0.1μF capacitor |
| 24 | PD | Power-Down Control Input. Active High |

DEFINITIONS OF SPECIFICATIONS

Linearity Error (Integral Nonlinearity or INL)

Linearity error is as the measure of the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (or DNL)

DNL is defined as the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity

As the digital input increases, if the output will never decreases, A D/A converter is monotonic.

Gain Error

The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s.

Offset Error

Offset Error is the measure of deviation of the output current from the ideal of zero when the inputs of D/A are all 0s.

Output Compliance Range

The maximum allowable voltage range measured at the D/A's output. Nonlinear performance might occur when the output voltage is beyond this limit.

Temperature Drift

Temperature drift indicates the influence of temperature. it measures the deviation of the value at either TMIN or TMAX with the reference value at 25°C. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per °C. For reference drift, the drift is reported in ppm per °C.

Power Supply Rejection

Power Supply Rejection indicates the influence of

variation of Power supply to the output. It is the ratio of the output change in the full-scale to the Power Supply change.

Settling Time

The time required for the output from the start of the output transition to reach and remain within a specified error band about its final value.

Glitch Impulse

Glitch Impulse is specified as the net area of the glitch in pV-s.

Spurious-Free Dynamic Range

SFDR is defined as the ratio in dB of the RMS value of the maximum signal component to the RMS value of the next largest noise or harmonic distortion component.

Total Harmonic Distortion

THD is the ratio in dB of the RMS sum of the first six harmonic components to the RMS value of the measured input signal.

Digital Video Engine

The Digital Video Engine (DVE) that is built in the SC9767 is part of the StediChips' Video Enhancement Algorithm (the rest part is carried by SC9207), which is optimized for optical video transmission system. Combining the SC9207 and the SC9767, the algorithm is complete and can fully function. By calibrating the inevitable distortion coming from transmission, the Video Enhancement Algorithm (VEA) may achieve an excellent video performance, especially for amplitude-frequency characteristic, chroma-luminance-gain-inequity and noise performance. The SC9767 can also be used alone or in pair with ADC without DVE, such as SC9204 (ADC without DVE inside). StediChips recommend the customers use SC9767, SC9207 and SC6362 together for optimal performance.

APPLICATION INFORMATION

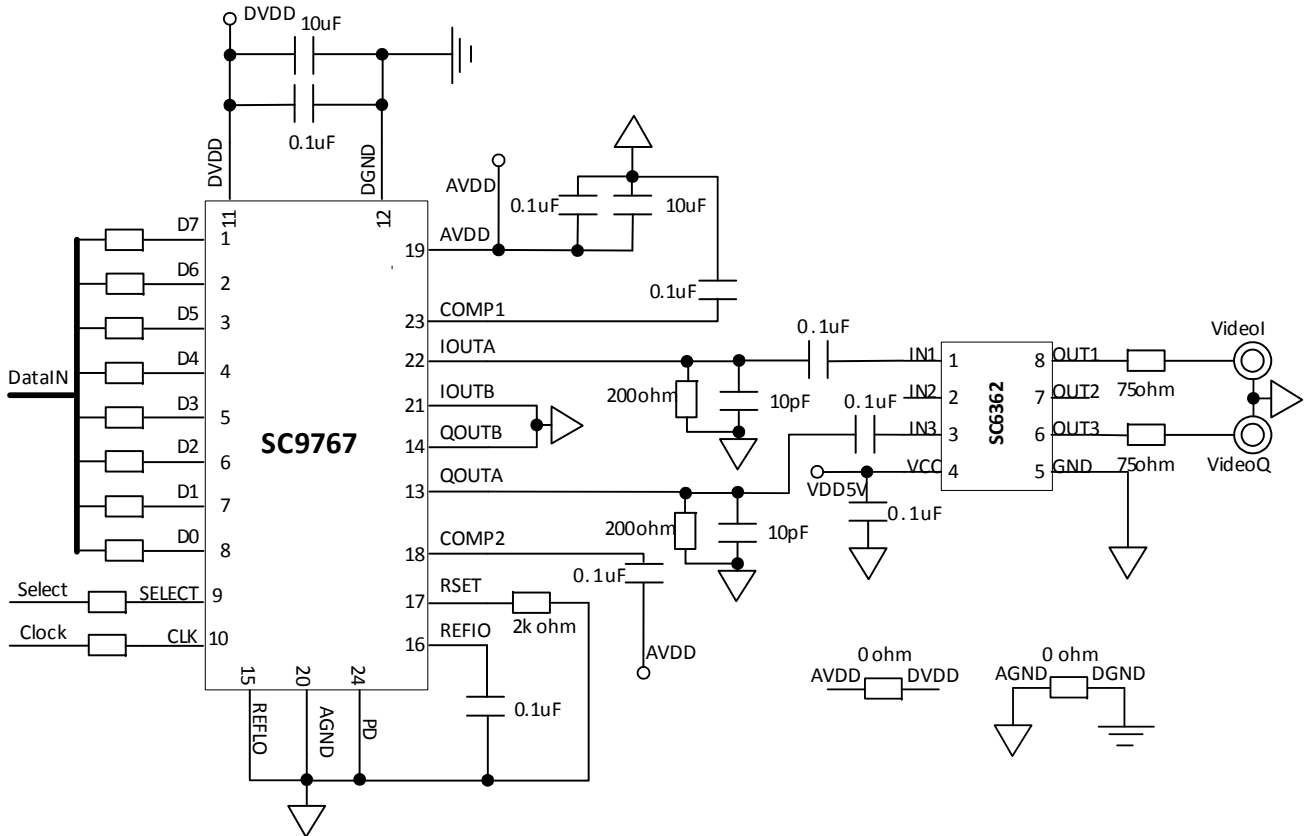


Figure 3. Application Schematic

MECHINAL DATA

24-LEAD SHRINK SMALL OUTLINE PACKAGE (SSOP24)

Table 2. Package information

| DIMENSIONS | | | |
|------------|---------|------|------|
| REF. | mm | | |
| | MIN. | TYP. | MAX. |
| A | - | - | 1.73 |
| A1 | 0.05 | - | 0.23 |
| A2 | 1.40 | - | 1.60 |
| b | 0.22 | - | 0.38 |
| c | 0.09 | - | 0.25 |
| D | 8.00 | 8.20 | 8.40 |
| E | 7.60 | 7.80 | 8.00 |
| E1 | 5.10 | 5.30 | 5.50 |
| e | 0.65BSC | | |
| K | 0° | - | 8° |
| L | 0.55 | - | 0.95 |



SSOP24

