

FEATURES

- **CMOS DUAL CHANNEL 8bit 40MHz DAC**
- **LOW POWER DISSIPATION: 105mW(+3V)**
- **DIFFERENTIAL NONLINEARITY ERROR: 0.3LSB**
- **SIGNAL-to-NOISE RATIO: 49dB**
- **SPURIOUS-FREE DYNAMIC RANGE:66dB**
- **SINGLE 3.3V POWER SUPPLY**
- **LOW POWER STANDBY MODE**
- **16-PIN SOP PB-FREE PACKAGE**

DESCRIPTION

The SC9765 is a dual channel 8bit 40MHz digital to analog converter. The two channels of SC9765 are close matching with I/Q channel data transmission. The SC9765 integrates dual 8-bit, 40MHz, DACs, a voltage reference and the digital input latches.

The I and Q input are combined to only 8 pins for pin count reduction. The digital input latches of SC9765 are used to split the 8bit input to original I and Q data. The output of latches serves as the input of digital filters and the 8-bit DACs convert the output of filters to analog current output.

Combined with a proprietary switching technique and segmented current source architecture, the DACs

dramatically reduce spurious components and enhance dynamic performance. The SC9765 along with SC9205(ADC) and SC6362(SD video filter) provide Video Transceiver designers a great choice to achieve excellent performance.

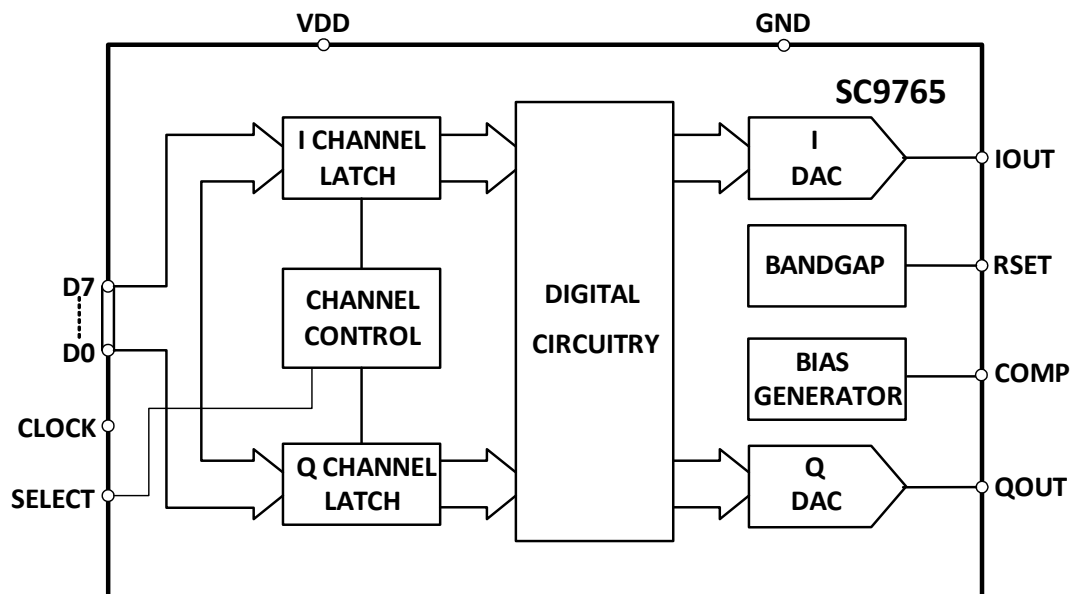
A built-in 1.2V temperature compensated bandgap reference provides the costumers an easy and cost-saving choice.

The SC9765 operates at single power supply from 2.7V to 3.6V. The power dissipation of SC9765 is only 120mW at 3V voltage supply and less than 3mW when power down.

The SC9765 is developed for low-cost low-power low-voltage applications. It's specified over the industrial (-40°C to +85°C) or commercial (0°C to +70°C) temperature ranges.

PRODUCT HIGHLIGHTS

- **DUAL 8BIT 40MHz DACS WITH EXCELENT DYNAMIC PERFORMANCE**
- **SINGLE 8BIT INPUT FOR PIN COUNT REDUCTION**
- **SIMPLEST APPLICATION SCHEMATIC**
- **LOW POWER DISSIPATION: 120mW (3V SUPPLY)**
- **HIGH ESD CAPABILITY (>8000V HBM)**

FUNCTIONAL BLOCK DIAGRAM


REV. 1.0.1

Information furnished by StediChips is believed to be accurate and reliable. However, no responsibility is assumed by StediChips for its use, or for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of StediChips

DC ELECTRICAL CHARACTERISTICS

(VDD=3.3V, I_{OUTFS}=10mA, Internal Reference, T_A = +25°C)

PARAMETER	MIN	TYP	MAX	UNITS
RESOLUTION			8	Bits
MONOTONICITY	GUARANTEED OVER SPECIFIED TEMPERATURE RANGE			
DC ACCURACY				
Differential Nonlinearity (DNL)	-1	±0.3	+1	LSB
Integral Nonlinearity (INL)	-1	±0.4	+1	LSB
ANALOG OUTPUT				
Offset Error	-1.5	±0.5	+1.5	% of FSR
Gain Error(Without Internal Reference)	-5	±1.2	+5	% of FSR
Gain Error(With Internal Reference)	-5	±1.2	+5	% of FSR
Gain Matching between DACs	-1.0	±0.4	+1.0	% of FSR
Full-Scale Output Current	1	10		mA
Output Compliance Range	-1.0		+1.24	V
Output Resistor		100		kΩ
Output Capacitance		5		pF
POWER SUPPLY				
Operating Voltage — VDD	2.7	3	3.6	V
Supply Current(I _{VDD}) ¹		35	38	mA
Power Consumption—P _D		105	114	mW
Power Supply Rejection Ratio		1		% of FSR
OPERATING RANGE	-40		+85	°C

NOTES

¹VDD=3V

²Measured at F_{clk}=40MHz and F_{out}=1MHz

DYNAMIC SPECIFICATIONS

(VDD=3.3V, F_{CLK}=40MSPS, I_{OUTFS}=10mA, T_A = +25°C)

PARAMETER	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE				
Maximum Output Update Rate		40		MHz
Output Settling Time (t _{ST})		30		ns
Glitch Impulse		5		pV-s
Output Rise Time (10% to 90%)		2.5		ns
Output Fall Time (90% to 10%)		2.5		ns
AC LINEARITY				
Signal-to-Noise and Distortion Ratio (SINAD)				
f = 1.01MHz		49		dB
Signal-to-Noise Ratio (SNR)				
f = 1.01MHz		50		dB
Spurious Free Dynamic Range (SFDR)				
f = 1.01MHz		66		dBc
Total Harmonic Distortion (THD)				
f = 1.01MHz		-65		dBc
Differential Phase		0.2		Degree
Differential Gain		0.1		%
DIGITAL INPUT				
High Input Voltage	2.4			V
Low Input Voltage			1	V
Logic 1 Current	-10		+10	μA
Logic 0 Current	-10		+10	μA
Input Capacitance		5		pF
Data Input Setup Time (t _{SD})		5		ns
Data Input Hold Time (t _{HD})		2		ns
Select Input Setup Time (t _{SS})		4		ns
Select Input Hold Time (t _{HS})		2		ns

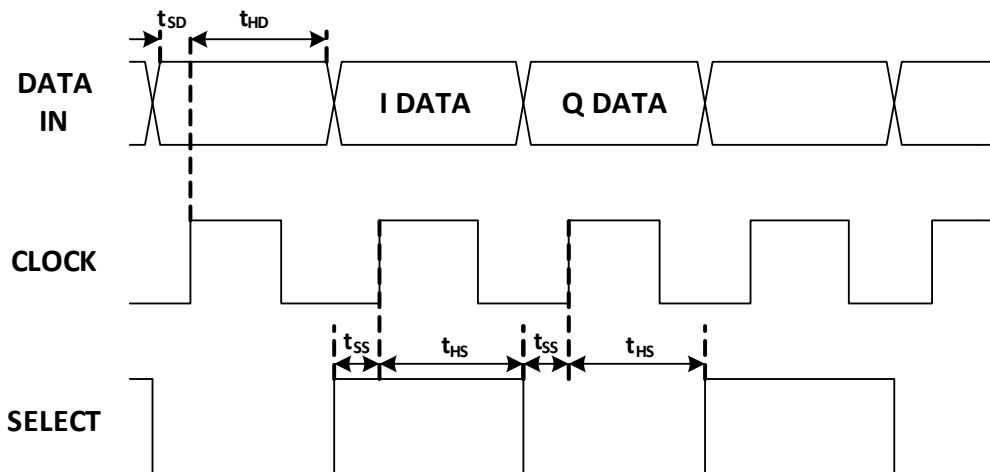


Figure 1. DAC Timing

PIN CONFIGURATION

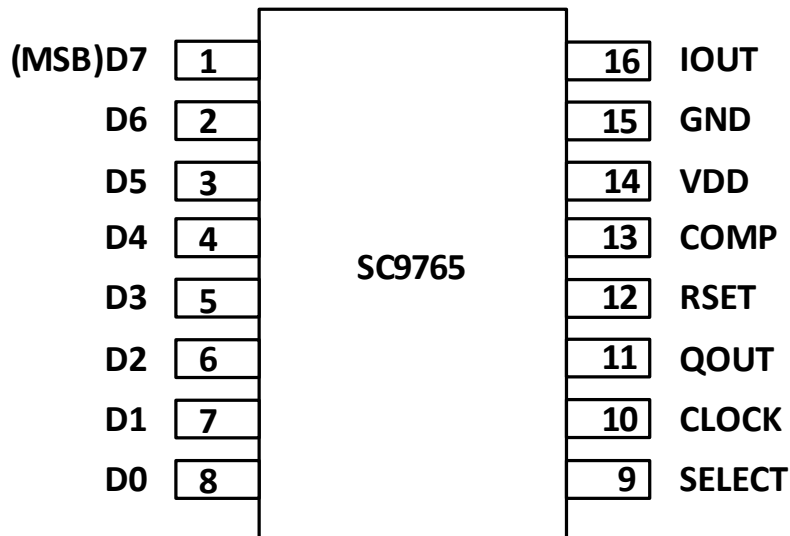


Figure2. Pin Configuration

Table 1. Pin Function Descriptions

Pin No.	Name	Function Description
1	D7	Most Significant Data Bit (MSB)
2-7	D6-D1	Data Bits 1-6
8	D0	Least Significant Data Bit (LSB)
9	SELECT	Select Input. Select high routes input data to I DAC; select low routes data to Q DAC
10	CLOCK	Clock Input. DAC input registers latched on positive edge of clk
11	QOUT	Q DAC Current Output. Full-scale current when all data bits are 1s
12	RSET	Full-Scale Current Output Adjust. Resistance to GND sets full-scale output current
13	COMP	Bandwidth/Noise Reduction Node. Add 0.1µF capacitor to VDD for optimum performance
14	VDD	Supply Voltage (normal 3.3V)
15	GND	Ground
16	IOOUT	I DAC Current Output. Full-scale current when all data bits are 1s

DEFINITIONS OF SPECIFICATIONS

Linearity Error (Integral Nonlinearity or INL)

Linearity error is as the measure of the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (or DNL)

DNL is defined as the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity

As the digital input increases, if the output will never decreases, A D/A converter is monotonic.

Gain Error

The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s.

Offset Error

Offset Error is the measure of deviation of the output current from the ideal of zero when the inputs of D/A are all 0s.

Output Compliance Range

The maximum allowable voltage range measured at the D/A's output. Nonlinear performance might occur when the output voltage is beyond this limit.

Temperature Drift

Temperature drift indicates the influence of

temperature. it measures the deviation of the value at either TMIN or TMAX with the reference value at 25°C. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per °C. For reference drift, the drift is reported in ppm per °C.

Power Supply Rejection

Power Supply Rejection indicates the influence of variation of Power supply to the output. It is the ratio of the output change in the full-scale to the Power Supply change.

Settling Time

The time required for the output from the start of the output transition to reach and remain within a specified error band about its final value.

Glitch Impulse

Glitch Impulse is specified as the net area of the glitch in pV-s.

Spurious-Free Dynamic Range

SFDR is defined as the ratio in dB of the RMS value of the maximum signal component to the RMS value of the next largest noise or harmonic distortion component.

Total Harmonic Distortion

THD is the ratio in dB of the RMS sum of the first six harmonic components to the RMS value of the measured input signal.

APPLICATION INFORMATION

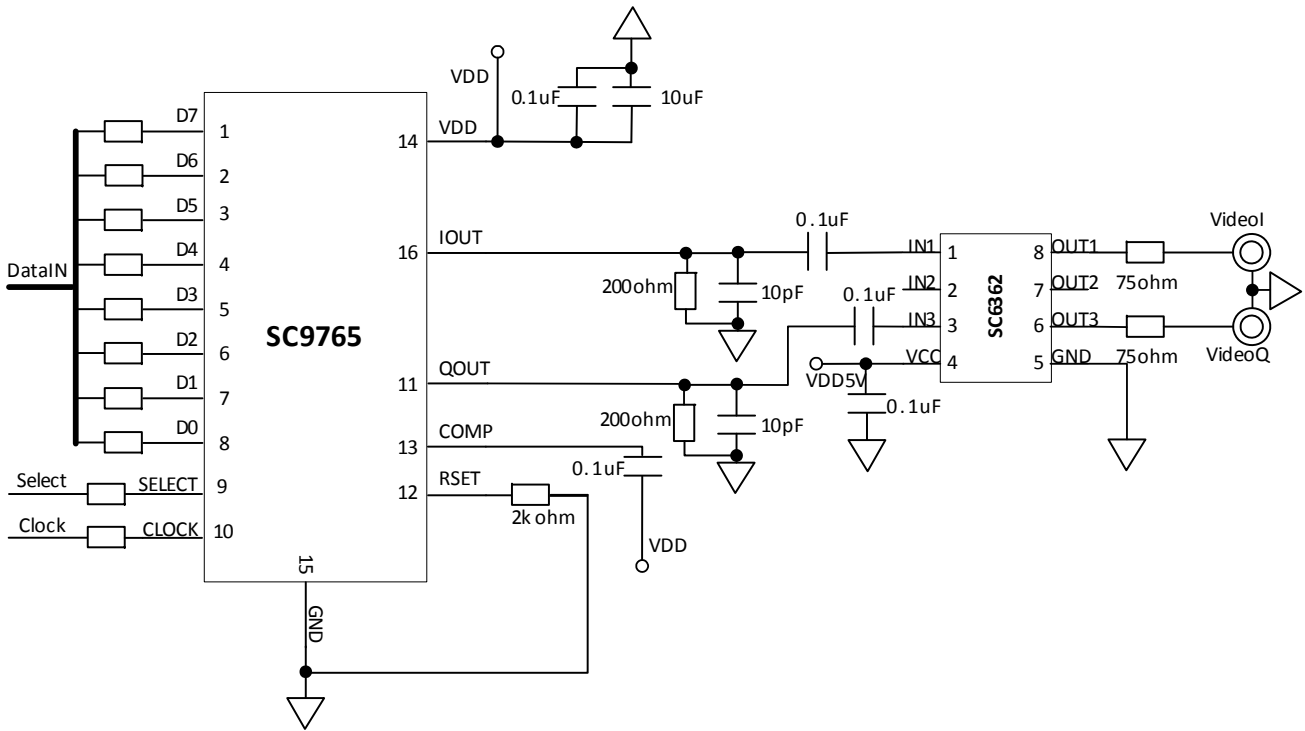


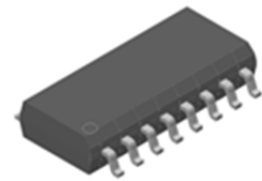
Figure 3. Application Schematic

MECHINAL DATA

16-LEAD SMALL OUTLINE PACKAGE (SOP16)

Table 2. Package information

DIMENSIONS			
REF.	mm		
	MIN.	TYP.	MAX.
A	-	-	1.75
A1	0.05	-	0.225
A2	1.30	1.40	1.50
b	0.39	-	0.48
b1	0.38	0.41	0.43
c	0.21	-	0.26
c1	0.19	0.20	0.21
D	9.70	9.90	10.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
θ	0°	-	8°
L	0.50	-	0.80
L1	1.05BSC		



SOP16

