SC9588

Low Cost, with Digital Video Engine 8-Bit 25MSPS 3.3V D/A Converter

FEATURES

- LOW-COST 8-BIT D/A CONVERTER
- EXCELLENT SPURIOUS-FREE DYNAMIC RANGE PERFORMANCE
- BUILD-IN STEADICHIPS' THIRD GENERATION DIGITAL VIDEO ENGINE
- DIFFERENTIAL CURRENT OUTPUT
- SINGLE 3.3V POWER SUPPLY
- LOW POWER CONSUMPTION
- 20-PIN SSOP PB-FREE PACKAGE

APPLICATIONS

- VIDEO APPLICATIONS
- WIDE BAND DATA COMMUNICATION
- MEDICAL IMAGING EQUIPMENT
- MEASUREMENT INSTRUMENTATION

DESCRIPTION

The SC9588 is an 8-bit resolution, wideband, low power, current-output CMOS digital-to-analog converter (DAC) with on-chip digital video processor. The SC9588's nominal full-scale output current is 10mA and the output impedance is greater than 100kΩ. As a member of ExDAC family, the SC9588 offers exceptional ac and dc performance while supporting data update rate up to 25MSPS.

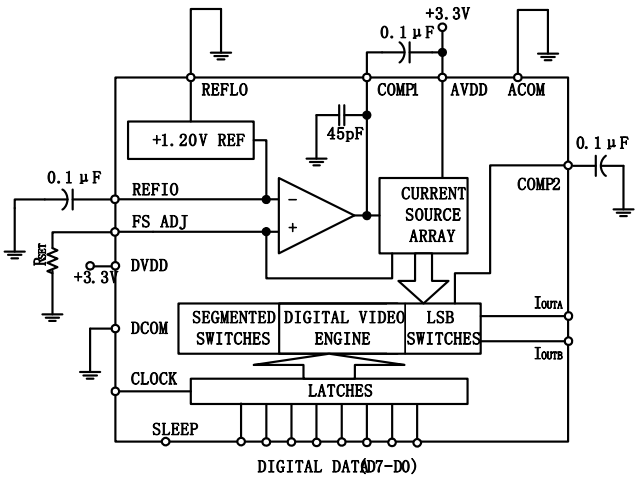
Coming with the integrated SteadiChips' 3rd generation Digital Video Engine (DVE), The SC9588 along with SC9087(ADC) and SC6362(SD video filter) provide Video Transceiver designers a great choice to achieve superior performance. The SC9588 is compatible with SC9518 in pin configuration except that the SC9588 needs the clock rate two times as high as the SC9518 does.

Featured low power dissipation , the SC9588 well suited for portable and low power applications. Its power dissipation can be further reduced to a mere 33mW with a slight degradation in performance by lowering the full-scale current output. Moreover, the SC9588 merely dissipates 3mW in power-down mode.

Combined with a proprietary switching technique and segmented current source architecture, the SC9588 dramatically reduce spurious components and enhance dynamic performance. Edge-triggered input latches and a built-in 1.2V temperature compensated bandgap reference provides the costumers an easy and cost-saving choice. The digital inputs support 3.3V CMOS logic families.

The SC9588 is specified over the industrial (–40°C to +85°C) and commercial (0°C to +70°C) temperature ranges.

FUNCTION BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

- MAXIMUM SAMPLING CLOCK FREQUENCY
  50MHz (25MHz DATA UPDATE RATE)
- RESOLUTION: 8Bit
- DNL/INL ±0.30LSB
- SFDR 67.5dB @ 1MHz OUTPUT
  59dB @ 10MHz OUTPUT
- 2.7~3.6V ANALOG POWER SUPPLY
  2.7~3.6V DIGITAL POWER SUPPLY
- ON-CHIP VOLTAGE REFERENCE
- DIFFERENTIAL CURRENT OUTPUT
- ADJUST SCALE FROM 1mA TO 10mA
- HIGH ESD CAPABILITY (>8000V HBM)

REV. 1.1.0

DC ELECTRICAL CHARACTERISTICS

(AVDD = 3.3V, DVDD = 3.3V, IOUTFS = 10mA, unless otherwise noted.)

PARAMETER	MIN	TYP	MAX	UNITS
RESOLUTION			8	Bits
MONOTONICITY	GUARANTEED OVER SPECIFIED TEMPERATURE RANGE			
DC ACCURACY[1]				
Differential Nonlinearity (DNL)	-0.6	±0.30	+0.6	LSB
Integral Nonlinearity (INL)	-0.8	±0.30	+0.8	LSB
ANALOG OUTPUT				
Offset Error	–0.02		+0.02	% of FSR
Gain Error (Without Internal Reference)	–10	±2	+10	% of FSR
Gain Error (With Internal Reference)	–5	±1	+5	% of FSR
Full-Scale Output Current	1		10	mA
Output Compliance Range	–1.0		+1.25	V
Output Resistance		100		kΩ
Output Capacitance		5		pF
REFERENCE OUTPUT				
Reference Voltage	1.10	1.20	1.30	V
Reference Output Current		100		nA
REFERENCE INPUT				
Input Compliance Range	0.1		1.25	V
Reference Input Resistance (Ext. Ref)		1		MΩ
Small Signal Bandwidth		1.5		MHz
TEMPERATURE COEFFICIENTS				
Offset Drift		0		ppm of FSR/℃
Gain Drift (Without Internal Reference)		±40		ppm of FSR/℃
Gain Drift (With Internal Reference)		±90		ppm of FSR/℃
Reference Voltage Drift		±40		ppm/℃
POWER SUPPLY				
Supply Voltages				
AVDD	2.7	3.3	3.6	V
DVDD	2.7	3.3	3.6	V
Analog Supply Current (I_{AVDD})		11.5	14	mA
Digital Supply Current (I_{DVDD})[2]		30	35	mA
Supply Current Sleep Mode (I_{AVDD})			1	mA
Power Dissipation(3.3V,I_{OUTFS}=10mA)		124.5	147	mW
Power Supply Rejection Ratio—AVDD	–0.5		+0.5	% of FSR/V
Power Supply Rejection Ratio—DVDD	–0.04		+0.04	% of FSR/V
OPERATING RANGE	–40		+85	℃

NOTES

1. Measured at I_{OUTA}, driving a virtual ground.
2. Measured at f_{CLOCK}=50MSPS and f_{OUT}=1.0MHZ; AVDD=3V, DVDD=3V.

DYNAMIC SPECIFICATIONS

(AVDD = 3.3V, DVDD = 3.3V, I_{OUTFS} = 10mA, Differential Transformer Coupled Output, 100Ω Doubly Terminated, unless otherwise noted.)

PARAMETER	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE				
Maximum Output Update Rate (f_{CLOCK})		50		MSPS
Output Settling Time (t_{ST}) (to 0.1%)[1]		30		ns
Output Propagation Delay (t_{PD})		1		ns
Glitch Impulse		5		pV-s
Output Rise Time (10% to 90%)[1]		2.5		ns
Output Fall Time (10% to 90%)[1]		2.5		ns
Output Noise (I_{OUTFS} = 10 mA)[2]		50		pA/√Hz
Output Noise (I_{OUTFS} = 1 mA)[2]		30		pA/√Hz
AC LINEARITY TO NYQUIST				
Signal-to-Noise and Distortion Ratio				
f_{CLOCK}=50MSPS; f_{OUT}=1.01MHz		51		dB
f_{CLOCK}=50MSPS; f_{OUT}=5.11MHz		49		dB
Spurious Free Dynamic Range				
f_{CLOCK}=50MSPS; f_{OUT}=1.01MHz		67.5		dBc
f_{CLOCK}=50MSPS; f_{OUT}=2.51MHz		65		dBc
f_{CLOCK}=50MSPS; f_{OUT}=5.11MHz		63		dBc
Total Harmonic Distortion				
f_{CLOCK}=50MSPS; f_{OUT}=1.01MHz		-65		dBc
f_{CLOCK}=50MSPS; f_{OUT}=2.51MHz		-64		dBc
f_{CLOCK}=50MSPS; f_{OUT}=5.11MHz		-62		dBc

NOTES

1. Measured single-ended into 100Ω load.

2. Output noise is measured with a full-scale output set to 10mA with no conversion activity. It is a measure of the thermal noise only.

DIGITAL CHARACTERISTICS

(AVDD = 3.3V, DVDD = 3.3V, I_{OUTFS} = 10mA, unless otherwise noted.)

PARAMETER	MIN	TYP	MAX	UNITS
DIGITAL INPUTS				
Logic "1" Voltage	2.1	3.3		V
Logic "0" Voltage		0	1.2	V
Logic "1" Current	-10		+10	μA
Logic "0" Current	-10		+10	μA
Input Capacitance		5		pF
Input Setup Time (t_S)	3.0			ns
Input Hold Time (t_H)	2.0			ns
Latch Pulse Width (t_{LPW})	1.5			ns

Specifications subject to change without notice

ORDERING GUIDE

Model	Temperature Range	Package Descriptions
SC9588AEH	-40°C to +85°C	20-Lead SSOP

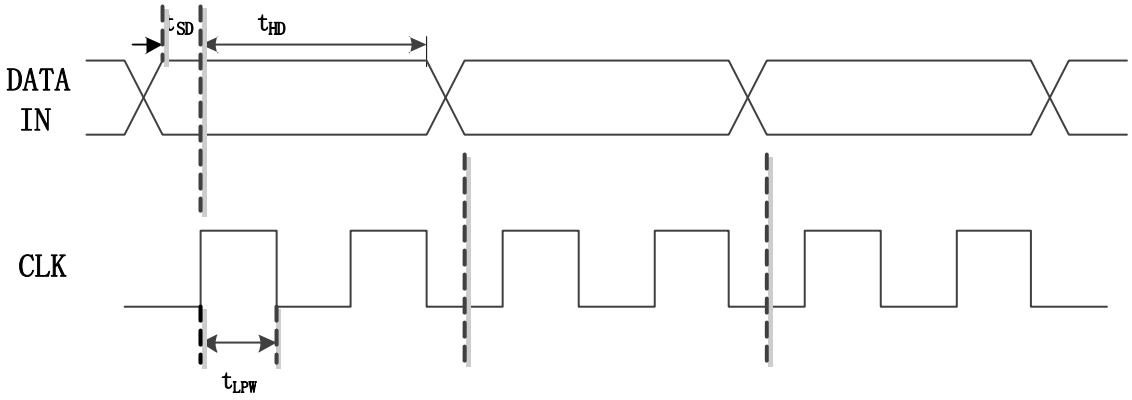
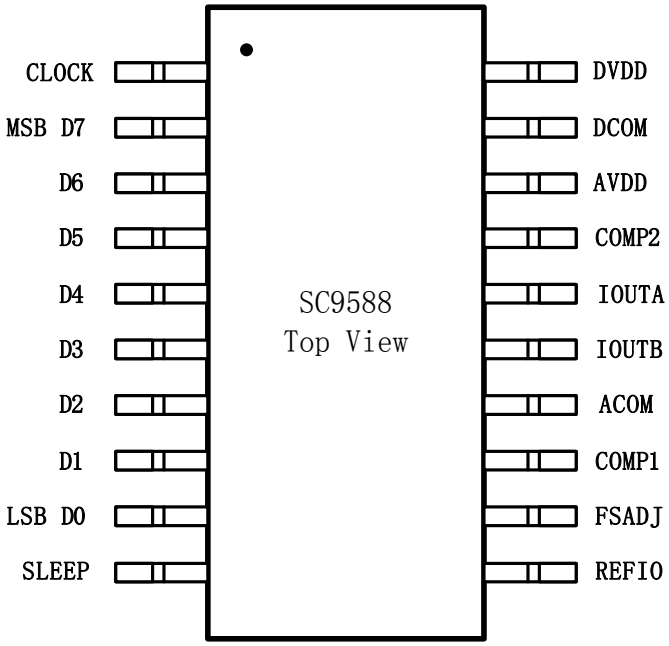


Figure 1. Timing Diagram

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Function
1	CLOCK	Clock Input. Data latched on positive edge of clock.
2	D7	Most Significant Data Bit (MSB).
3–8	D6–D1	Data Bits 1-6.
9	D0	Least Significant Data Bit (LSB).
10	SLEEP	Power-Down Control Input. Active High. A built-in pull-down circuit is attached.
11	REFIO	Reference Output. Requires 0.1uF capacitor to ACOM when internal reference activated.
12	FS ADJ	Full-Scale Current Output Adjust.
13	COMP1	Bandwidth/Noise Reduction Node. Add 0.1uF to AVDD for optimum performance.
14	ACOM	Analog Common.
15	IOUTB	Complementary DAC Current Output. Full-scale current when all data bits are 0s.
16	IOUTA	DAC Current Output. Full-scale current when all data bits are 1s.
17	COMP2	Internal Bias Node for Switch Driver Circuitry. Decouple to ACOM with 0.1uF capacitor.
18	AVDD	Analog Supply Voltage (nominal 3.3V).
19	DCOM	Digital Common.
20	DVDD	Digital Supply Voltage (nominal 3.3V).

DEFINITIONS OF SPECIFICATIONS

Linearity Error (Integral Nonlinearity or INL)

Linearity error is as the measure of the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (or DNL)

DNL is defined as the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code.

Monotonicity

As the digital input increases, if the output will never decreases, D/A converter is monotonic.

Gain Error

The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s.

Offset Error

Offset Error is the measure of deviation of the output current from the ideal of zero when the inputs of D/A are all 0s.

Output Compliance Range

The maximum allowable voltage range measured at the D/A's output. Nonlinear performance might occur when the output voltage is beyond this limit.

Temperature Drift

Temperature drift indicates the influence of temperature. It measures the deviation of the value at either TMIN or TMAX with the reference value at 25℃. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per ℃. For reference drift, the drift is reported in ppm per ℃.

Power Supply Rejection

Power Supply Rejection indicates the influence of variation of Power supply to the output. It is the ratio of the output change in the full-scale to the Power Supply change.

Settling Time

The time required for the output from the start of the output transition to reach and remain within a specified error band about its final value.

Glitch Impulse

Glitch Impulse is specified as the net area of the glitch in pV-s.

Spurious-Free Dynamic Range

SFDR is defined as the ratio in dB of the RMS value of the maximum signal component the RMS value of the next largest noise or harmonic distortion component.

Total Harmonic Distortion

THD is the ratio in dB of the RMS sum of the first six harmonic components to the RMS value of the measured input signal.

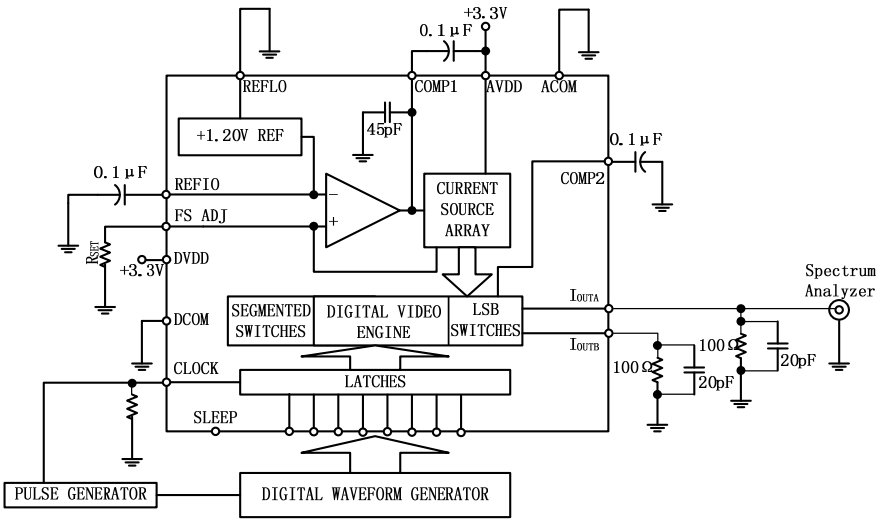


Figure 2. An AC Characterization Test Setup

Typical DC Characterization Curves (AVDD=3.3V, DVDD=3.3V, 100Ω Doubly Terminated Load, I_{OUTFS}=10mA, TA=+25°C, unless otherwise noted)

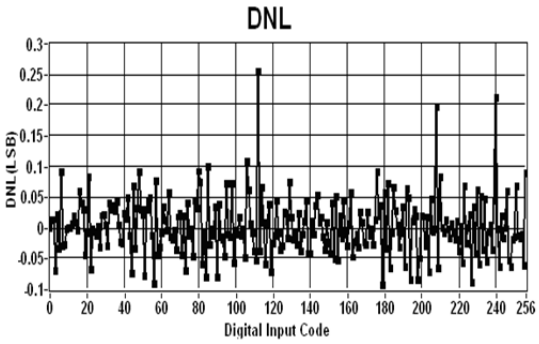


Figure 3. Typical DNL

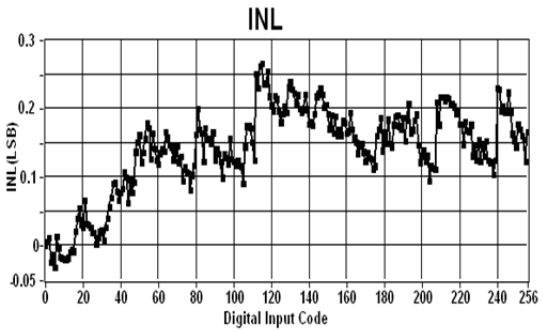


Figure 4. Typical INL

Typical AC Characterization Curves (AVDD=3.3V, DVDD=3.3V, 100Ω Doubly Terminated Load, I_{OUTFS}=10mA, TA=+25°C, unless otherwise noted)

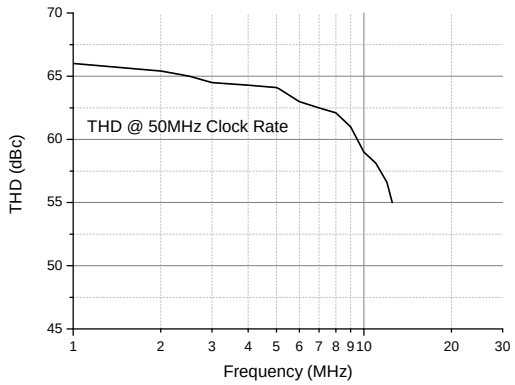


Figure 5. THD vs. f_{out} (AVDD and DVDD=3.3V)

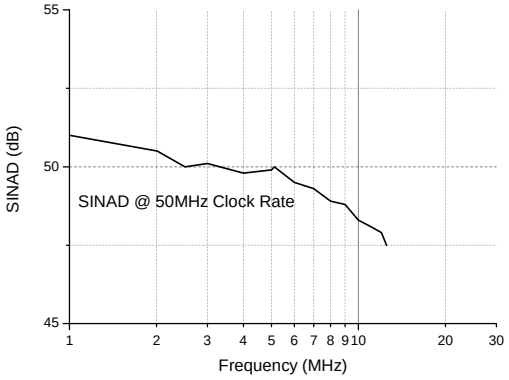


Figure 6. SINAD vs. f_{out} (AVDD and DVDD=3.3V)

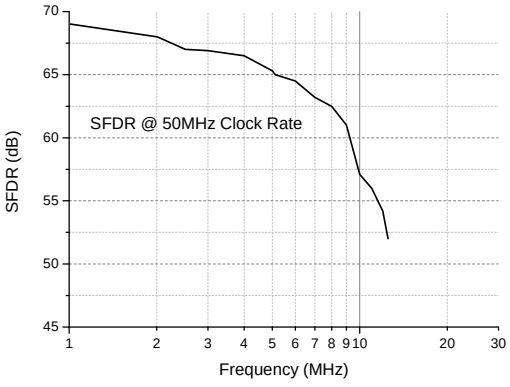


Figure 7. SFDR vs. f_{out} (AVDD and DVDD=3.3V)

FUNCTIONAL DESCRIPTION

Figure 8 shows a simplified block diagram of the SC9588. The SC9588 is capable of providing total current up to 10mA through a large PMOS current source array. The six most significant bits (MSBs) control 63 equal currents sub-array. The remaining 2 LSBs are also implemented with equally weighted current sources whose sum equals 3/4th of an MSB current source. Implementing the upper and lower bits with current sources helps maintain the high output impedance (i.e.>100k). All of these current sources are switched to either of two output nodes (i.e., IOUA or IOUTB) via PMOS differential current switches. A highly linearized PMOS current switch structure has been utilized to guarantee distortion performance.

The power supply inputs of analog section and digital section of the SC9588 are separated (i.e., AVDD and DVDD), each of them can operate independently over a 2.7Volt to 3.6Volt range.

The digital section mainly consists of edge-triggered latches and segment decoding logic circuitry. The analog section includes the PMOS current sources, the associated differential switches, a 1.20V bandgap voltage reference and a reference control amplifier.

The full-scale output current is regulated by the reference control amplifier and voltage reference V_{REFIO}. By properly setting the reference current I_{REF}, the full-scale output current has been reached great performance.

The SC9588 is capable of operating up to a 50MSPS clock rate.

VOLTAGE REFERENCE

The SC9588 has a built-in 1.2V band gap reference and the internal reference voltage will be shown at REFIO by simply decoupling the REFIO pin to ACOM with a 0.1µF capacitor. Furthermore, if the voltage at REFIO is to be used by other circuitry, an external buffer amplifier is recommended because this reference can only drive a current less than 100nA. Such example is given in Figure 9.

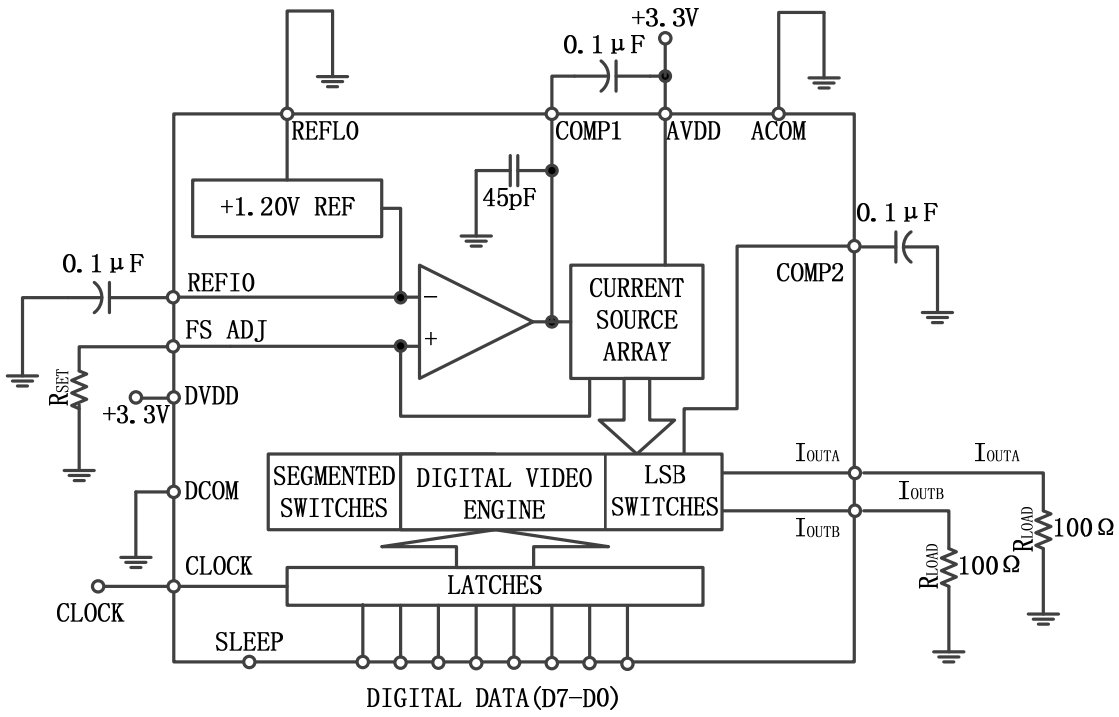


Figure 8. Functional Block Diagram

The SC9588's full-scale output current, say I_{OUTFS}, is directly proportional to I_{REF} that is adjustable by setting the ratio of the V_{REFIO} and an external resistor, R_{SET}. The span of I_{OUTFS} is from 1mA to 10mA.
By adjusting I_{OUTFS}, several benefits have been shown along with such wide adjustment span of I_{OUTFS}. The first relates directly to the power dissipation of the SC9588, which is proportional to I_{OUTFS} (refer to the Power Dissipation section). The second relates to the 20dB adjustment, which is useful for system gain control purposes.

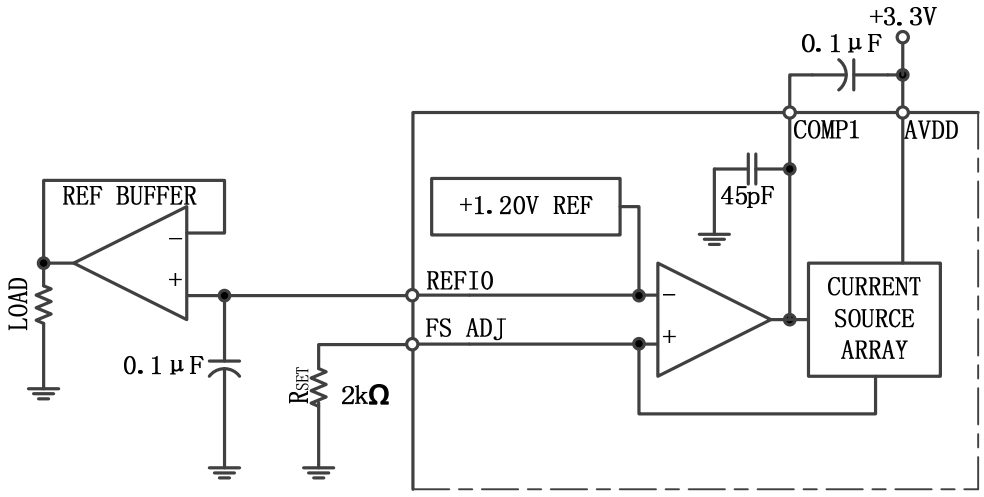


Figure 9. Reference Output Driver Configuration

DAC TRANSFER FUNCTION

The SC9588 provides complementary current outputs, I_{OUTA} and I_{OUTB}. The amplitude of I_{OUTA} is proportional to the input code while the amplitude of I_{OUTB} is reversely proportional to the input code. That is, when the input codes are all 1s, I_{OUTA} will provide a near full-scale current output, I_{OUTFS}. Meanwhile, I_{OUTB}, the complementary output, provides no current. The current output appearing at I_{OUTA} and I_{OUTB} is a function of both the input code and I_{OUTFS}, such relationship can be expressed as,

$$I_{OUTA} = (\text{DAC CODE}/256) \times I_{OUTFS} \quad \text{(Eq.1)}$$
$$I_{OUTB} = (255-\text{DAC CODE})/256 \times I_{OUTFS} \quad \text{(Eq.2)}$$

Where DAC CODE = 0 to 255 (i.e., decimal representation). As mentioned previously, I_{OUTFS} is directly proportional to I_{REF}, and I_{REF} is adjustable by setting the ratio of the V_{REFIO} and an external resistor, R_{SET}. I_{OUTFS} can be expressed as,

$$I_{OUTFS} = 16 \times IREF \quad \text{(Eq.3)}$$

Where

$$I_{REF} = V_{REFIO} / R_{SET} \quad \text{(Eq. 4)}$$

Typically, the two current outputs will drive a resistive load directly or via a transformer. If dc coupling is required, I_{OUTA} and I_{OUTB} should be directly connected to matching resistive loads, R_{LOAD}, that are tied to analog common, ACOM. The following equations express the simple single-ended voltage output which appears at the I_{OUTA} and I_{OUTB} nodes,

$$V_{OUTA} = I_{OUTA} \times R_{LOAD} \quad \text{(Eq.5)}$$
$$V_{OUTB} = I_{OUTB} \times R_{LOAD} \quad \text{(Eq.6)}$$

Note, to maintain specified distortion and linearity performance, the full-scale value of V_{OUTA} and V_{OUTB} cannot exceed the specified output compliance range.

$$V_{DIFF} = (I_{OUTA} - I_{OUTB}) \times R_{LOAD} \quad \text{(Eq.7)}$$

Substituting the values of I_{OUTA}, I_{OUTB}, I_{REF}, and V_{DIFF} can be expressed as,

$$V_{DIFF} = \{(2\times\text{DAC CODE} - 255)/256\} / (16\times R_{LOAD} / R_{SET}) \times V_{REFIO} \quad \text{(Eq.8)}$$

Eq. 8 is the transfer function of the SC9588 operating differentially. Not only doubling the value of the single-ended voltage output (i.e., V_{OUTA} or V_{OUTB}), the differential operation also help cancelling common-mode error sources associated with I_{OUTA} and I_{OUTB}, such as noise, distortion, and dc offsets. Note, performing a differential to single-ended conversion via a transformer also provides the ability to deliver twice the reconstructed signal power to the load.
Also from Eq.8, the gain drift temperature performance for a single-ended (V_{OUTA} and V_{OUTB}) or differential output (V_{DIFF}) of the SC9588 can be enhanced by selecting temperature tracking resistors for R_{LOAD} and R_{SET} (see the R_{LOAD} / R_{SET} part in Eq.8).

ANALOG OUTPUTS AND OUTPUT CONFIGURATIONS

The SC9588 can be configured in either single-ended or differential way. By differential configuration, SC9588 achieves enhanced distortion and noise performance especially as the frequency content of the reconstructed waveform increases and/or its amplitude decreases.

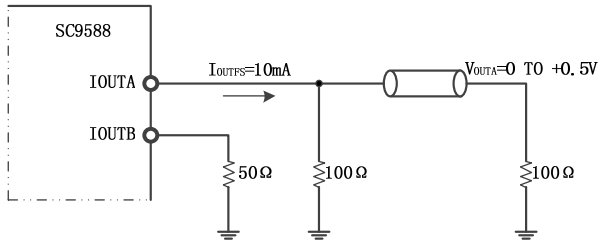


Figure 10. 0V to +0.5V Unbuffered Voltage Output

The output impedance of IOUTA and IOUTB of SC9588 is typically 100kΩ in parallel with 5pF and slightly dependent on the output voltage (i.e., VOUTA and VOUTB). As a result, to maintain optimum dc linearity, it should keep IOUTA and/or IOUTB at a virtual ground via an I-V op amp. Please be noted, the INL/DNL specifications of the SC9588 are measured with IOUTA maintained at a virtual ground via an op-amp.

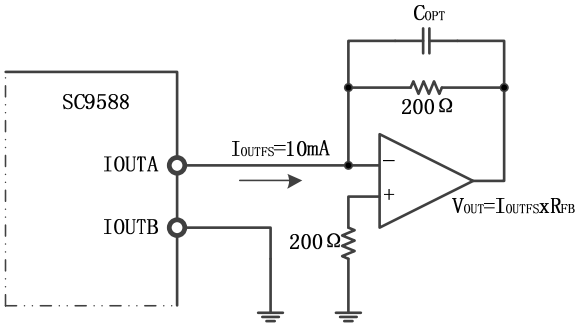


Figure 11. Unipolar Buffered Voltage Output

As mentioned previously, to achieve optimum performance the voltage at IOUTA and IOUTB must adhere the negative and positive voltage compliance range. The positive output compliance range is slightly dependent on the full-scale output current, IOUTFS. The negative output compliance range of –1.0 V is set by the breakdown limits of the CMOS process. Operating beyond this limit will affect the reliability of the SC9588.

DIGITAL INPUTS

The SC9588's digital section consists of 8 input pins and 1 clock pin. Standard positive binary coding applies to the SC9588's inputs, where the D7 is the most significant bit (MSB) and the D0 is the least significant bit (LSB). The digital interface is implemented using an edge-triggered latch. When the input codes are all 1s, I_{OUTA} will provide a near full-scale current output, I_{OUTFS}. Meanwhile, I_{OUTB}, the complementary output, provides no current. The current output appearing at I_{OUTA} and I_{OUTB} is a function of both the input code and I_{OUTFS}, as expressed in Eq.1 and Eq.2.

DAC TIMING

The SC9588 has been armed with SteadiChips' third generation digital video engine technology. This technology can eliminate more than 80% data latency which is quite sensitive at high-end video application. To meet the system timing requirement, SC9588 supports clock rate up to 50MSPS. Although its data update rate is half of the clock rate; please refer to figure 1 for the timing details.

The SC9588 supports clock with duty cycle in wide range, best performance is typically achieved when the input data transitions on the falling edge of a 50% duty cycle clock.

INPUT CLOCK AND DATA TIMING RELATIONSHIP

Since the SC9588 is rising-edge triggered, the relationship between the position of the clock edges and input data transition point affect the dynamic performance. In general, when the input data transition is close to the falling clock edge, optimum performance is achieved.

SLEEP MODE OPERATION

The SC9588 may be powered down by tying the SLEEP pin to AVDD. In this case, the supply current is reduced to less than 1mA typically. A built-in active pull-down circuit guarantees that the SC9588 remains enabled as this SLEEP pin is left disconnected. The SC9588 takes less than 50ns to power down and approximately 250us to power back up.

POWER DISSIPATION

Several factors affect the power dissipation, of the SC9588:

- The power supply voltages (AVDD and DVDD)
- The update rate f_{CLOCK}
- The full-scale current output I_{OUTFS}
- The reconstructed digital input waveform

The power dissipation is directly related the total supply current I_{TOTAL}, which consist of analog supply current, I_{AVDD}, and the digital supply current, I_{DVDD}. I_{AVDD} is directly proportional to I_{OUTFS} and is insensitive to f_{CLOCK}, while, I_{DVDD} is dependent on both the digital input waveform, f_{CLOCK}, and digital supply DVDD.

APPLYING THE SC9588

Output Configurations

Unless otherwise noted, the following sections are assumed that a differential output configuration is used and I_{OUTFS} is set to a nominal 10mA. For any application that allows ac coupling, the RF transformer is recommended to achieve the optimum high-frequency performance, while for applications requiring dc coupling, a differential op amp is recommended.

The SC9588 can be configured as single-ended manner by connecting I_{OUTA} and/or I_{OUTB} to an appropriately sized load resistor, R_{LOAD}, referred to ACOM, This configuration is suitable for a single-supply system requiring a dc-coupled, ground referred output voltage. Alternatively, an amplifier could be configured as an I-V converter, thus converting I_{OUTA} or I_{OUTB} into a negative unipolar voltage. This configuration provides the best dc linearity since I_{OUTA} or I_{OUTB} is maintained at a virtual ground.

Differential Coupling Using a Transformer

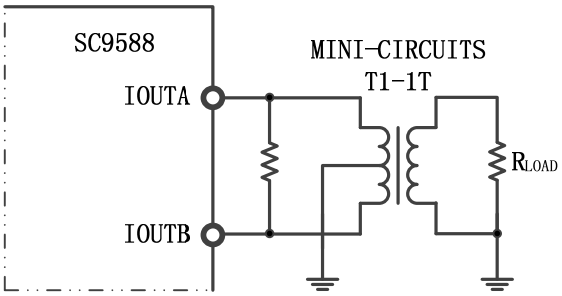


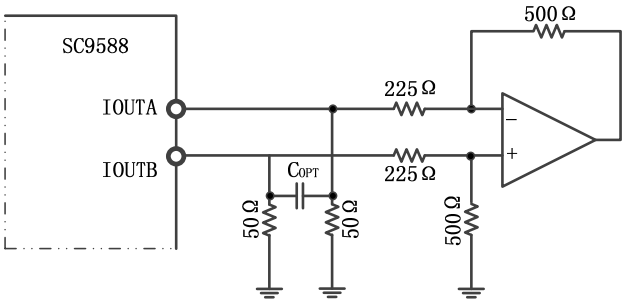
Figure 12. Differential Output Using a Transformer

An RF transformer can be used to perform a differential to single-ended signal conversion as shown in Figure 12. By using a good RF transformer, SC9588 may provide excellent rejection of common-mode distortion, also provides electrical isolation and the ability to deliver twice the power to the load. Furthermore, transformers with different impedance ratios may also be used for impedance matching purposes. Note that the transformer provides ac coupling only.

To provide the necessary dc current path for both I_{OUTA} and I_{OUTB}, the center tap on the primary side of the transformer must be connected to ACOM. A differential resistor, R_{DIFF}, may be inserted in applications where the output of the transformer is connected to the load, R_{LOAD}, via a passive recon-structure filter or cable.

Differential Coupling Using an Op Amp

Figure 13. DC Differential Coupling Using an Op Amp



An op amp can also be used to perform a differential to single-ended conversion as shown in Figure 13. Note that the capacitor C_{OPT} forms a real pole in a low-pass filter. Also this capacitor enhances the op amp's distortion performance by preventing the DACs high slewing output from overloading the op amp's input.

Resistor matching is critical in this configuration due to the common-mode rejection reason. In this circuit, the differential op amp circuit configured to provide some additional signal gain and the necessary level shifting required in a single-supply system. The op amp's differential gain, its gain setting resistor values, and full-scale output swing capabilities should all be considered when optimizing this circuit.

Single-Ended, Buffered Voltage Output Configuration

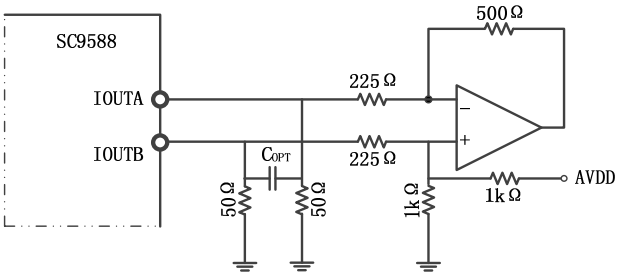


Figure 14. Single-supply DC Differential Coupled Circuit

Figure 14 shows a buffered single-ended output configuration. In this configuration, an op amp performs an I-V conversion on the SC9588 output current. As discussed in the Analog Output section, the op amp maintains I_{OUTA} (or I_{OUTB}) at a virtual ground to achieve the best DAC's INL performance. Although this single-ended configuration typically provides the best dc linearity performance, its ac distortion performance is limited. An improvement in ac distortion performance may result with a reduced I_{OUTFS} since the signal current op amp will be required to sink less signal current.

POWER AND GROUNDING CONSIDERATIONS

Power Supply Rejection

The PSRR is defined as the ratio of the change in supply voltage to the corresponding change in output voltage. Generally, to minimize PSRR is a crucial requirement in both printed circuit board design and circuit design. Proper grounding and decoupling may greatly reduce the PSRR of a circuit and therefore should be a primary objective in any high-speed, high resolution system. The SC9588 features separate analog and digital supply and ground pins. This provides a flexible manner to optimize the grounding and decoupling in a system. In general AVDD should be decoupled to ACOM as close to the chip as physically possible. Similarly, DVDD, the digital supply, should be decoupled to DCOM as close to the chip as physically possible. For those applications that require a single 3.3V supply for both the analog and digital supplies, a clean analog supply may be generated. The circuit consists of a differential LC filter with separate power supply and return lines. Lower noise can be attained by using low ESR type electrolytic and tantalum capacitors.

SteadiChips' Digital Video Engine

The Digital Video Engine (DVE) that is built in the SC9588 is part of the SteadiChips' Video Enhancement Algorithm (the rest part is carried by SC9087), which is optimized for optical video transmission system. Combining the SC9087 and the SC9588, the algorithm is complete and can fully function. By calibrating the inevitable distortion coming from transmission, the Video Enhancement Algorithm (VEA) may achieve an excellent video performance, especially for amplitude-frequency characteristic and chroma-luminance-gain-inequity. The SC9588 can also be used alone or in pair with ADC without DVE, such as SC9082 (ADC without DVE inside). SteadiChips recommend the customers use SC9588, SC9087 and SC6362 together for optimal performance. The SC9588 is compatible with SC9518 in pin configuration except that the SC9588 needs the clock rate two times as high as the SC9518 does.

APPLICATION INFORMATION

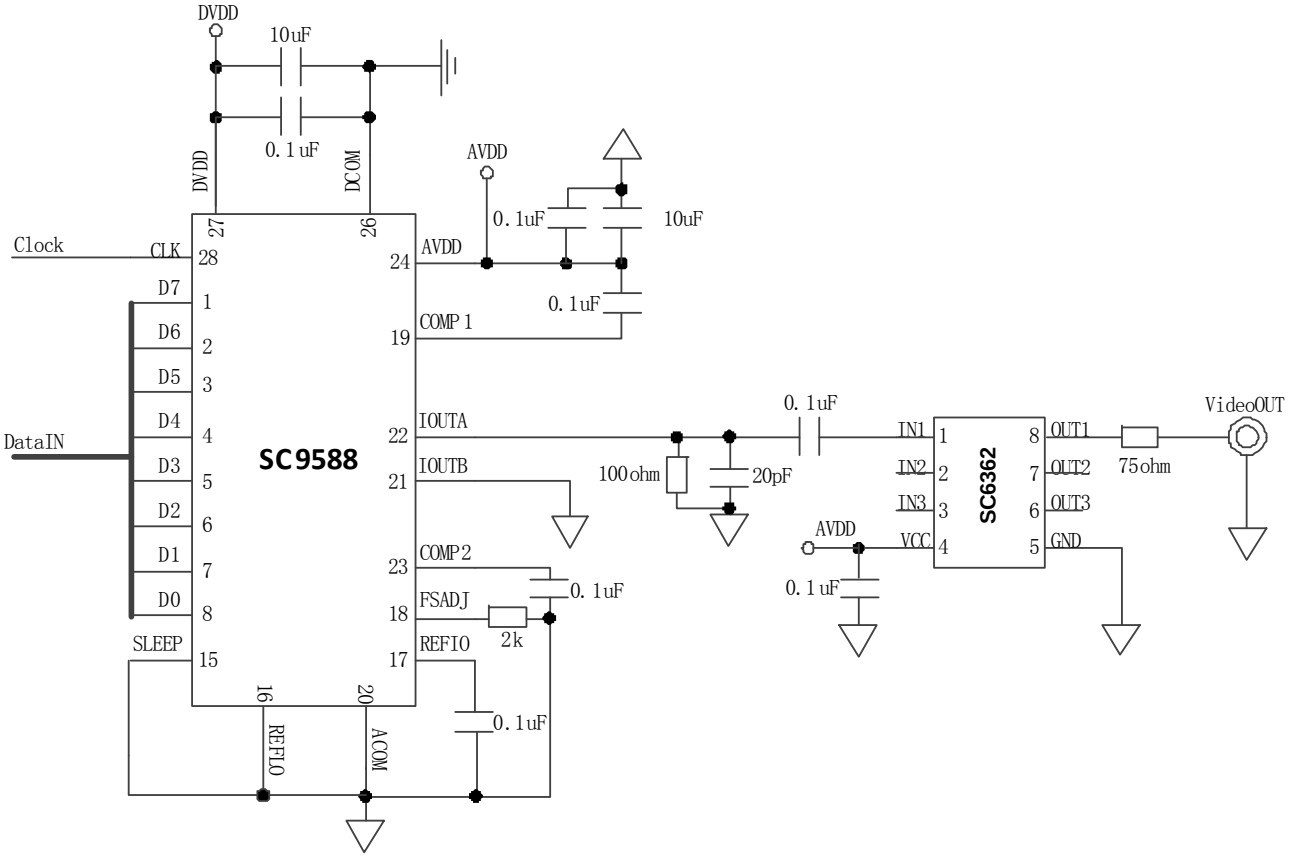
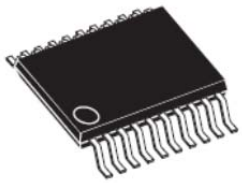


Figure 15. Application Schematic

MECHINAL DATA

20-LEAD SHRINK SMALL OUTLINE PACKAGE (SSOP20)

DIMENSIONS			
REF.	mm		
	MIN.	TYP.	MAX.
A	-	-	1.730
A1	0.050	-	0.230
A2	1.400	-	1.600
b	0.220	-	0.380
c	0.090	-	0.250
D	7.000	-	7.400
E	7.600	-	8.000
E1	5.100	-	5.500
e	0.65BSC		
θ	0°	-	8°
L	0.550	-	0.950



SSOP20

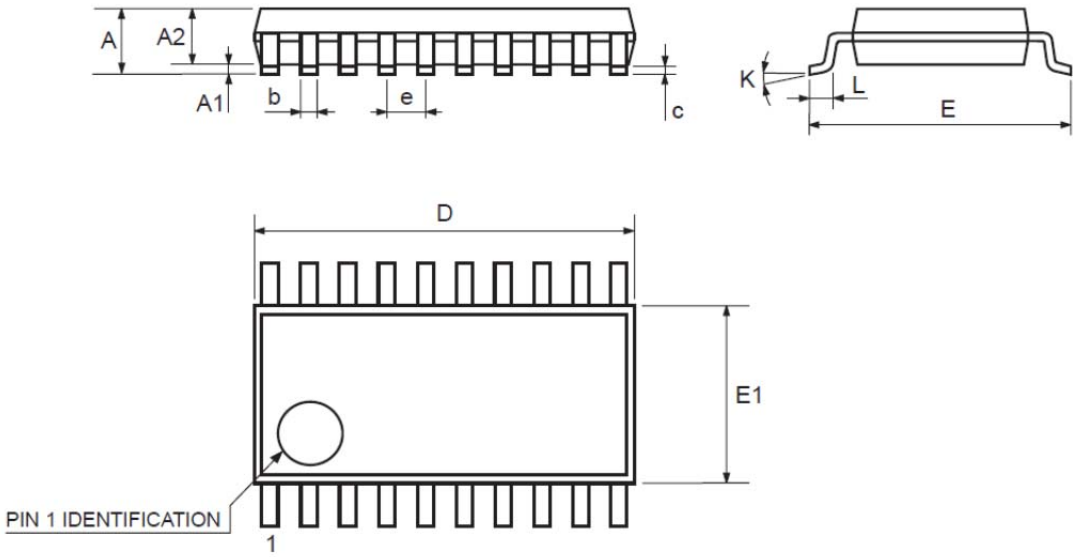


Figure 16. SSOP20 Outline