## Feature

- 140ns propagation delay (@100mV Overdrive)
- Rail to Rail output, CMOS/TTL Compatible
- Internal Hysteresis to ensure clean switching
- DC coupled Input
- Offset voltage: +/-5mV Max.
- Low HYS voltage Temperature Drift: 5uV/℃.
- 2.7~5.5V power supply Voltage.
- Low quiescent current: 200uA
- Chip available in SOT23-5 Package

## Applications

- High speed Line Receivers;
- Threshold Detector /Discriminators;
- Sampling Circuits;
- IR Receivers.

## General Description

8051 is a high speed, low power dissipation comparator. It applies 140ns Propagation Delay at 100mV Overdrive voltage.

8051 is DC coupled normally, and It includes internal hysteresis(5mV) to ensure clean output switch, the HYS voltage has a ultra-low temperature drift 5uV/℃.

8051 consists of a high speed Class AB structure, which supports rail to rail output.

## Package

The package of 8051 is SOT23-5

## Block Diagram

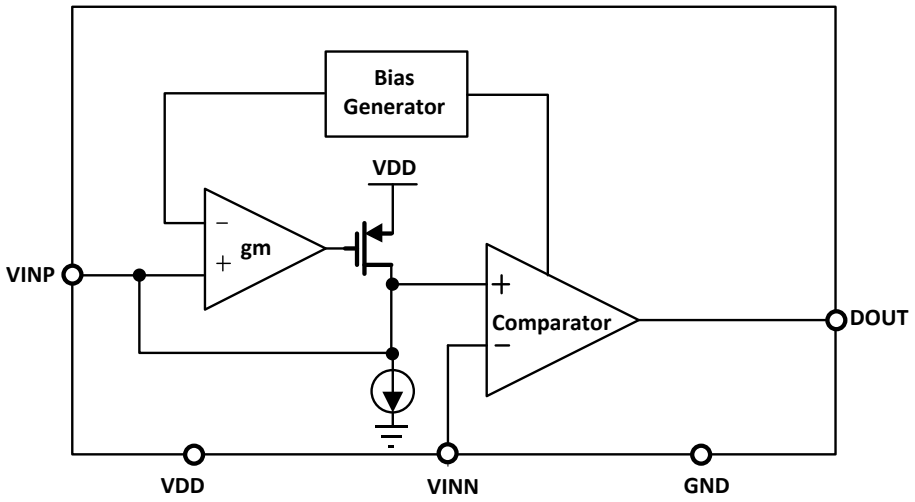



Fig.1 block diagram of 8051

REV. 1.0

## Absolute Maximum Ratings

(If out of these ratings, the filter may be fail or damaged)

Table 1

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| VDD | Power supply | 5.5 | V |
| $T_A$ | Operating ambient Temperature Range | -40~+85 | ℃ |
| $T_{STG}$ | Storage Temperature | -65~+150 | ℃ |

## Recommended Operating Conditions

Table 2

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| VDD | Power supply | 2.7~5.5 | V |
| $T_A$ | Operating ambient Temperature Range | -40~+85 | ℃ |

## Electrical Characteristics

Table 3

Specifications are at VDD=+2.7V ~ +5.5V Vin+=VDD, Vin-=1.2V RL=10Kohm CL=15pF Vin-=1.2V tt corner & T=30 ºC)

| Symbol | Parameter | | Spec | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| VCC | Operating Supply Voltage | | 2.7 | 3.3 | 5.5 | V |
| VOS | Input Offset Voltage | | -5 | +/-0.15 | +5 | mV |
| VOS_TC | Input Offset voltage Temp Drift | | 0.64 | 1.96 | 4.7 | uV/℃ |
| Vhyst | Input Hysteresis Voltage | | 4 | 5 | 10.8 | mV |
| Vhyst_TC | Input Hysteresis Voltage Temp Drift | | | 4.8 | 5.4 | uV/℃ |
| CIN | Input Capacitance | Differential | | 1.8 | | pF |
| | | Common Mode | | 3.6 | | |
| RIN | Input Resistance | | | >100 | | GΩ |
| IQ | Quiescent Current | | | 200 | | uA |
| ISC | Output short to VDD | | | 25 | | mA |
| Vin_cm | Common mode Input voltage | | GND+0.2 | - | VDD-0.2 | V |
| VOH | Output Voltage High Swing | | VDD-0.3 | | | V |
| VOL | Output Voltage Low Swing | | | | GND+0.3 | mV |
| CMRR | Common Mode Rejection Ratio | | | 70 | | dB |
| PSRR | Power supply rejection ratio | | | 63 | | dB |
| tR | Rising time | | | 35 | | ns |
| tF | Falling time | | | 28 | | ns |
| TPD+ | Propagation Delay(Low to High) | | | 140 | | ns |
| TPD- | Propagation Delay(High to Low) | | | 135 | | ns |

*Note1: The input offset voltage is the average of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.

## PAD Definition

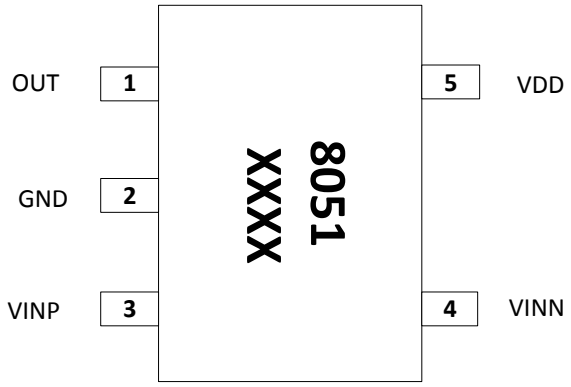



Fig.2 Pad definition of 8051

Table 4 Pad definition

| Pad | Name | I/O | Analog/Digital | Description |
|---|---|---|---|---|
| 1 | OUT | O | A | Comparator Output PAD, High Voltage level is Pulled to VDD, Low Voltage is GND. |
| 2 | GND | GROUND | GROUND | Ground pin. Connect to the most negative supply, ALL GND pads are connected on die. |
| 3 | VINP | I | A | Video signal input PAD, DC coupled. |
| 4 | VINN | I | A | DC Reference voltage input PAD. |
| 5 | VDD | POWER | POWER | Power supply (3.3V/5V), connect to positive voltage supply. |

## Application Circuits

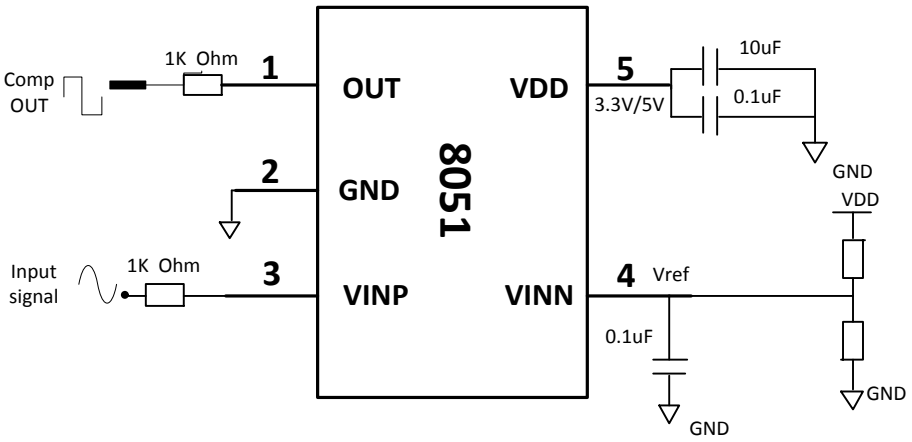
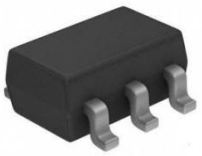



Fig.3 Applications Circuits of 8051

## Package

**SOT23-5**

| Symbol | Unit(mm) | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | - | - | 1.35 |
| A1 | 0.04 | - | 0.15 |
| A2 | 1.00 | 1.10 | 1.20 |
| b | 0.38 | - | 0.48 |
| b1 | 0.37 | 0.40 | 0.43 |
| c | 0.11 | - | 0.21 |
| c1 | 0.10 | 0.13 | 0.16 |
| D | 2.72 | 2.92 | 3.12 |
| E | 2.60 | 2.80 | 3.00 |
| E1 | 1.40 | 1.60 | 1.80 |
| e | 0.95BSC | | |
| θ | 0° | - | 8° |
| L | 0.30 | - | 0.60 |



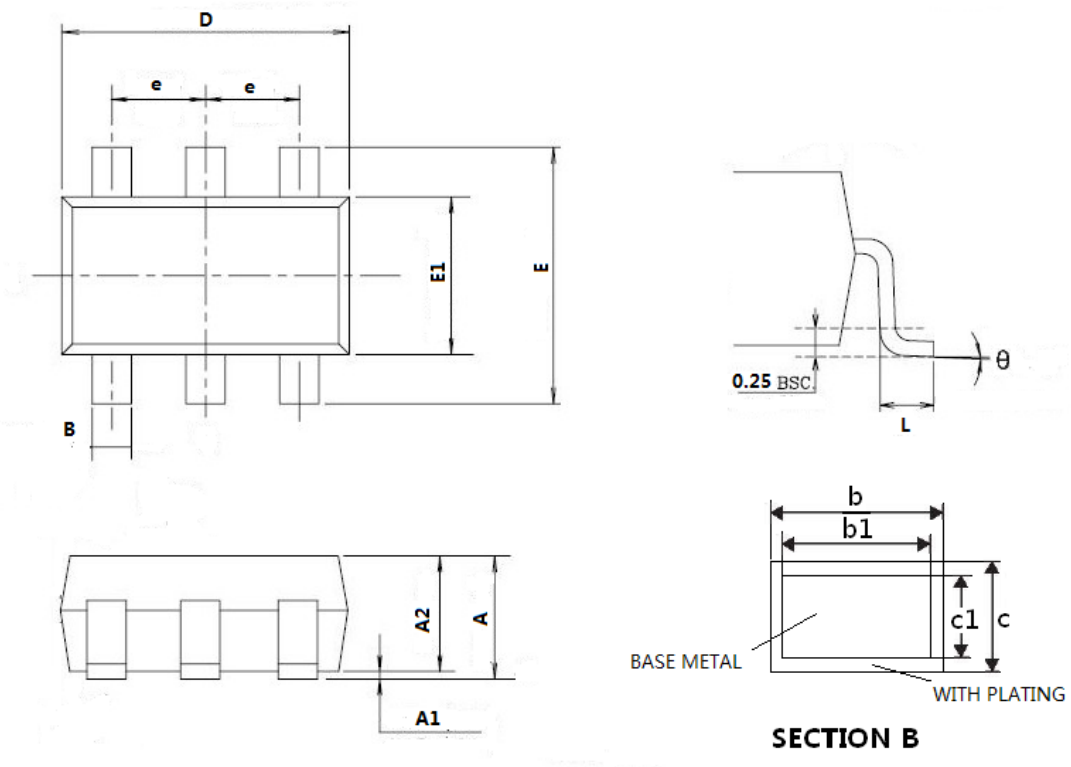



Fig.4 Package of 8051