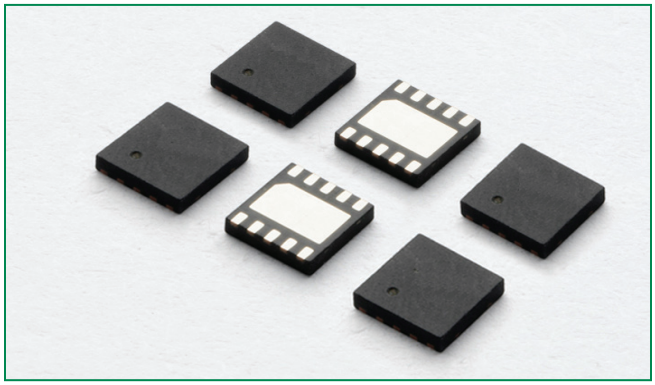
SP4042 Series 3.3V Diode Array

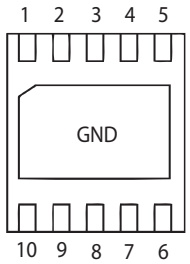
RoHS Pb GREEN



Description

The SP4042 integrates low capacitance steering diodes with a TVS diode to provide 2 channels of protection against lightning induced surge events and ESD. This robust device can safely absorb up to 120A per IEC61000-4-5 (t_P= 2/10µs) without performance degradation and a minimum ±30kV ESD per IEC61000-4-2 international standard. The low loading capacitance makes the SP4042 ideal for protecting Ethernet interfaces.

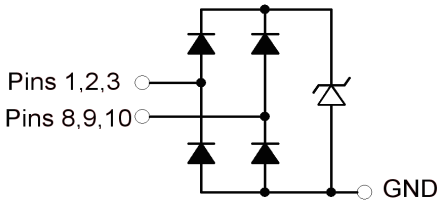
Pinout



Features

- ESD, IEC61000-4-2, ±30kV contact, ±30kV air
- Lightning, IEC61000-4-5 2nd edition, 120A (t_P=2/10µs)
- EFT, IEC61000-4-4, 40A (t_P=5/50ns)
- Low capacitance of 11pF (TYP) per line
- Low leakage current of 0.1µA (MAX) at 3.3V
- Lead-free and RoHS compliant

Functional Block Diagram



Applications

- 10/100/1000 Ethernet Interfaces
- Customer Premise Equipment (CPE)
- Carrier Class Equipment
- PBX Systems

Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Revision: 01/29/16

TVS Diode Arrays (SPA® Diodes)

Lightning Surge Protection- SP4042 Series

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{PP}	Peak Current (t_p=8/20µs)	95	A
I_{PP}	Peak Current (t_p=2/10µs)	120	A
P_{PK}	Peak Pulse Power (t_p=2/10µs)	2500	W
T_{OP}	Operating Temperature	-40 to 85	ºC
T_{STOR}	Storage Temperature	-55 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

Parameter	Rating	Units
Storage Temperature Range	-55 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s)	260	°C

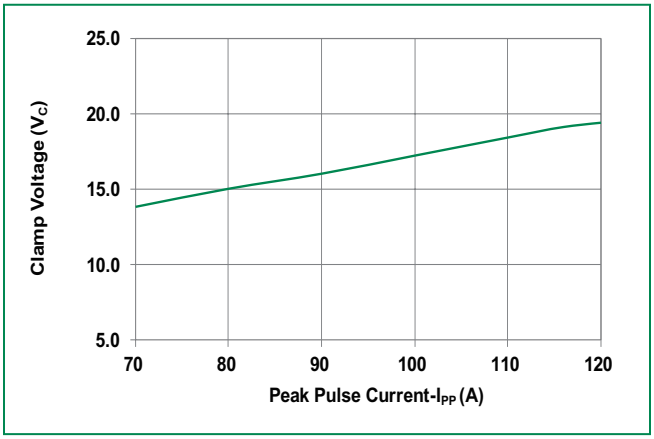
Electrical Characteristics (T_{OP}=25°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	V_{RWM}	I_R≤1µA, Line to Line			3.3	V
Reverse Breakdown Voltage	V_{BR}	I_T=1mA, Line to Line	3.5			V
Snap Back Voltage	V_{SB}	I_{SB}=50mA	2.8			V
Reverse Leakage Current	I_{LEAK}	V_R=3.3V, Line to Line			0.1	µA
Clamp Voltage, Line to GND[1]	V_C	I_{PP}=100A, t_p=2/10µs		17	22	V
Clamp Voltage, Line to Line[1]		I_{PP}=100A, t_p=2/10µs		22	25	V
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact)	±30			kV
		IEC61000-4-2 (Air)	±30			kV
Dynamic Resistance, Line to GND[2]	R_{DYN}	TLP, t_p=100ns		0.05		Ω
Dynamic Resistance, Line to Line[2]				0.15		Ω
Diode Capacitance[1]	$C_{I/O-GND}$	Line to GND, V_R=0V, f=1MHz		11	25	pF
	$C_{I/O-I/O}$	Line to Line, V_R=0V, f=1MHz		5.5	12	pF

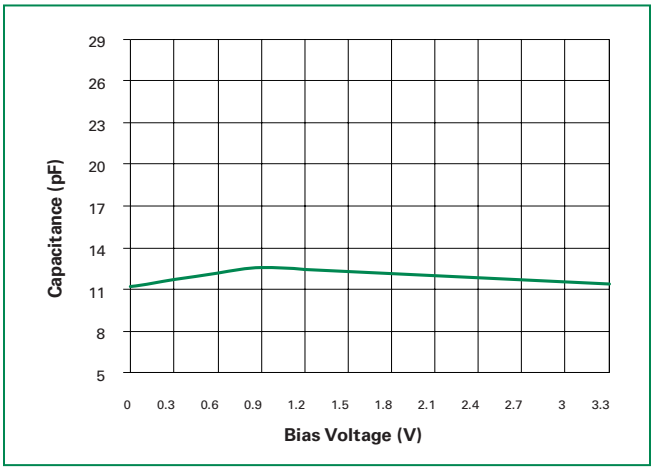
Note: 1 Parameter is guaranteed by design and/or device characterization.

2 Transmission Line Pulse (TLP) test setting : Std.TDR(50Ω),tp=100ns, tr=0.2ns ITLP and VTLP averaging window: star t1=70ns to end t2=80ns

Wave Form 2/10µs Clamping Voltage vs. Peak Pulse Crrent (Line to GND)



Capacitance vs. Reverse Bias(Line to GND)

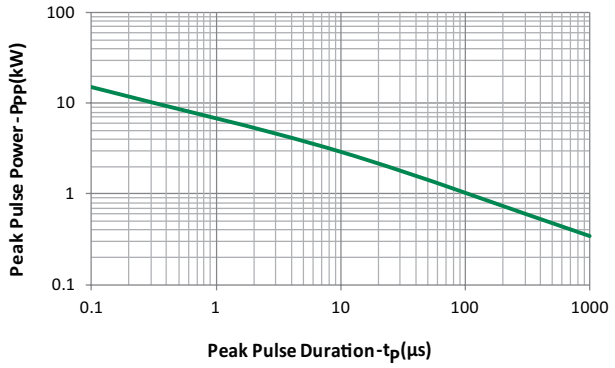


Revision: 01/29/16

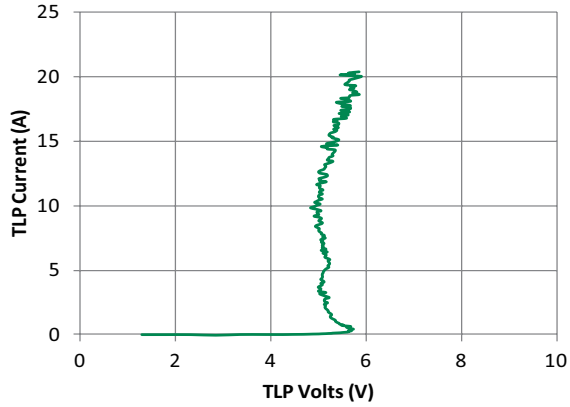
TVS Diode Arrays (SPA® Diodes)

Lightning Surge Protection- SP4042 Series

Non-Repetitive Peak Pulse Power vs. Pulse Time

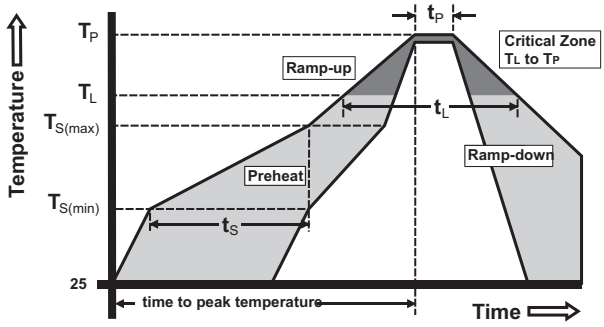


Positive Transmission Line Pulsing (TLP) Plot (Line to GND)



Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	- Temperature Min ($T_{s(min)}$)	150°C
	- Temperature Max ($T_{s(max)}$)	200°C
	- Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	- Temperature (T_L) (Liquidus)	217°C
	- Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Product Characteristics

Lead Plating	Pre-Plated Frame
Lead Material	Copper Alloy
Lead Coplanarity	0.004 inches(0.102mm)
Substrate material	Silicon
Body Material	Molded Epoxy
Flammability	UL 94 V-0

Notes :

1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4.. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
5. Package surface matte finish VDI 11-13.

Part Numbering System

SP 4042-02 U T G

- SP: TVS Diode Arrays (SPA® Diodes)
- 4042: Series
- 02: Number of Channels -02= 2 channel
- U: Package U= µDFN-10
- T: T= Tape & Reel
- G: G= Green

Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP4042-02UTG	µDFN-10	A2*2	3000

Part Marking System

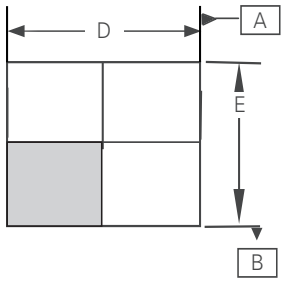
A2 * 2

- A2: Product Series A2 = SP4042
- *: Assembly Site
- 2: Number of Channels

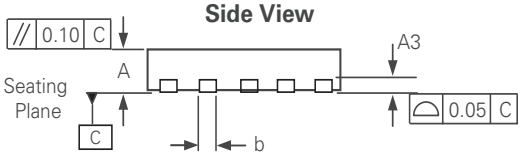
Revision: 01/29/16

Package Dimensions — µDFN-10

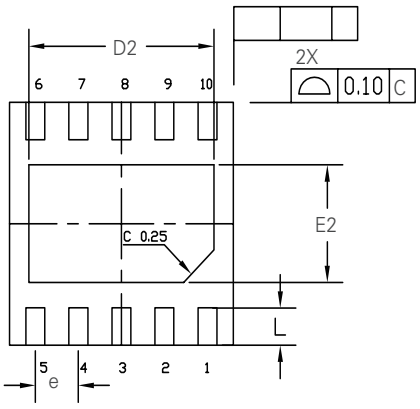
Top View



Side View

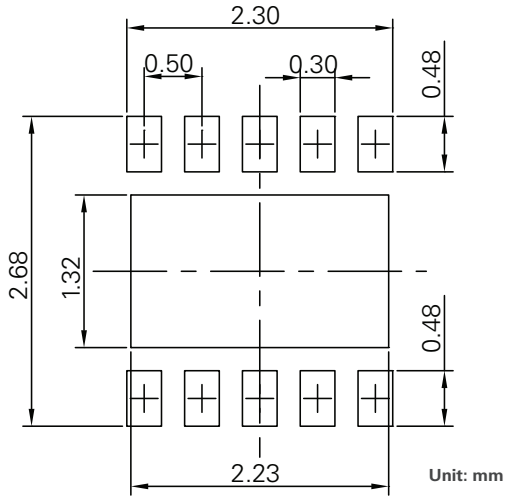


Bottom View

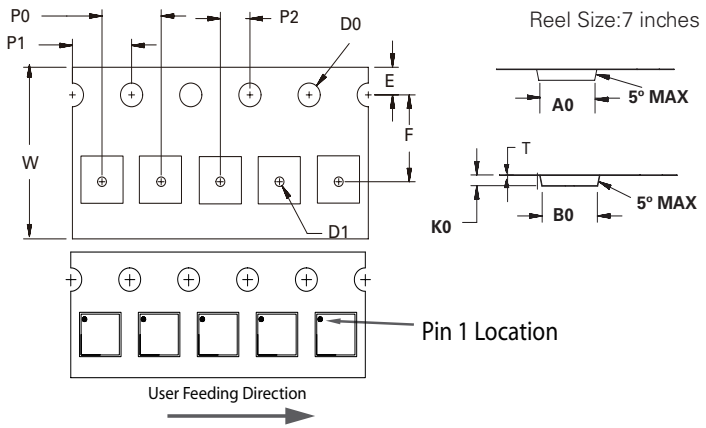


Package	µDFN-10 (2.6x2.6mm)					
JEDEC	MO-229					
Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.45	0.52	0.55	0.018	0.020	0.022
A3		0.127Ref			0.005 Ref	
b	0.17	0.22	0.27	0.006	0.009	0.011
D	2.50	2.60	2.70	0.098	0.102	0.106
D2	2.10	2.15	2.20	0.083	0.085	0.087
E	2.50	2.60	2.70	0.098	0.102	0.106
E2	1.21	1.26	1.31	0.048	0.050	0.052
e		0.50 BSC			0.020 BSC	
L	0.35	0.40	0.45	0.014	0.016	0.018

RECOMMENDED SOLDER PAD



Embossed Carrier Tape & Reel Specification — µDFN-10 (2.6x2.6mm)



Symbol	Millimeters
A0	2.82 +/- 0.05
B0	2.82 +/- 0.05
D0	Ø1.50 + 0.10
D1	Ø 0.50 + 0.05
E	1.75 +/- 0.10
F	3.50 +/- 0.05
K0	0.76 +/- 0.05
P0	4.00 +/- 0.10
P1	4.00 +/- 0.10
P2	2.00 +/- 0.05
T	0.25 +/- 0.02
W	8.00 + 0.30 /- 0.10

Revision: 01/29/16