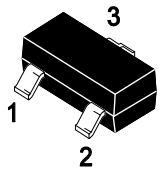
Dual transil array for ESD protection

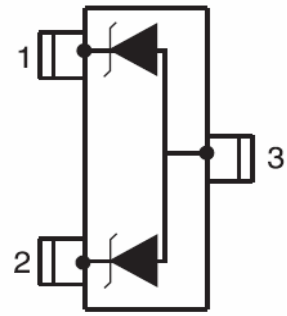
LESDA6V1LLT1G

General Description

The LESDA6V1LLT1G is a dual monolithic voltage suppressor designed to protect components which are connected to data and transmission lines against ESD. It clamps the voltage just above the logic level supply for positive transients, and to a diode drop below ground for negative transients. It can also work as bidirectionnal suppressor by connecting only pin1 and 2.



SOT23(TO-236)



Applications

- Computers
- Printers
- Communication systems

It is particulary recommended for the RS232 I/O port protection where the line interface withstands only with 2kV ESD surges.

Features

- 2 Unidirectional Transil functions
- Low leakage current: I_R max< 20 μA at VBR
- 3 00W peak pulse power(8/20 μ s)
- High ESD protection level: up to 25 kV
- We declare that the material of product compliance with RoHS requirements and Halogen Free.

Benefits

- High ESD protection level
- up to 25 kV. High integration.
- Suitable for high density boards.

Ordering Information

Device	Marking	Shipping
LESDA6V1LLT1G	E61	3000/Tape&Reel
LESDA6V1LLT3G	E61	10000/Tape&Reel

Complies with the following standards

IEC61000-4-2 Level 4

MIL STD 883c - Method 3015-6 Class 3

(Human Body Model)

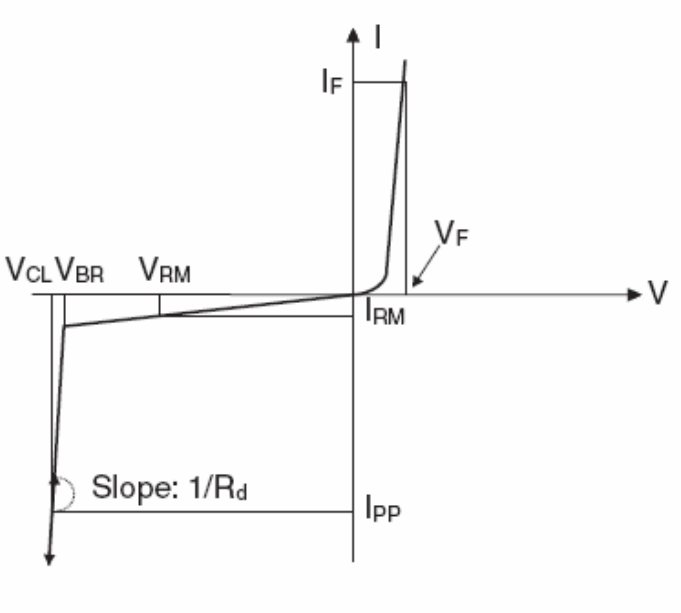
Absolute Ratings (T_{amb}=25°C)

Symbol	Parameter	Value	Units
P_{PP}	Peak Pulse Power (t_p = 8/20μs)	300	W
T_L	Maximum lead temperature for soldering during 10s	260	°C
T_{stg}	Storage Temperature Range	-55 to +150	°C
T_{op}	Operating Temperature Range	-40 to +125	°C
T_j	Maximum junction temperature	150	°C
V_{PP}	Electrostatic discharge MIL STD 883C -Method 3015-6 IEC61000-4-2 air discharge IEC61000-4-2 contact discharge	 25 16 9	kv

LESDA6V1LLT1G

Electrical Parameter

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{CL}	Clamping voltage
I_{RM}	Leakage current
I_{PP}	Peak pulse current
αT	Voltage temperature coefficient
V_F	Forward voltage drop
C	Capacitance
R_d	Dynamic resistance



Electrical Characteristics

Part Numbers	V_{BR}		I_R	V_{RM}	I_{RM}	V_F	I_F	V_C @ I_{PP} = 5A (V)	V_C @ I_{PP}=18A (V)	I_{PP}	R_d	α T	C
	Min.	Max.				Max.				Max.	Typ.(1)	Max.(2)	Typ. 0v bias
	v	v	mA	v	μA	v	mA	Max.	Max.	A	mΩ	10^{-4}/°C	pF
LESDA6V1LLT1G	6.1	7.2	1	5.25	20	1.25	200	11.5	16	18	350	6	140

1. Square pulse I_{PP}=15A,t_p=2.5μs 2. $\triangle V_{BR}=aT^*(T_{amb}-25°C)*V_{BR}(25°C)$

Typical Characteristics

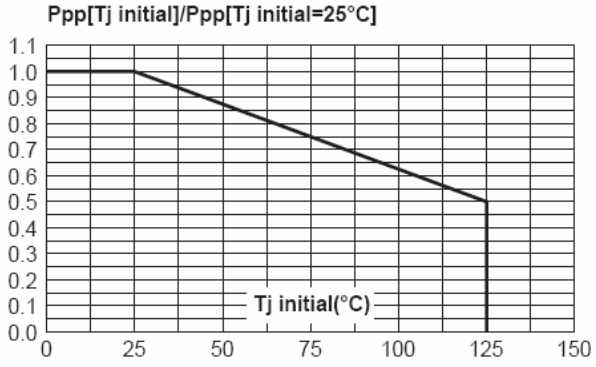


Fig1.Peak power dissipation versus Initial junction temperature

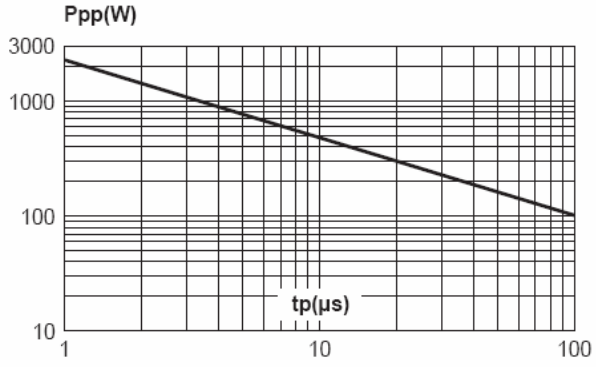


Fig2. Peak pulse power versus exponential pulse duration(T_j initial=25°C)

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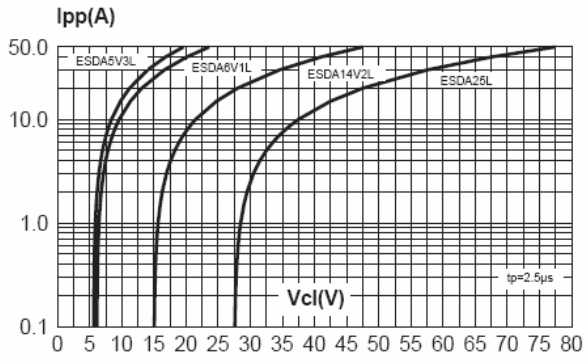

Fig3. Clamping voltage versus peak pulse current(T_j initial=25°C, rectangular Waveform,t_p=2.5 μ s)

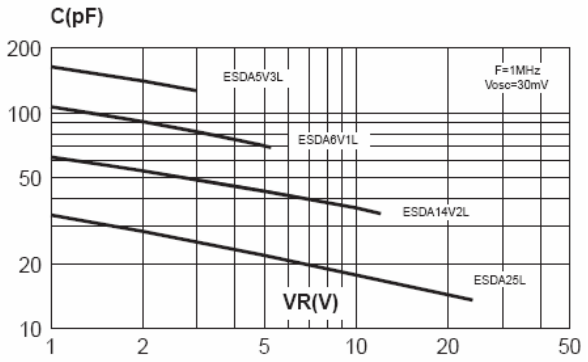

Fig4. Capacitance versus reverse Applied voltage

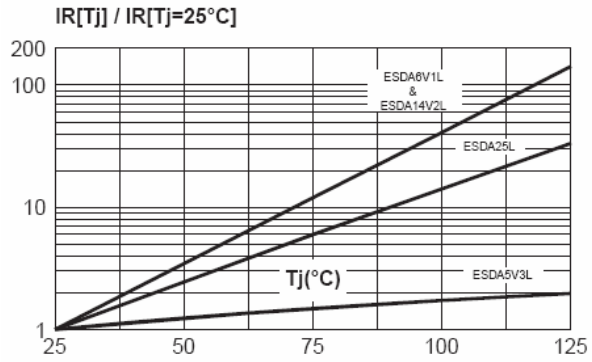

Fig5.Relative variation of leakage current Versus junction temperature

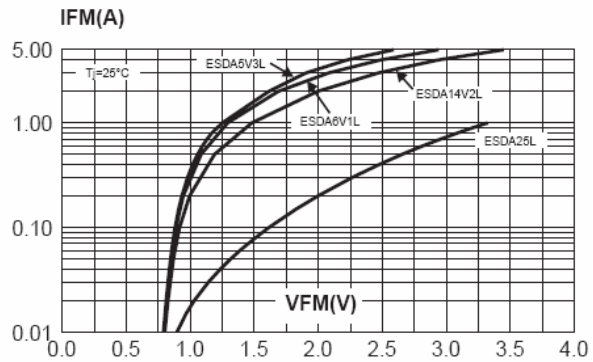

Fig6. Peak forward voltage drop versus peak forward current

Application Note

Electrostatic discharge (ESD) is a major cause of failure in electronic systems. Transient Voltage Suppressors (TVS) are an ideal choice for ESD protection. They are capable of clamping the incoming transient to a low enough level such that damage to the protected semiconductor is prevented.

Surface mount TVS arrays offer the best choice for minimal lead inductance. They serve as parallel protection elements, connected between the signal line to ground. As the transient rises above the operating voltage of the device, the TVS array becomes a low impedance path diverting the transient current to ground. The ESDAxxL array is the ideal board evel protection of ESD sensitive semiconductor components.

The tiny SOT23 package allows design flexibility in the design of high density boards where the space saving is at a premium. This enables to shorten the routing and contributes to hardening againt ESD.

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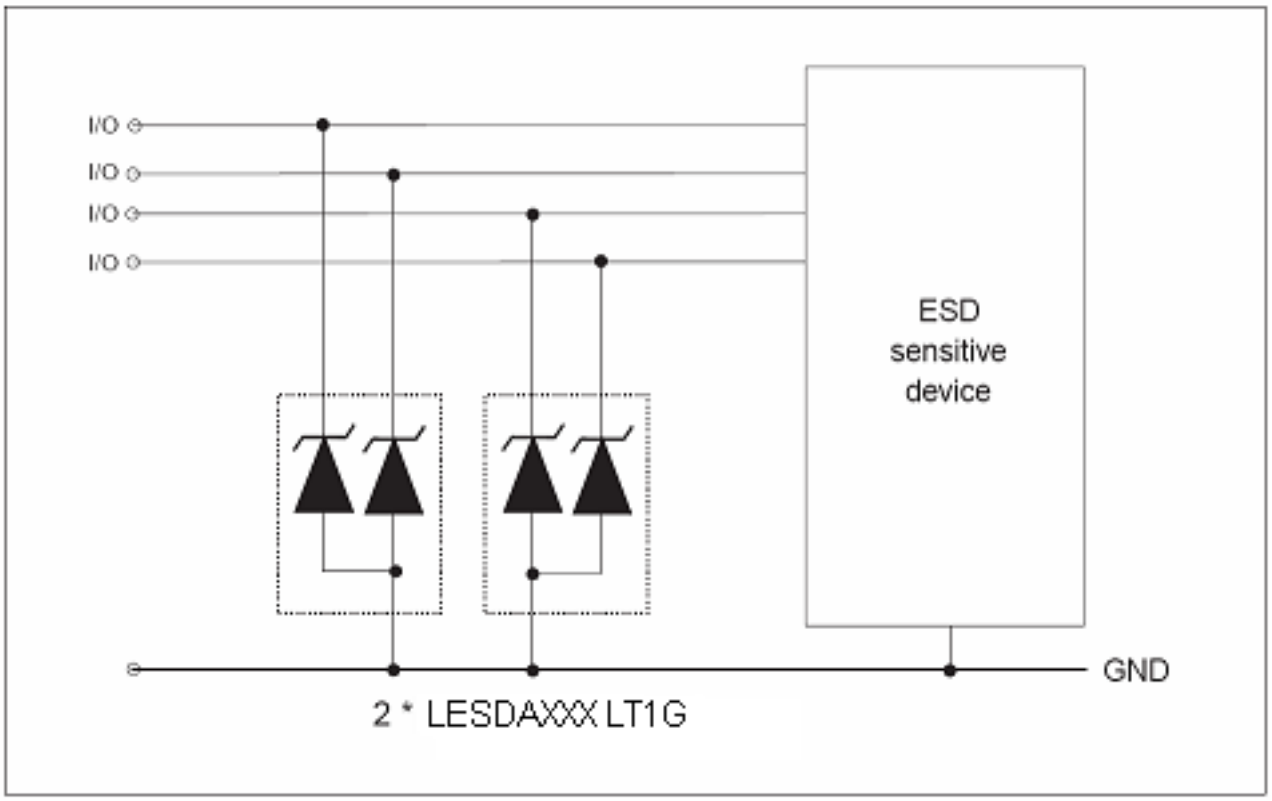

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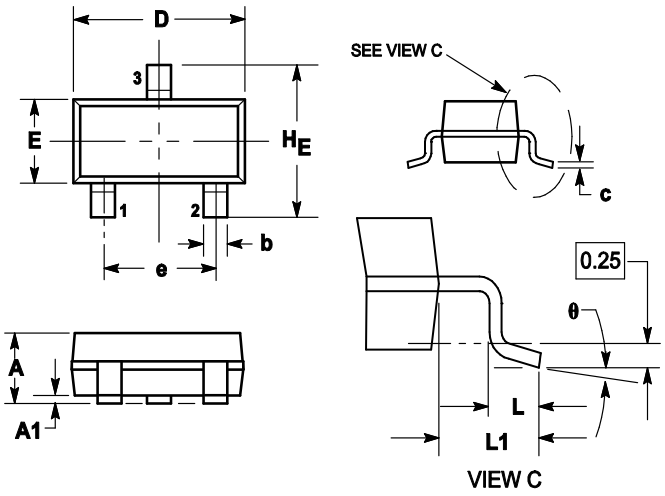
OUTLINE AND DIMENSIONS

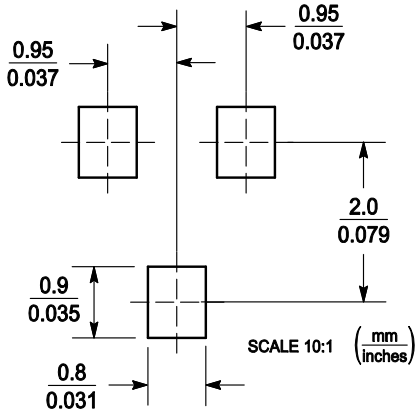


Notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1	1.11	0.035	0.04	0.044
A1	0.01	0.06	0.1	0.001	0.002	0.004
b	0.37	0.44	0.5	0.015	0.018	0.02
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.9	3.04	0.11	0.114	0.12
E	1.20	1.3	1.4	0.047	0.051	0.055
e	1.78	1.9	2.04	0.07	0.075	0.081
L	0.10	0.2	0.3	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.4	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

SOLDERING FOOTPRINT



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