



# GL8P04

## GL Silicon P-Channel Power MOSFET

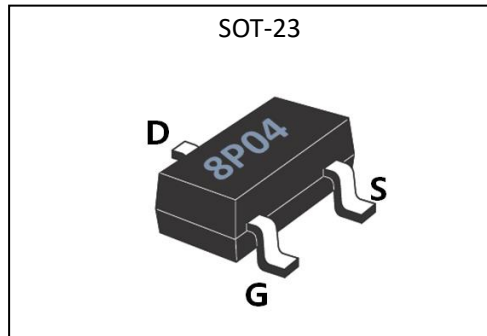
### General Description:

The GL8P04 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications. The package form is SOT-23-3L, which accords with the RoHS standard.

$V_{DSS}$	-40	V
$I_D$	-58	A
$P_D$	2.0	W
$R_{DS(ON)type}$	23	m $\Omega$

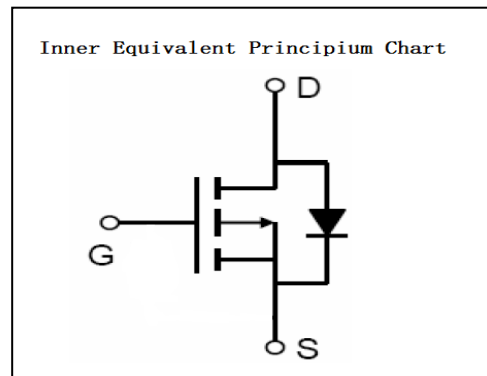
### Features:

- $R_{DS(ON)} < 33m\Omega$  @  $V_{GS} = 10V$  (Typ 23m $\Omega$ )
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation



### Applications:

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



### Absolute (Tc= 25°C unless otherwise specified):

Symbol	Parameter	Rating	Units
$V_{DSS}$	Drain-to-Source Voltage	-40	V
$I_D$	Continuous Drain Current	-8	A
$I_{DM}$	Pulsed Drain Current	-5.6	A
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$P_D$	Power Dissipation	2.0	W
$T_J, T_{stg}$	Operating Junction and Storage Temperature Range	150, -55 to 150	$^{\circ}C$



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**Electrical Characteristics** ( $T_c = 25^\circ\text{C}$  unless otherwise specified) :

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$V_{DSS}$	Drain to Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	-40	--	--	V
$I_{DSS}$	Drain to Source Leakage Current	$V_{DS}=-40V, V_{GS}=0V, T_a=25^\circ\text{C}$	--	--	-1.0	$\mu A$
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+20V$	--	--	0.1	$\mu A$
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-20V$	--	--	-0.1	$\mu A$

ON Characteristics <sup>a3</sup>						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	$V_{GS}=-10V, I_D=-5A$	--	23	33	$m\Omega$
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	-1.0	--	-3.0	V

Pulse width  $t_p \leq 380\mu s, \delta \leq 2\%$

Dynamic Characteristics <sup>a4</sup>						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$g_{fs}$	Forward Transconductance	$V_{DS}=-15V, I_D=-5A$	20	--	--	S
$C_{iss}$	Input Capacitance	$V_{GS}=0V, V_{DS}=-20V$ $f=1.0\text{MHz}$	--	750	--	pF
$C_{oss}$	Output Capacitance		--	100	--	
$C_{rss}$	Reverse Transfer Capacitance		--	75	--	

Resistive Switching Characteristics <sup>a4</sup>						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$V_{DD}=-20V, R_L=2\Omega$ $V_{GS}=-10V, R_G=3\Omega$	--	10	--	ns
$t_r$	Rise Time		--	9	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	28	--	
$t_f$	Fall Time		--	11	--	
$Q_g$	Total Gate Charge	$V_{DD}=-20V, I_D=-8A$ $V_{GS}=-10V$	--	15	--	nC
$Q_{gs}$	Gate to Source Charge		--	4.2	--	
$Q_{gd}$	Gate to Drain ( "Miller" )Charge		--	4.0	--	



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### Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$I_S$	Continuous Source Current <sup>a2</sup> (Body Diode)		--	--	-8	A
$V_{SD}$	Diode Forward Voltage <sup>a3</sup>	$I_S = -8A, V_{GS} = 0V$	--	--	-1.2	V

Symbol	Parameter	Typ.	Units
$R_{\theta JC}$	Junction-to-Case <sup>a2</sup>	83.3	°C/W

<sup>a1</sup>: Repetitive Rating: Pulse width limited by maximum junction temperature.

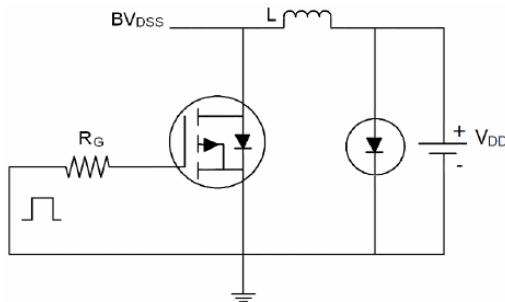
<sup>a2</sup>: Surface Mounted on FR4 Board,  $t \leq 10\text{sec}$ .

<sup>a3</sup>: Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

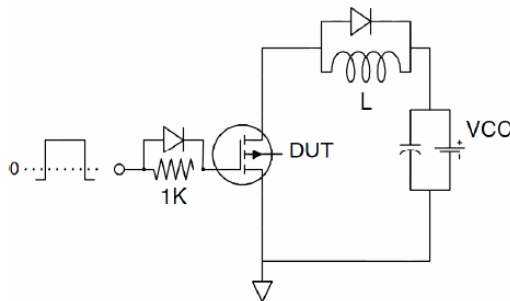
<sup>a4</sup>: Guaranteed by design, not subject to production

### Test circuit

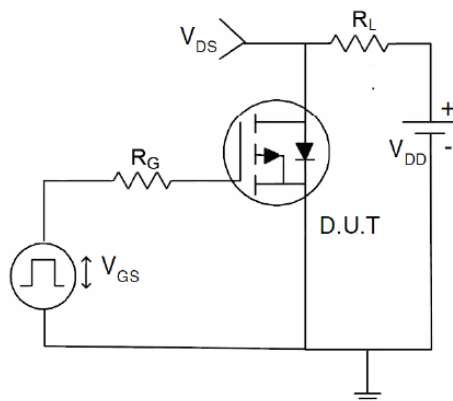
#### 1) $E_{AS}$ Test Circuit



#### 2) Gate Charge Test Circuit



#### 3) Switch Time Test Circuit





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### P-Channel Typical Electrical and Thermal Characteristics (Curves)

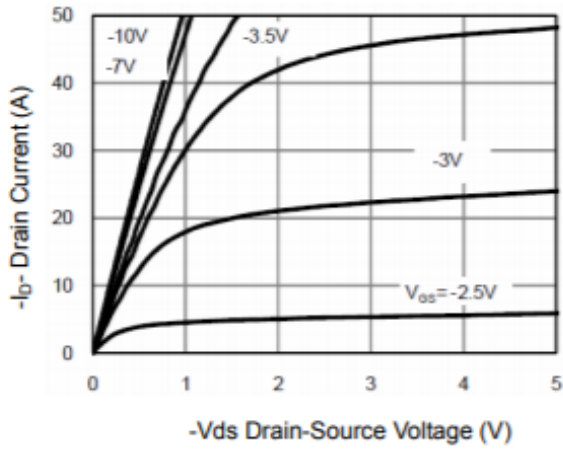


Figure 1 Output Characteristics

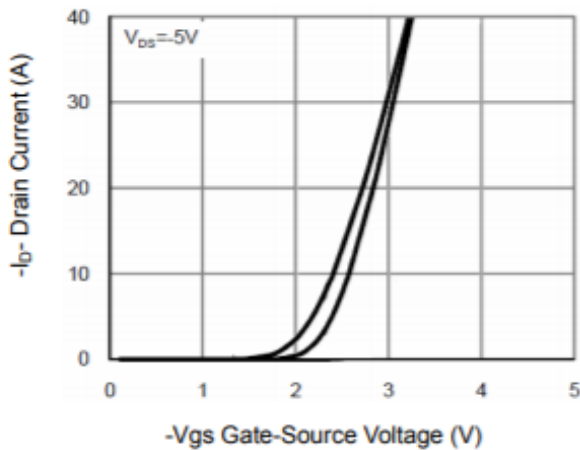


Figure 2 Transfer Characteristics

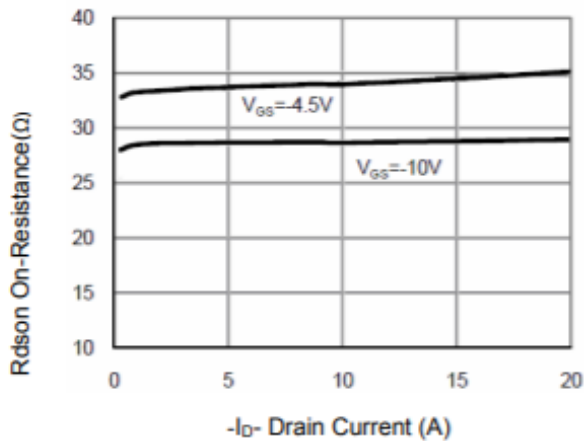


Figure 3  $R_{DS(on)}$ - Drain Current

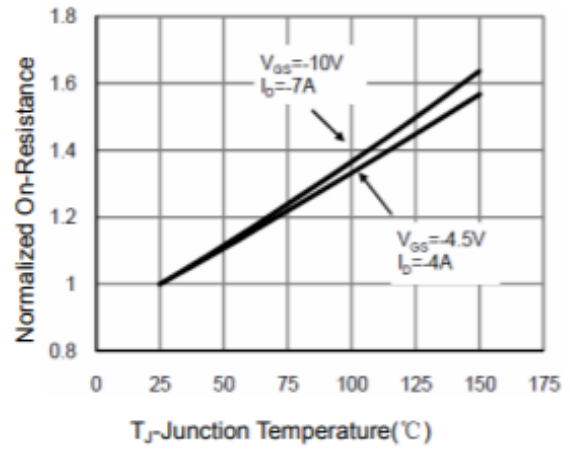


Figure 4  $R_{DS(on)}$ -Junction Temperature

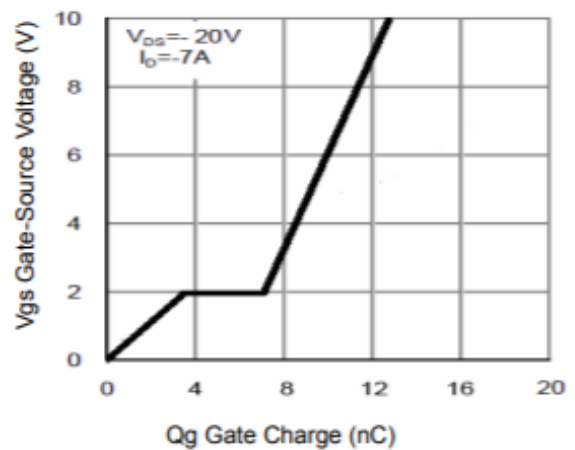


Figure 5 Gate Charge

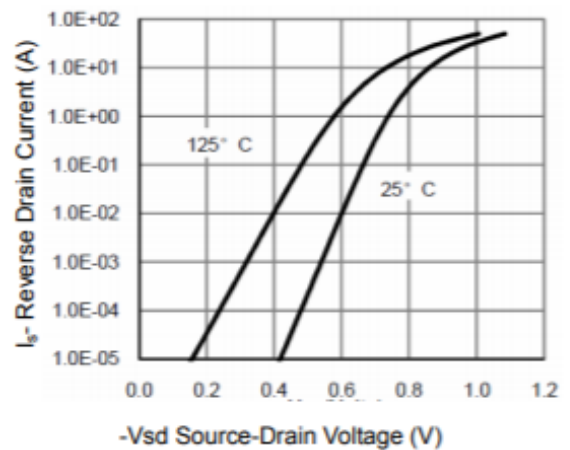


Figure 6 Source- Drain Diode Forward



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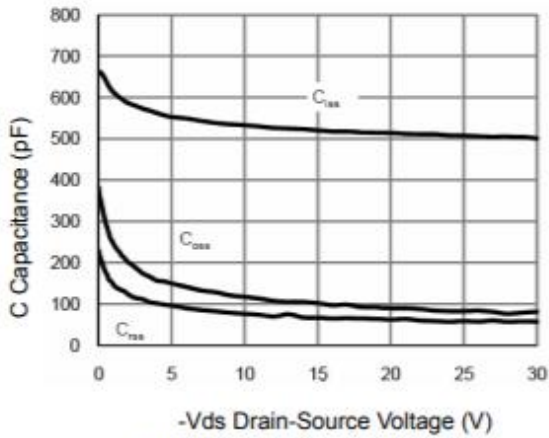


Figure 7 Capacitance vs Vds

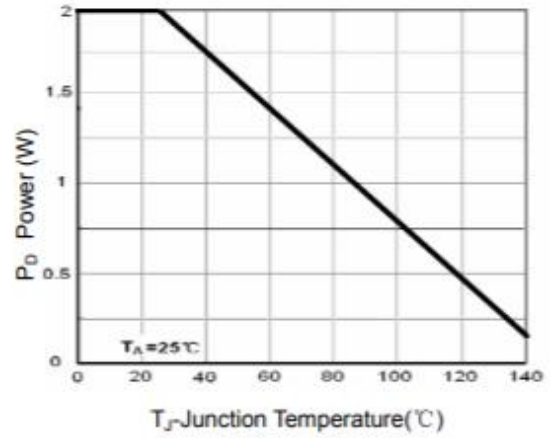


Figure 9 Power Dissipation

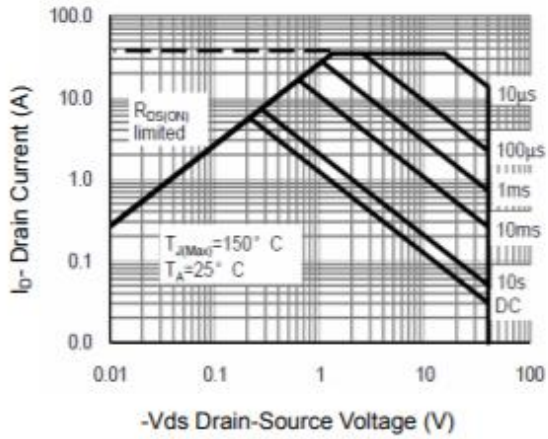


Figure 8 Safe Operation Area

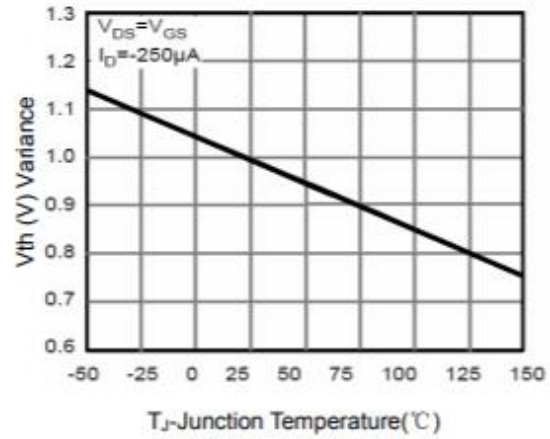


Figure 10  $V_{GS(th)}$  vs Junction Temperature

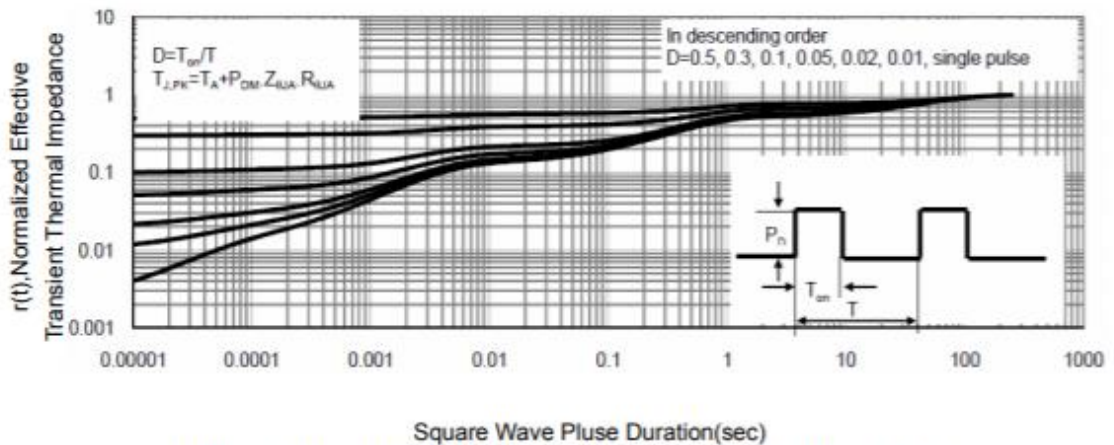


Figure 11 Normalized Maximum Transient Thermal Impedance