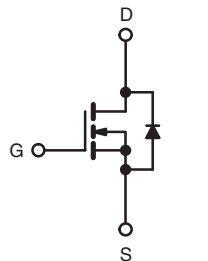


Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	100
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$ 0.27
Q_g (Max.) (nC)	16
Q_{gs} (nC)	4.4
Q_{gd} (nC)	7.7
Configuration	Single



N-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- 175 °C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC



Available

RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF520PbF
	SiHF520-E3
SnPb	IRF520
	SiHF520

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V_{DS}	100	V	
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current	V_{GS} at 10 V	I_D	$T_C = 25\text{ }^\circ\text{C}$	9.2	A
			$T_C = 100\text{ }^\circ\text{C}$	6.5	
Pulsed Drain Current ^a		I_{DM}	37		
Linear Derating Factor			0.40	W/ $^\circ\text{C}$	
Single Pulse Avalanche Energy ^b		E_{AS}	200	mJ	
Repetitive Avalanche Current ^a		I_{AR}	9.2	A	
Repetitive Avalanche Energy ^a		E_{AR}	6.0	mJ	
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	60	W	
Peak Diode Recovery dV/dt ^c		dV/dt	5.5	V/ns	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 175	$^\circ\text{C}$	
Soldering Recommendations (Peak Temperature)	for 10 s		300 ^d		
Mounting Torque	6-32 or M3 screw		10		lbf · in
			1.1	N · m	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 3.5\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 9.2\text{ A}$ (see fig. 12).
- $I_{SD} \leq 9.2\text{ A}$, $dI/dt \leq 110\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 175\text{ }^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

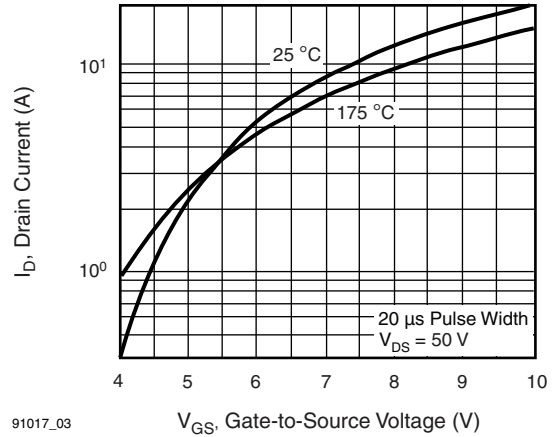
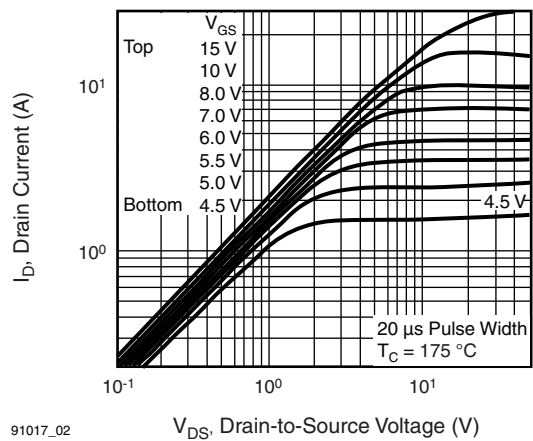
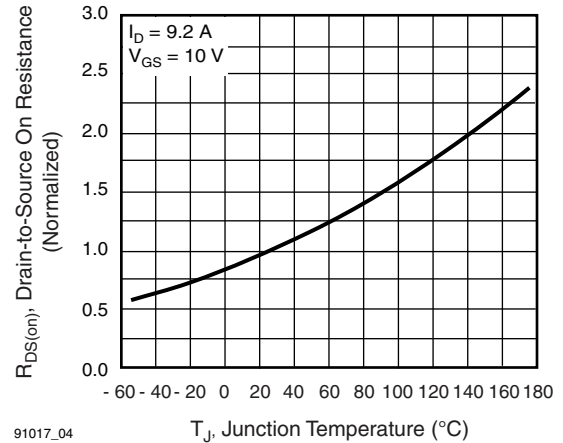
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	2.5	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$	-	0.13	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	μA
		$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 5.5\text{ A}^b$	-	-	0.27	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 5.5\text{ A}^b$	2.7	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz},$ see fig. 5	-	360	-	pF
Output Capacitance	C_{oss}		-	150	-	
Reverse Transfer Capacitance	C_{rss}		-	34	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V},$ $I_D = 9.2\text{ A}, V_{DS} = 80\text{ V},$ see fig. 6 and 13 ^b	-	-	16	nC
Gate-Source Charge	Q_{gs}		-	-	4.4	
Gate-Drain Charge	Q_{gd}		-	-	7.7	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\text{ V}, I_D = 9.2\text{ A},$ $R_g = 18\text{ }\Omega, R_D = 5.2\text{ }\Omega,$ see fig. 10 ^b	-	8.8	-	ns
Rise Time	t_r		-	30	-	
Turn-Off Delay Time	$t_{d(off)}$		-	19	-	
Fall Time	t_f		-	20	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	9.2	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	37	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 9.2\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.8	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 9.2\text{ A}, dl/dt = 100\text{ A}/\mu\text{s}^b$	-	110	260	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	0.53	1.3	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics, $T_C = 175\text{ }^\circ\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature



91017_05

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



91017_07

Fig. 7 - Typical Source-Drain Diode Forward Voltage



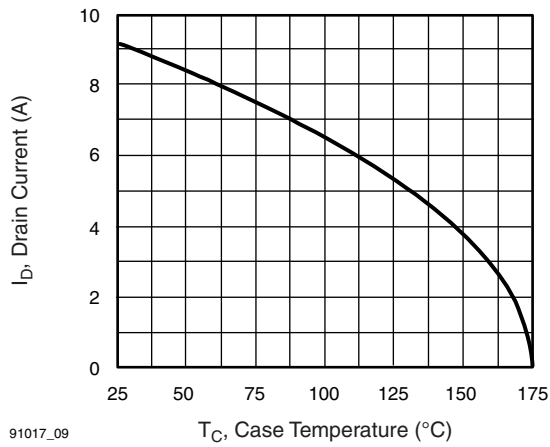
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Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



91017_08

Fig. 8 - Maximum Safe Operating Area



91017_09

Fig. 9 - Maximum Drain Current vs. Case Temperature

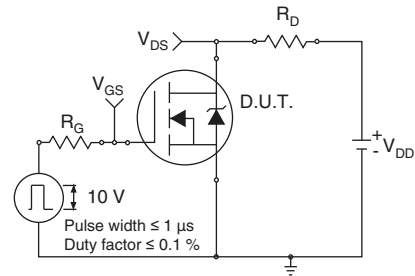
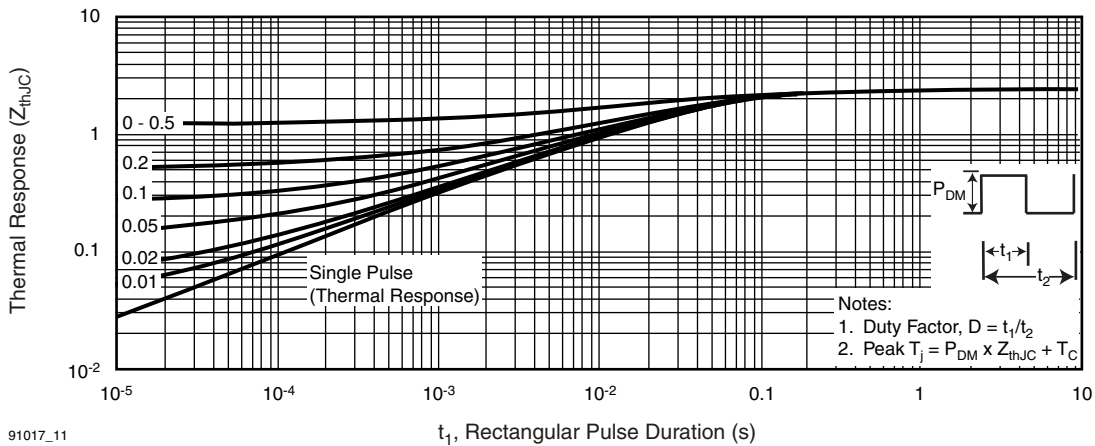


Fig. 10a - Switching Time Test Circuit



Fig. 10b - Switching Time Waveforms



91017_11

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

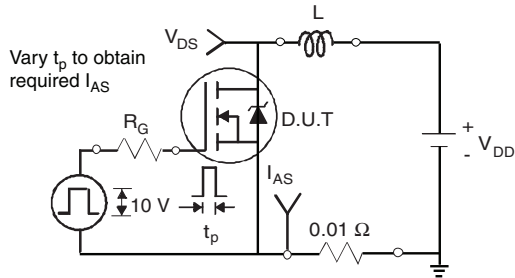


Fig. 12a - Unclamped Inductive Test Circuit



Fig. 12b - Unclamped Inductive Waveforms



91017_12c

Fig. 12c - Maximum Avalanche Energy vs. Drain Current



Fig. 13a - Basic Gate Charge Waveform

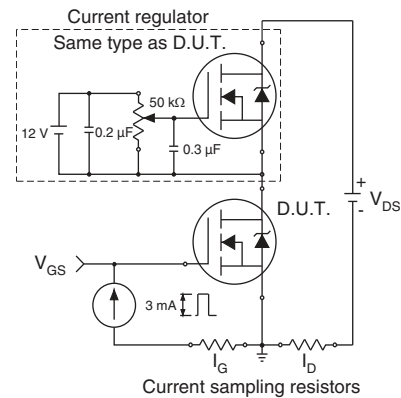


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note
a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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TO-220-1



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.14	4.70	0.163	0.185
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.73	0.045	0.068
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	0.43	1.40	0.017	0.055
H(1)	6.10	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.59	3.00	0.102	0.118

ECN: X15-0003-Rev. A, 19-Jan-15
DWG: 6031

Notes

- M* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM
- Outline conforms to JEDEC® outline TO-220AB with exception of dimension F





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