

FEATURES

Latch-up proof
 8 kV human body model (HBM) ESD rating
 Low on resistance (13.5 Ω)
 ± 9 V to ± 22 V dual-supply operation
 9 V to 40 V single-supply operation
 48 V supply maximum ratings
 Fully specified at ± 15 V, ± 20 V, +12 V, and +36 V
 V_{SS} to V_{DD} analog signal range

APPLICATIONS

Relay replacement
 Automatic test equipment
 Data acquisition
 Instrumentation
 Avionics
 Audio and video switching
 Communication systems

GENERAL DESCRIPTION

The ADG5408/ADG5409 are monolithic CMOS analog multiplexers comprising eight single channels and four differential channels, respectively. The ADG5408 switches one of eight inputs to a common output, as determined by the 3-bit binary address lines, A0, A1, and A2. The ADG5409 switches one of four differential inputs to a common differential output, as determined by the 2-bit binary address lines, A0 and A1.

An EN input on both devices enables or disables the device. When EN is disabled, all channels switch off. The on-resistance profile is very flat over the full analog input range, which ensures good linearity and low distortion when switching audio signals. High switching speed also makes the parts suitable for video signal switching.

Each switch conducts equally well in both directions when on, and each switch has an input signal range that extends to the power supplies. In the off condition, signal levels up to the supplies are blocked.

FUNCTIONAL BLOCK DIAGRAMS

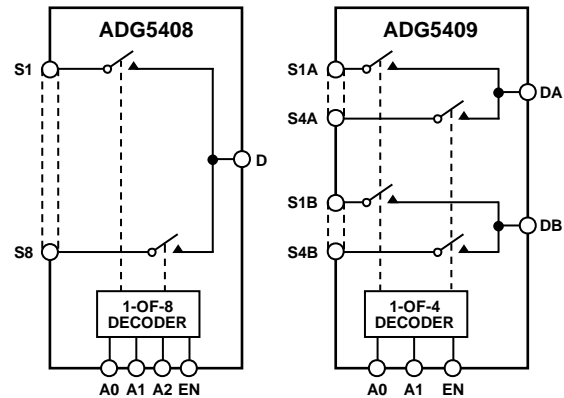


Figure 1.

The ADG5408/ADG5409 do not have V_L pins; rather, the logic power supply is generated internally by an on-chip voltage generator.

PRODUCT HIGHLIGHTS

1. Trench isolation guards against latch-up. A dielectric trench separates the P and N channel transistors thereby preventing latch-up even under severe overvoltage conditions.
2. Low R_{ON} .
3. Dual-supply operation. For applications where the analog signal is bipolar, the ADG5408/ADG5409 can be operated from dual supplies up to ± 22 V.
4. Single-supply operation. For applications where the analog signal is unipolar, the ADG5408/ADG5409 can be operated from a single rail power supply up to 40 V.
5. 3 V logic compatible digital inputs: $V_{INH} = 2.0$ V, $V_{INL} = 0.8$ V.
6. No V_L logic power supply required.

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REVISION HISTORY

3/13—Rev. B to Rev. C

Changes to Table 5 and Table 6.....	8
Changed ADG5408 Peak Current from 370 mA to 435 mA; Changed ADG5409 Peak Current from 275 mA to 300 mA; Changed Reflow Soldering Peak Temperature, Pb Free from 260(+0/-5)°C to As per JEDEC J-STD-020; Table 7	9
Changes to Figure 25, Figure 26, and Figure 29	16

5/12—Rev. A to Rev. B

Removed Automotive Information (Throughout).....	1
Changes to Ordering Guide	22
Deleted Automotive Products Section.....	22

6/11—Rev. 0 to Rev. A

Change to Features Section	1
Change to I _{SS} Parameter, Table 2.....	5
Changes to Figure 3.....	10
Changes to Figure 5.....	11
Updated Outline Dimensions	21
Changes to Ordering Guide	21
Added Automotive Products Section.....	21

7/10—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	13.5			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$; see Figure 26
	15	18	22	Ω max	$V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$
On-Resistance Match Between Channels, ΔR_{ON}	0.3			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
	0.8	1.3	1.4	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	1.8			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
	2.2	2.6	3	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.05			nA typ	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$
	± 0.25	± 1	± 7	nA max	$V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$; see Figure 29
Drain Off Leakage, I_D (Off)	± 0.1			nA typ	$V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$; see Figure 29
	± 0.4	± 4	± 30	nA max	
Channel On Leakage, I_D (On), I_S (On)	± 0.1			nA typ	$V_S = V_D = \pm 10\text{ V}$; see Figure 25
	± 0.4	± 4	± 30	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	μA max	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{TRANSITION}$	170			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	217	258	292	ns max	$V_S = 10\text{ V}$; see Figure 32
t_{ON} (EN)	140			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	175	213	242	ns max	$V_S = 10\text{ V}$; see Figure 34
t_{OFF} (EN)	130			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	161	183	198	ns max	$V_S = 10\text{ V}$; see Figure 34
Break-Before-Make Time Delay, t_D	50			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
			16	ns min	$V_{S1} = V_{S2} = 10\text{ V}$; see Figure 33
Charge Injection, Q_{INJ}	115			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 35
Off Isolation	-60			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 28
Channel-to-Channel Crosstalk	-60			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 27
Total Harmonic Distortion + Noise	0.01			% typ	$R_L = 1\text{ k}\Omega$, 15 V p-p , $f = 20\text{ Hz to }20\text{ kHz}$; see Figure 30
-3 dB Bandwidth					$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 31
ADG5408	50			MHz typ	
ADG5409	87			MHz typ	
Insertion Loss	0.9			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Figure 31
C_S (Off)	15			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (Off)					
ADG5408	102			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
ADG5409	50			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
C_D (On), C_S (On)					
ADG5408	133			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
ADG5409	81			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
POWER REQUIREMENTS					$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$
I_{DD}	45		70	$\mu\text{A typ}$	Digital inputs = 0 V or V_{DD}
	55			$\mu\text{A max}$	
I_{SS}	0.001		1	$\mu\text{A typ}$	Digital inputs = 0 V or V_{DD}
				$\mu\text{A max}$	
V_{DD}/V_{SS}			$\pm 9/\pm 22$	V min/V max	GND = 0 V

¹ Guaranteed by design; not subject to production test.

±20 V DUAL SUPPLY

$V_{DD} = +20\text{ V} \pm 10\%$, $V_{SS} = -20\text{ V} \pm 10\%$, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analogue Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	12.5			Ω typ	$V_S = \pm 15\text{ V}$, $I_S = -10\text{ mA}$; see Figure 26
	14	17	21	Ω max	$V_{DD} = +18\text{ V}$, $V_{SS} = -18\text{ V}$
On-Resistance Match Between Channels, ΔR_{ON}	0.3			Ω typ	$V_S = \pm 15\text{ V}$, $I_S = -10\text{ mA}$
On-Resistance Flatness, $R_{FLAT(ON)}$	0.8	1.3	1.4	Ω max	
	2.3			Ω typ	$V_S = \pm 15\text{ V}$, $I_S = -10\text{ mA}$
	2.7	3.1	3.5	Ω max	
LEAKAGE CURRENTS					$V_{DD} = +22\text{ V}$, $V_{SS} = -22\text{ V}$
Source Off Leakage, I_S (Off)	± 0.1			nA typ	$V_S = \pm 15\text{ V}$, $V_D = \mp 15\text{ V}$; see Figure 29
	± 0.25	± 1	± 7	nA max	
Drain Off Leakage, I_D (Off)	± 0.15			nA typ	$V_S = \pm 15\text{ V}$, $V_D = \mp 15\text{ V}$; see Figure 29
	± 0.4	± 4	± 30	nA max	
Channel On Leakage, I_D (On), I_S (On)	± 0.15			nA typ	$V_S = V_D = \pm 15\text{ V}$; see Figure 25
	± 0.4	± 4	± 30	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			$\mu\text{A typ}$	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	$\mu\text{A max}$	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS ¹					
Transition Time, $t_{TRANSITION}$	160			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	207	237	262	ns max	$V_S = 10\text{ V}$; see Figure 32
t_{ON} (EN)	140			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	165	194	218	ns max	$V_S = 10\text{ V}$; see Figure 34
t_{OFF} (EN)	133			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	153	174	189	ns max	$V_S = 10\text{ V}$; see Figure 34
Break-Before-Make Time Delay, t_D	38			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
			11	ns min	$V_{S1} = V_{S2} = 10\text{ V}$; see Figure 33
Charge Injection, Q_{INJ}	155			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 35
Off Isolation	-60			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 28
Channel-to-Channel Crosstalk	-60			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 27

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
Total Harmonic Distortion + Noise	0.012			% typ	$R_L = 1\text{ k}\Omega$, 20 V p-p, $f = 20\text{ Hz to }20\text{ kHz}$; see Figure 30
-3 dB Bandwidth					$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 31
ADG5408	50			MHz typ	
ADG5409	88			MHz typ	
Insertion Loss	0.8			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 31
C_S (Off)	17			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (Off)					
ADG5408	98			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
ADG5409	48			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (On), C_S (On)					
ADG5408	128			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
ADG5409	80			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	50			$\mu\text{A typ}$	$V_{DD} = +22\text{ V}$, $V_{SS} = -22\text{ V}$
	70		110	$\mu\text{A max}$	Digital inputs = 0 V or V_{DD}
I_{SS}	0.001			$\mu\text{A typ}$	Digital inputs = 0 V or V_{DD}
			1	$\mu\text{A max}$	
V_{DD}/V_{SS}			$\pm 9/\pm 22$	V min/V max	GND = 0 V

¹ Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	26			Ω typ	$V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$; see Figure 26
	30	36	42	Ω max	$V_{DD} = 10.8\text{ V}$, $V_{SS} = 0\text{ V}$
On-Resistance Match Between Channels, ΔR_{ON}	0.3			Ω typ	$V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$
	1	1.5	1.6	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	5.5			Ω typ	$V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$
	6.5	8	12	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.02			nA typ	$V_{DD} = 13.2\text{ V}$, $V_{SS} = 0\text{ V}$
	± 0.25	± 1	± 7	nA max	$V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$; see Figure 29
Drain Off Leakage, I_D (Off)	± 0.05			nA typ	$V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$; see Figure 29
	± 0.4	± 4	± 30	nA max	
Channel On Leakage, I_D (On), I_S (On)	± 0.05			nA typ	$V_S = V_D = 1\text{ V}/10\text{ V}$; see Figure 25
	± 0.4	± 4	± 30	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			$\mu\text{A typ}$	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	$\mu\text{A max}$	
Digital Input Capacitance, C_{IN}	3			pF typ	

Parameter	25°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{\text{TRANSITION}}$	230			ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$
	321	388	430	ns max	$V_S = 8 \text{ V}$; see Figure 32
$t_{\text{ON}} (\text{EN})$	215			ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$
	276	345	397	ns max	$V_S = 8 \text{ V}$; see Figure 34
$t_{\text{OFF}} (\text{EN})$	134			ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$
	161	187	209	ns max	$V_S = 8 \text{ V}$; see Figure 34
Break-Before-Make Time Delay, t_D	118			ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$
			55	ns min	$V_{S1} = V_{S2} = 8 \text{ V}$; see Figure 33
Charge Injection, Q_{INJ}	45			pC typ	$V_S = 6 \text{ V}$, $R_S = 0 \Omega$, $C_L = 1 \text{ nF}$; see Figure 35
Off Isolation	–60			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$; see Figure 28
Channel-to-Channel Crosstalk	–60			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$; see Figure 27
Total Harmonic Distortion + Noise	0.1			% typ	$R_L = 1 \text{ k}\Omega$, 6 V p-p , $f = 20 \text{ Hz to } 20 \text{ kHz}$; see Figure 30
–3 dB Bandwidth					$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$; see Figure 31
ADG5408	35			MHz typ	
ADG5409	74			MHz typ	
Insertion Loss	–1.8			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$; see Figure 31
C_S (Off)	22			pF typ	$V_S = 6 \text{ V}$, $f = 1 \text{ MHz}$
C_D (Off)					
ADG5408	119			pF typ	$V_S = 6 \text{ V}$, $f = 1 \text{ MHz}$
ADG5409	59			pF typ	$V_S = 6 \text{ V}$, $f = 1 \text{ MHz}$
C_D (On), C_S (On)					
ADG5408	146			pF typ	$V_S = 6 \text{ V}$, $f = 1 \text{ MHz}$
ADG5409	86			pF typ	$V_S = 6 \text{ V}$, $f = 1 \text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	40			$\mu\text{A typ}$	$V_{\text{DD}} = 13.2 \text{ V}$
	50		65	$\mu\text{A max}$	Digital inputs = 0 V or V_{DD}
V_{DD}			9/40	V min/V max	$\text{GND} = 0 \text{ V}$, $V_{\text{SS}} = 0 \text{ V}$

¹ Guaranteed by design; not subject to production test.

36 V SINGLE SUPPLY

$V_{\text{DD}} = 36 \text{ V} \pm 10\%$, $V_{\text{SS}} = 0 \text{ V}$, $\text{GND} = 0 \text{ V}$, unless otherwise noted.

Table 4.

Parameter	25°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	14.5			Ω typ	$V_S = 0 \text{ V to } 30 \text{ V}$, $I_S = -10 \text{ mA}$; see Figure 26
	16	19	23	Ω max	$V_{\text{DD}} = 32.4 \text{ V}$, $V_{\text{SS}} = 0 \text{ V}$
On-Resistance Match Between Channels, ΔR_{ON}	0.3			Ω typ	$V_S = 0 \text{ V to } 30 \text{ V}$, $I_S = -10 \text{ mA}$
	0.8	1.3	1.4	Ω max	
On-Resistance Flatness, $R_{\text{FLAT}} (\text{ON})$	3.5			Ω typ	$V_S = 0 \text{ V to } 30 \text{ V}$, $I_S = -10 \text{ mA}$
	4.3	5.5	6.5	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.1			nA typ	$V_{\text{DD}} = 39.6 \text{ V}$, $V_{\text{SS}} = 0 \text{ V}$
	± 0.25	± 1	± 7	nA max	$V_S = 1 \text{ V}/30 \text{ V}$, $V_D = 30 \text{ V}/1 \text{ V}$; see Figure 29

Parameter	25°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
Drain Off Leakage, I_D (Off)	±0.15			nA typ	$V_S = 1\text{ V}/30\text{ V}$, $V_D = 30\text{ V}/1\text{ V}$; see Figure 29
Channel On Leakage, I_D (On), I_S (On)	±0.4	±4	±30	nA max	$V_S = V_D = 1\text{ V}/30\text{ V}$; see Figure 25
	±0.15			nA typ	
	±0.4	±4	±30	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	$V_{IN} = V_{GND}$ or V_{DD}
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002		±0.1	µA typ	
Digital Input Capacitance, C_{IN}	3			µA max pF typ	
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{TRANSITION}$	187			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	242	257	281	ns max	$V_S = 18\text{ V}$; see Figure 32
t_{ON} (EN)	160			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	195	219	237	ns max	$V_S = 18\text{ V}$; see Figure 34
t_{OFF} (EN)	147			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	184	184	190	ns max	$V_S = 18\text{ V}$; see Figure 34
Break-Before-Make Time Delay, t_D	53			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
Charge Injection, Q_{INJ}	150		17	ns min	$V_{S1} = V_{S2} = 18\text{ V}$; see Figure 33
Off Isolation	–60			pC typ	$V_S = 18\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 35
Channel-to-Channel Crosstalk	–60			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 28
Total Harmonic Distortion + Noise	0.4			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 27
–3 dB Bandwidth				% typ	$R_L = 1\text{ k}\Omega$, 18 V p-p, $f = 20\text{ Hz}$ to 20 kHz; see Figure 30
	ADG5408			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 31
ADG5409	45			MHz typ	
Insertion Loss	76			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 31
	–1			dB typ	
C_S (Off)	18			pF typ	$V_S = 18\text{ V}$, $f = 1\text{ MHz}$
C_D (Off)				pF typ	$V_S = 18\text{ V}$, $f = 1\text{ MHz}$
	ADG5408	120		pF typ	$V_S = 18\text{ V}$, $f = 1\text{ MHz}$
ADG5409	60			pF typ	$V_S = 18\text{ V}$, $f = 1\text{ MHz}$
C_D (On), C_S (On)				pF typ	$V_S = 18\text{ V}$, $f = 1\text{ MHz}$
	ADG5408	137		pF typ	$V_S = 18\text{ V}$, $f = 1\text{ MHz}$
ADG5409	80			pF typ	$V_S = 18\text{ V}$, $f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	80			µA typ	$V_{DD} = 39.6\text{ V}$
	100		130	µA max	Digital inputs = 0 V or V_{DD}
V_{DD}			9/40	V min/V max	$GND = 0\text{ V}$, $V_{SS} = 0\text{ V}$

¹ Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, Sx OR D

Table 5. ADG5408

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR D				
$V_{DD} = +15\text{ V}, V_{SS} = -15\text{ V}$				
TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	120	78	50	mA maximum
LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	207	113	60	mA maximum
$V_{DD} = +20\text{ V}, V_{SS} = -20\text{ V}$				
TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	127	81	51	mA maximum
LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	218	117	61	mA maximum
$V_{DD} = 12\text{ V}, V_{SS} = 0\text{ V}$				
TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	97	66	44	mA maximum
LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	168	99	57	mA maximum
$V_{DD} = 36\text{ V}, V_{SS} = 0\text{ V}$				
TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	125	80	50	mA maximum
LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	214	116	61	mA maximum

Table 6. ADG5409

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR D				
$V_{DD} = +15\text{ V}, V_{SS} = -15\text{ V}$				
TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	90	62	43	mA maximum
LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	156	95	55	mA maximum
$V_{DD} = +20\text{ V}, V_{SS} = -20\text{ V}$				
TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	95	65	44	mA maximum
LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	165	98	56	mA maximum
$V_{DD} = 12\text{ V}, V_{SS} = 0\text{ V}$				
TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	71	51	35	mA maximum
LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	126	81	50	mA maximum
$V_{DD} = 36\text{ V}, V_{SS} = 0\text{ V}$				
TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	92	64	43	mA maximum
LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	161	97	56	mA maximum

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 7.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	-0.3 V to +48 V
V_{SS} to GND	+0.3 V to -48 V
Analog Inputs ¹	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs ¹	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, Sx or D Pins	
ADG5408	435 mA (pulsed at 1 ms, 10% duty cycle maximum)
ADG5409	300 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or D ²	Data + 15%
Temperature Range	
Operating	-40°C to +125°C
Storage	-65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA}	
16-Lead TSSOP (4-Layer Board)	112.6°C/W
16-Lead LFCSP (4-Layer Board)	30.4°C/W
Reflow Soldering Peak Temperature, Pb Free	As per JEDEC J-STD-020

¹ Overvoltages at the Ax, EN, Sx, and D pins are clamped by internal diodes. Limit current to the maximum ratings given.

² See Table 5.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

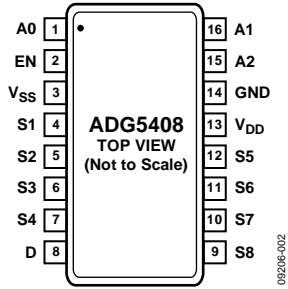
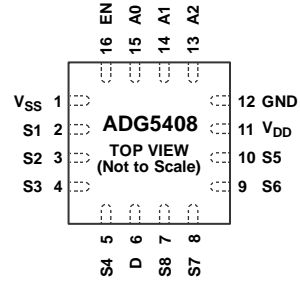


Figure 2. ADG5408 Pin Configuration (TSSOP)



NOTES
 1. THE EXPOSED PAD IS CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE SUBSTRATE, V_{SS}.

Figure 3. ADG5408 Pin Configuration (LFCSP)

Table 8. ADG5408 Pin Function Descriptions

Pin No.		Mnemonic	Description
TSSOP	LFCSP		
1	15	A0	Logic Control Input.
2	16	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
3	1	V _{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
4	2	S1	Source Terminal 1. This pin can be an input or an output.
5	3	S2	Source Terminal 2. This pin can be an input or an output.
6	4	S3	Source Terminal 3. This pin can be an input or an output.
7	5	S4	Source Terminal 4. This pin can be an input or an output.
8	6	D	Drain Terminal. This pin can be an input or an output.
9	7	S8	Source Terminal 8. This pin can be an input or an output.
10	8	S7	Source Terminal 7. This pin can be an input or an output.
11	9	S6	Source Terminal 6. This pin can be an input or an output.
12	10	S5	Source Terminal 5. This pin can be an input or an output.
13	11	V _{DD}	Most Positive Power Supply Potential.
14	12	GND	Ground (0 V) Reference.
15	13	A2	Logic Control Input.
16	14	A1	Logic Control Input.
	EP	Exposed Pad	The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V _{SS} .

Table 9. ADG5408 Truth Table

A2	A1	A0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

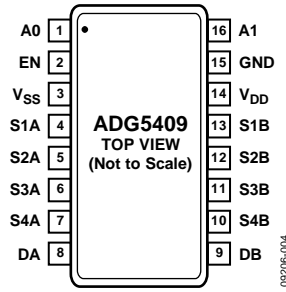
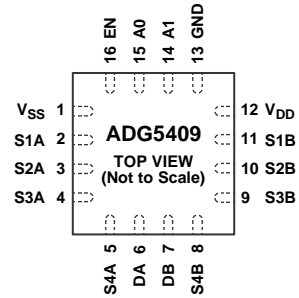


Figure 4. ADG5409 Pin Configuration (TSSOP)



NOTES
 1. THE EXPOSED PAD IS CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE SUBSTRATE, V_{SS}.

Figure 5. ADG5409 Pin Configuration (LFCSP)

Table 10. ADG5409 Pin Function Descriptions

Pin No.		Mnemonic	Description
TSSOP	LFCSP		
1	15	A0	Logic Control Input.
2	16	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, A _x logic inputs determine on switches.
3	1	V _{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
4	2	S1A	Source Terminal 1A. This pin can be an input or an output.
5	3	S2A	Source Terminal 2A. This pin can be an input or an output.
6	4	S3A	Source Terminal 3A. This pin can be an input or an output.
7	5	S4A	Source Terminal 4A. This pin can be an input or an output.
8	6	DA	Drain Terminal A. This pin can be an input or an output.
9	7	DB	Drain Terminal B. This pin can be an input or an output.
10	8	S4B	Source Terminal 4B. This pin can be an input or an output.
11	9	S3B	Source Terminal 3B. This pin can be an input or an output.
12	10	S2B	Source Terminal 2B. This pin can be an input or an output.
13	11	S1B	Source Terminal 1B. This pin can be an input or an output.
14	12	V _{DD}	Most Positive Power Supply Potential.
15	13	GND	Ground (0 V) Reference.
16	14	A1	Logic Control Input.
	EP	Exposed Pad	The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V _{SS} .

Table 11. ADG5409 Truth Table

A1	A0	EN	On Switch Pair
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

TYPICAL PERFORMANCE CHARACTERISTICS

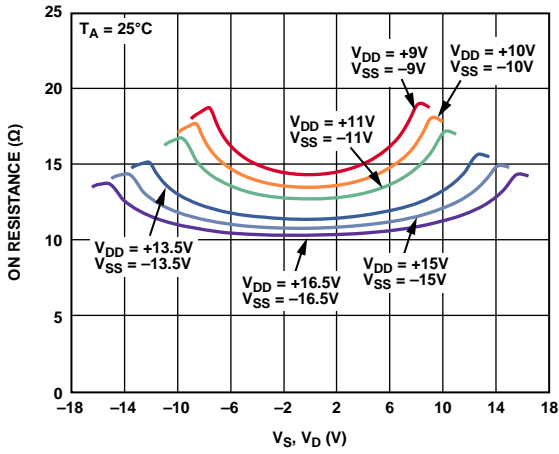


Figure 6. R_{ON} as a Function of V_S, V_D (Dual Supply)

09206-028

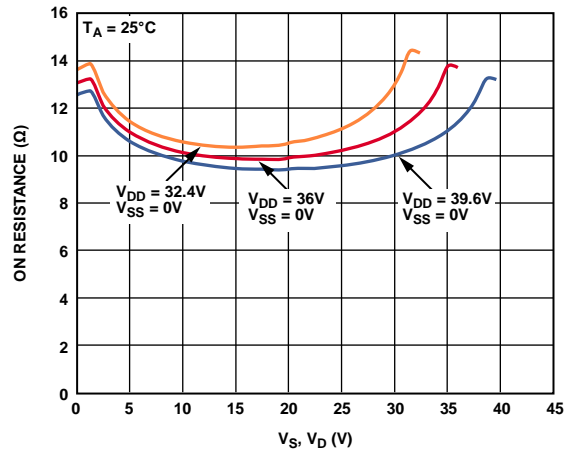


Figure 9. R_{ON} as a Function of V_S, V_D (Single Supply)

09206-027

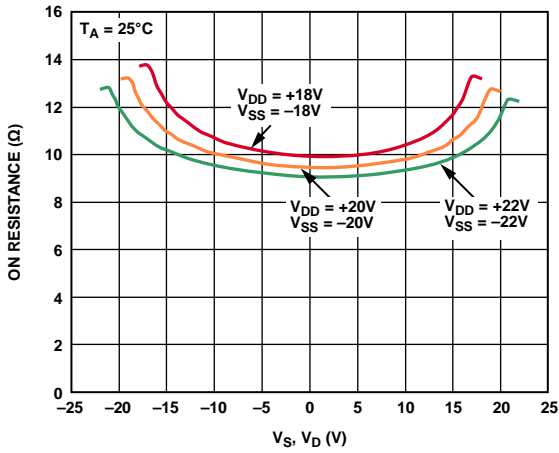


Figure 7. R_{ON} as a Function of V_S, V_D (Dual Supply)

09206-029

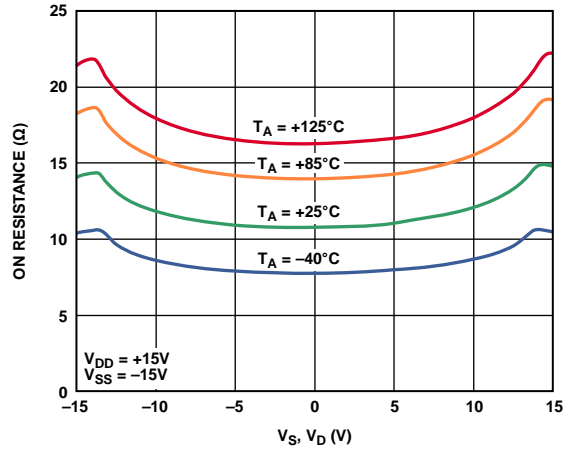


Figure 10. R_{ON} as a Function of $V_S (V_D)$ for Different Temperatures, ± 15 V Dual Supply

09206-030

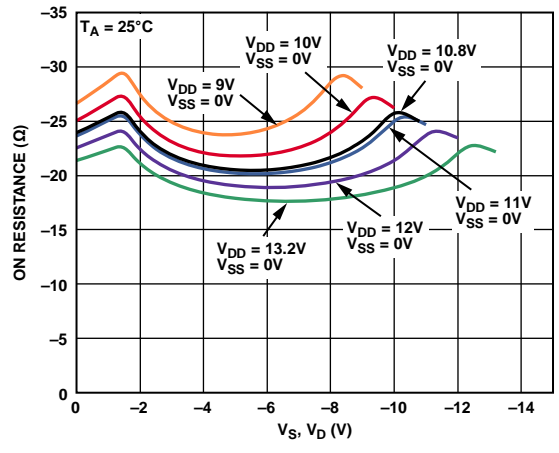


Figure 8. R_{ON} as a Function of V_S, V_D (Single Supply)

09206-023

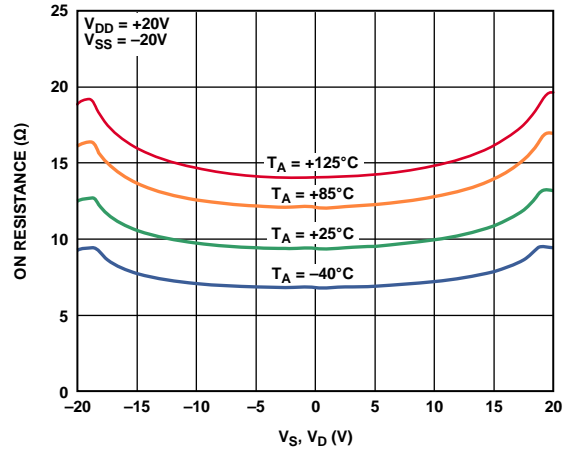


Figure 11. R_{ON} as a Function of $V_S (V_D)$ for Different Temperatures, ± 20 V Dual Supply

09206-024

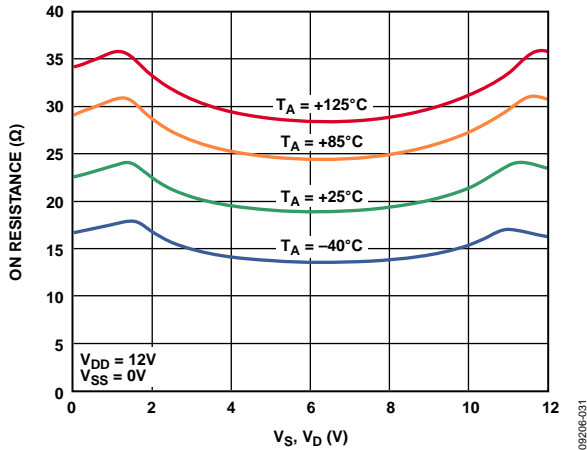


Figure 12. R_{ON} as a Function of V_S (V_D) for Different Temperatures, 12 V Single Supply

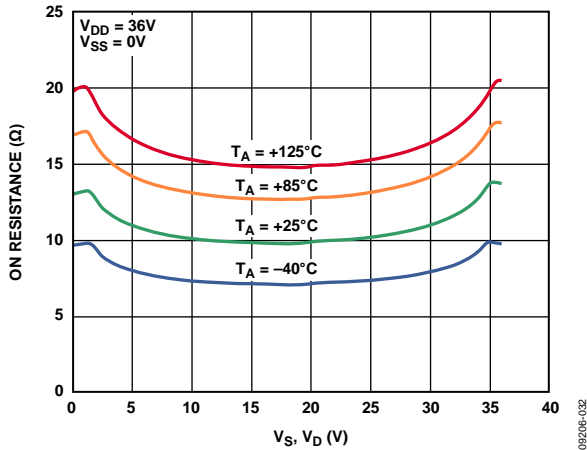


Figure 13. R_{ON} as a Function of V_D (V_S) for Different Temperatures, 36 V Single Supply

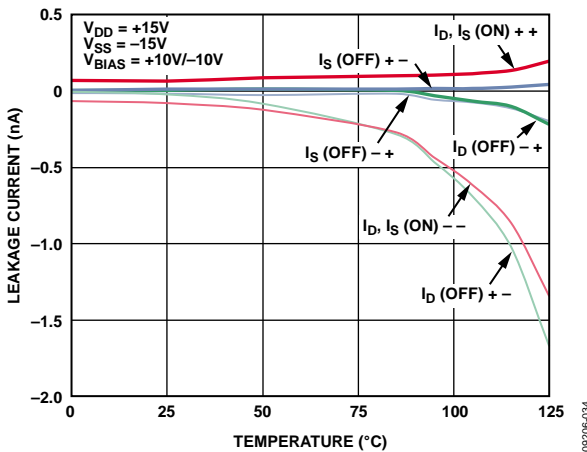


Figure 14. Leakage Currents vs. Temperature, ±15 V Dual Supply

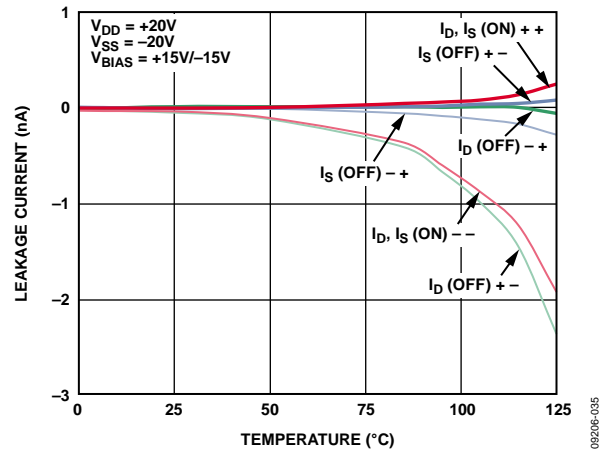


Figure 15. Leakage Currents vs. Temperature, ±20 V Dual Supply

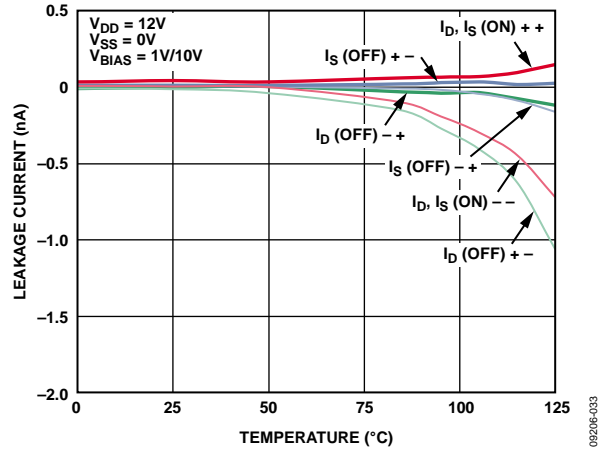


Figure 16. Leakage Currents vs. Temperature, 12 V Single Supply

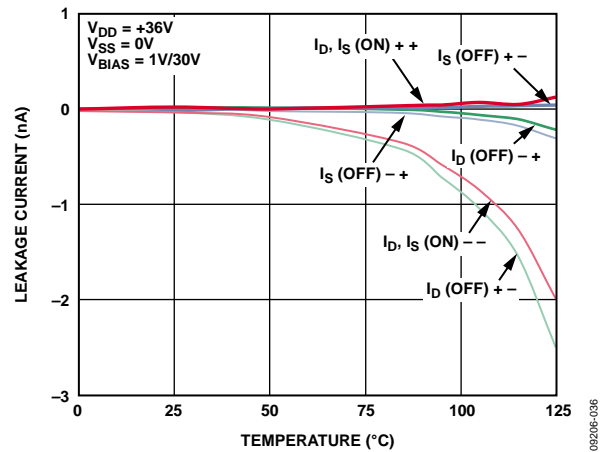


Figure 17. Leakage Currents vs. Temperature, 36 V Single Supply

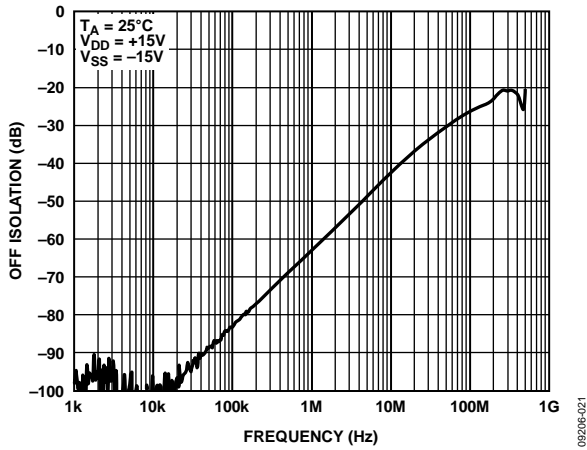


Figure 18. Off Isolation vs. Frequency, ±15 V Dual Supply

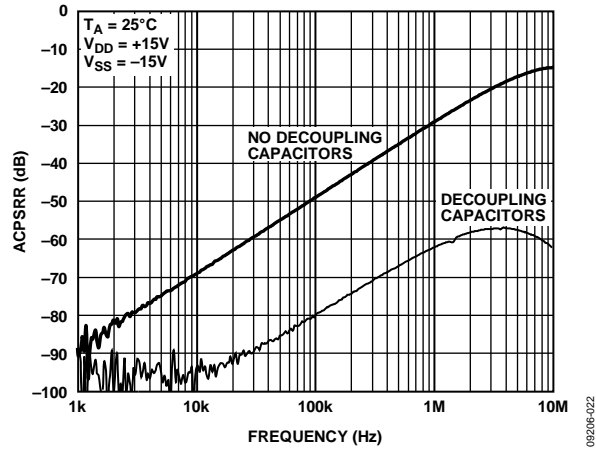


Figure 21. ACPSRR vs. Frequency, ±15 V Dual Supply

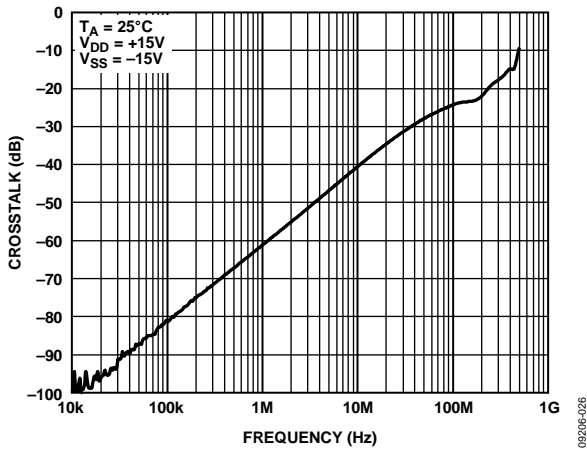


Figure 19. Crosstalk vs. Frequency, ±15 V Dual Supply

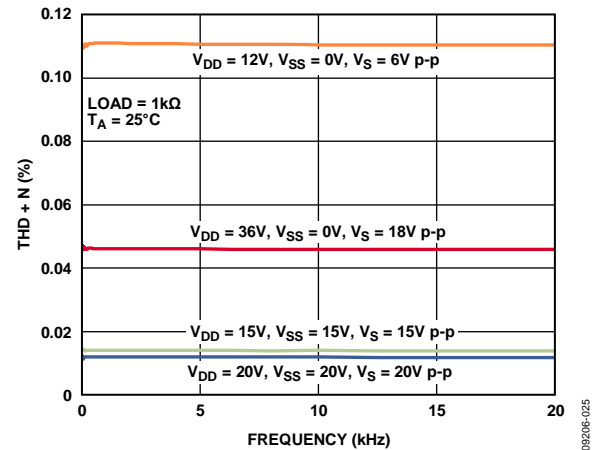


Figure 22. THD + N vs. Frequency

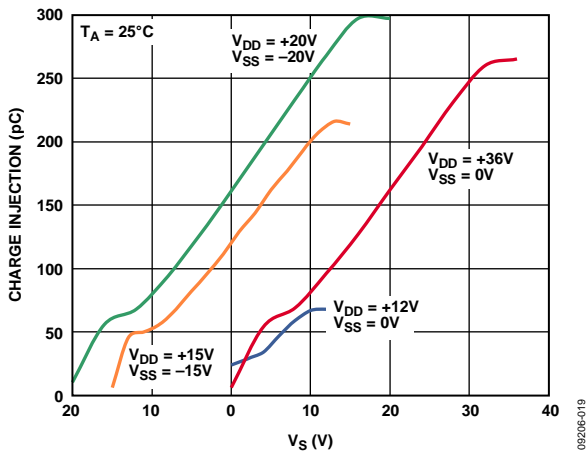


Figure 20. Charge Injection vs. Source Voltage

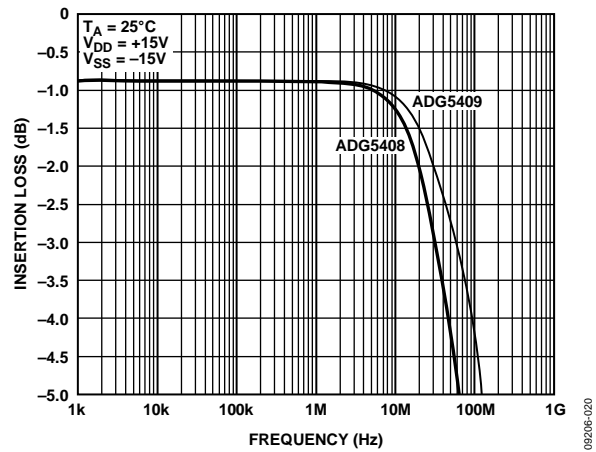


Figure 23. Bandwidth

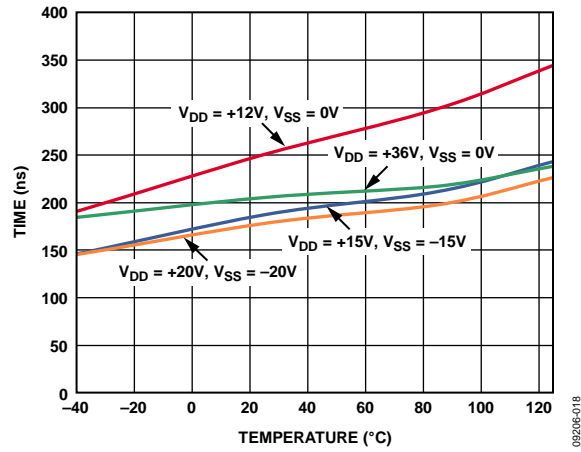


Figure 24. $t_{TRANSITION}$ Times vs. Temperature

09208-018

TEST CIRCUITS

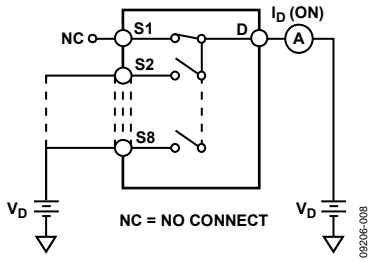


Figure 25. On Leakage

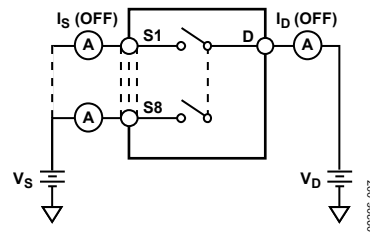


Figure 29. Off Leakage

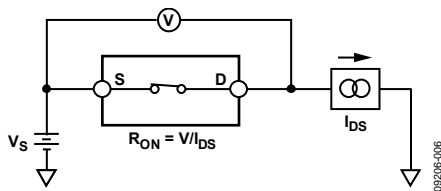


Figure 26. On Resistance

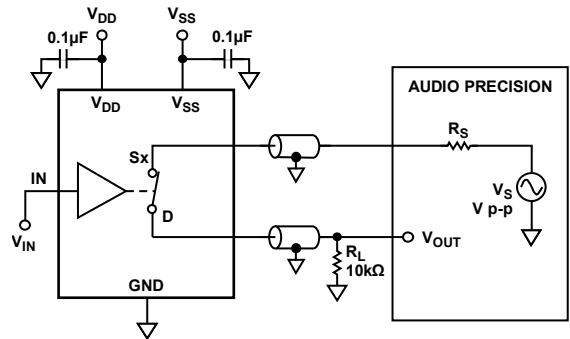
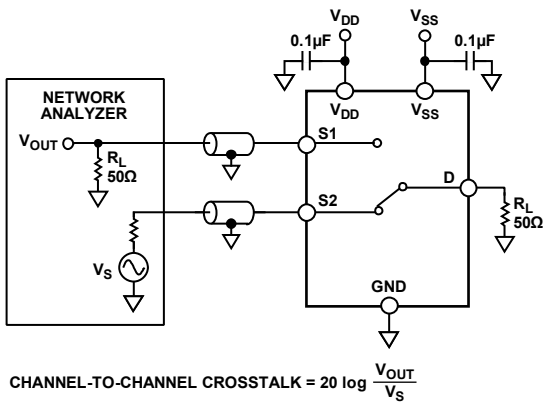
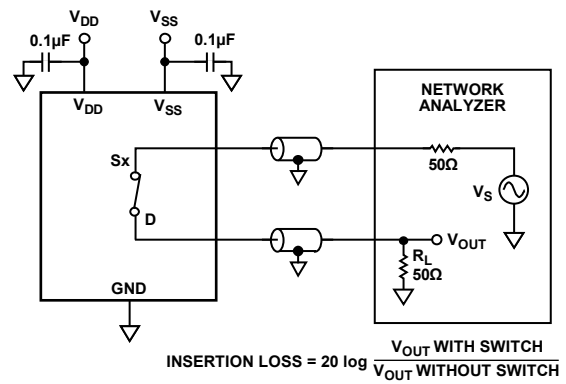


Figure 30. THD + Noise Figure



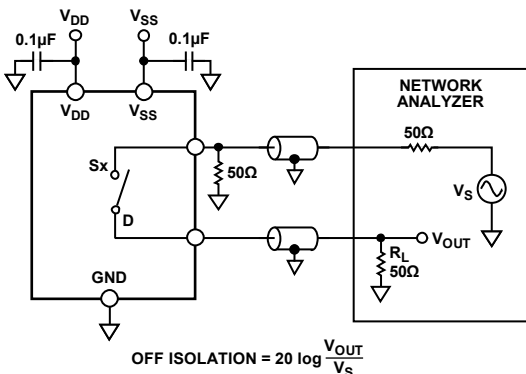
$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{OUT}}{V_S}$$

Figure 27. Channel-to-Channel Crosstalk



$$\text{INSERTION LOSS} = 20 \log \frac{V_{OUT \text{ WITH SWITCH}}}{V_{OUT \text{ WITHOUT SWITCH}}}$$

Figure 31. Bandwidth



$$\text{OFF ISOLATION} = 20 \log \frac{V_{OUT}}{V_S}$$

Figure 28. Off Isolation

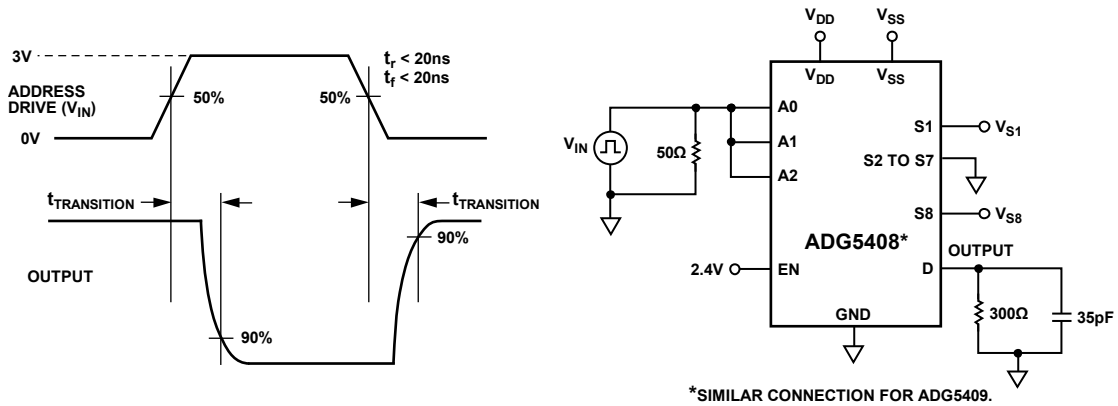


Figure 32. Address to Output Switching Times, $t_{TRANSITION}$

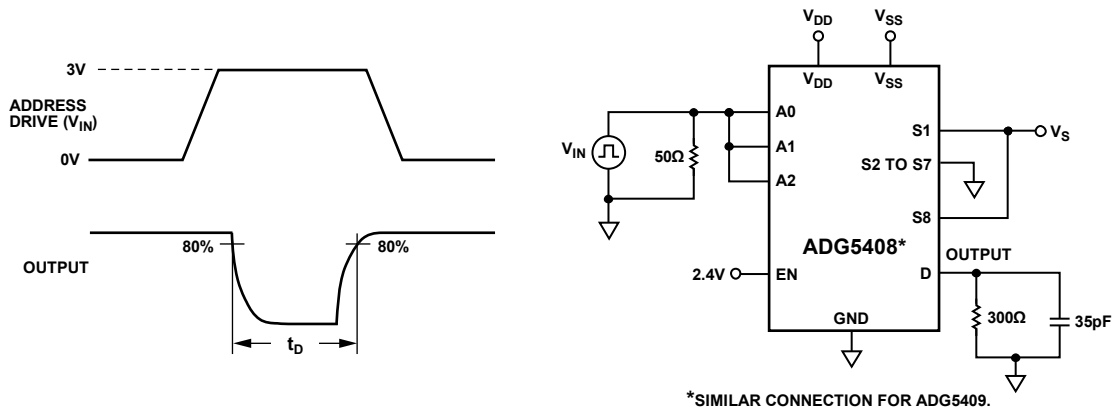


Figure 33. Break-Before-Make Delay, t_D

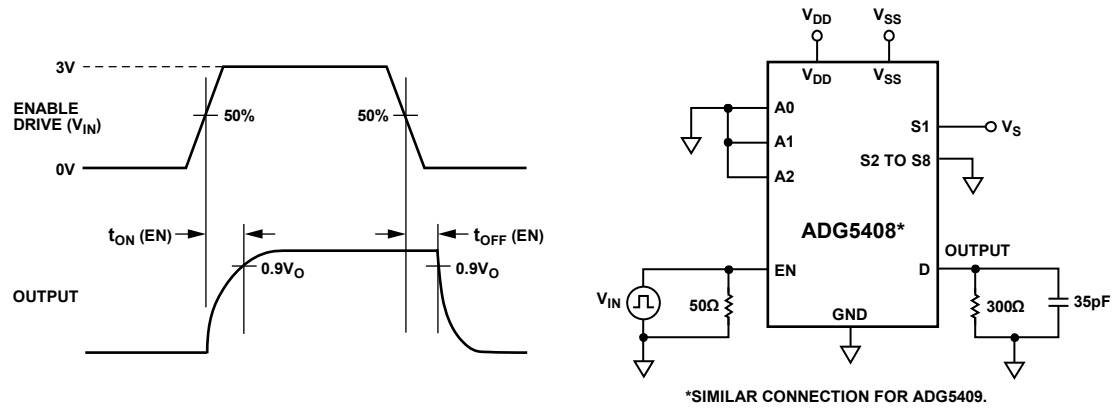


Figure 34. Enable Delay, $t_{ON}(EN)$, $t_{OFF}(EN)$

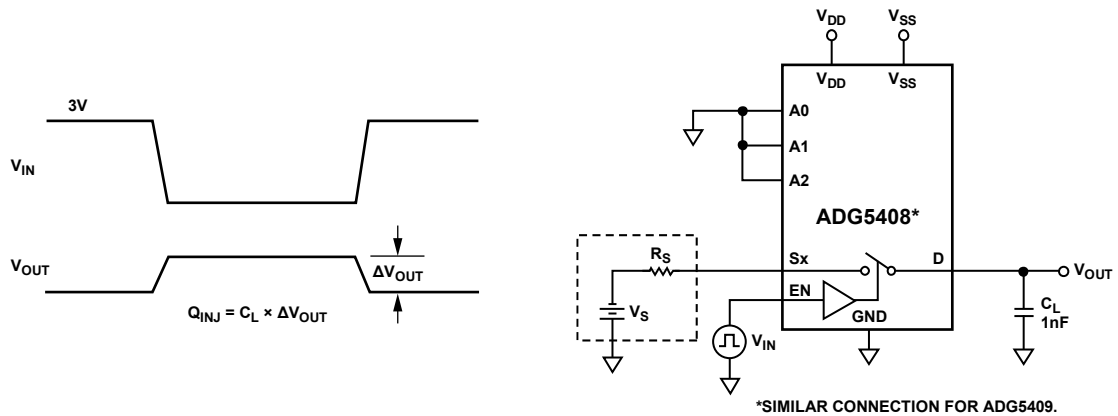


Figure 35. Charge Injection

TERMINOLOGY

I_{DD}

I_{DD} represents the positive supply current.

I_{SS}

I_{SS} represents the negative supply current.

V_D, V_S

V_D and V_S represent the analog voltage on Terminal D and Terminal S, respectively.

R_{ON}

R_{ON} is the ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}

ΔR_{ON} represents the difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$

The difference between the maximum and minimum value of on resistance as measured over the specified analog signal range is represented by $R_{FLAT(ON)}$.

I_S (Off)

I_S (Off) is the source leakage current with the switch off.

I_D (Off)

I_D (Off) is the drain leakage current with the switch off.

I_D (On), I_S (On)

I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}

V_{INL} is the maximum input voltage for Logic 0.

V_{INH}

V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}

I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)

C_D (Off) represents the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)

C_S (Off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)

C_D (On) and C_S (On) represent on switch capacitances, which are measured with reference to ground.

C_{IN}

C_{IN} represents digital input capacitance.

$t_{ON(EN)}$

$t_{ON(EN)}$ represents the delay time between the 50% and 90% points of the digital input and switch on condition.

$t_{OFF(EN)}$

$t_{OFF(EN)}$ represents the delay time between the 50% and 90% points of the digital input and switch off condition.

$t_{TRANSITION}$

Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_D

t_D represents the off time measured between the 80% point of both switches when switching from one address state to another.

Off Isolation

Off isolation is a measure of unwanted signal coupling through an off channel.

Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk

Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

Bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response

On response is the frequency response of the on switch.

Total Harmonic Distortion + Noise (THD + N)

The ratio of the harmonic amplitude plus noise of the signal to the fundamental is represented by THD + N.

AC Power Supply Rejection Ratio (ACPSRR)

ACPSRR is a measure of the ability of a part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR.

TRENCH ISOLATION

In the ADG5408/ADG5409, an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode can become forward-biased. A silicon controlled rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current that, in turn, leads to latch-up. With trench isolation, this diode is removed, and the result is a latch-up proof switch.

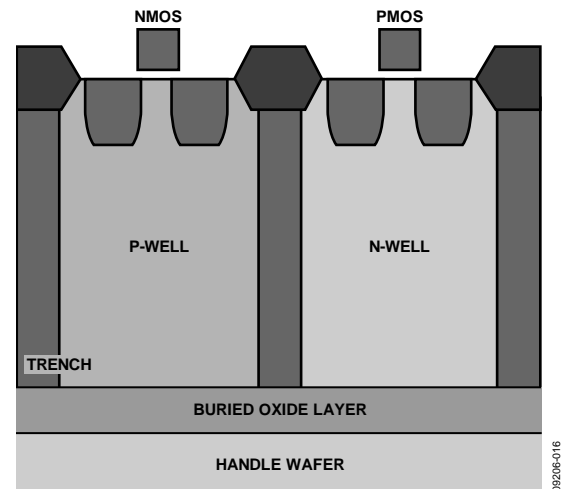


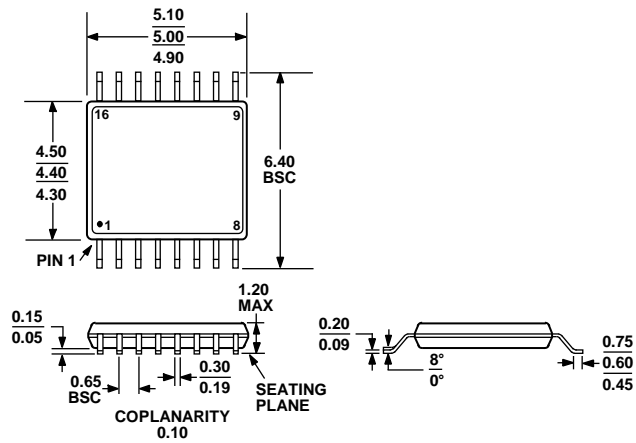
Figure 36. Trench Isolation

APPLICATIONS INFORMATION

The ADG54xx family switches and multiplexers provide a robust solution for instrumentation, industrial, aerospace, and other harsh environments that are prone to latch-up, which is an undesirable high current state that can lead to device failure and persist until the power supply is turned off. The ADG5408/ADG5409 high voltage switches allow single-supply operation

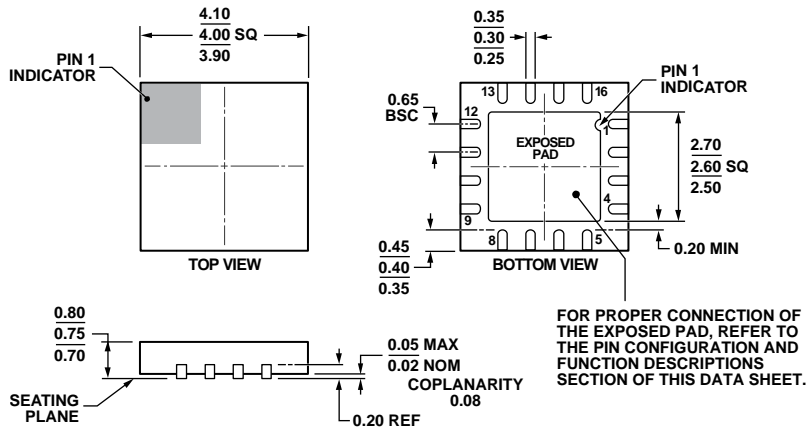
from 9 V to 40 V and dual-supply operation from ± 9 V to ± 22 V. The ADG5408/ADG5409 (as well as select devices within the same family) achieve an 8 kV human body model ESD rating that provides a robust solution eliminating the need for separate protect circuitry designs in some applications.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 37. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



FOR PROPER CONNECTION OF THE EXPOSED PAD, REFER TO THE PIN CONFIGURATION AND FUNCTION DESCRIPTIONS SECTION OF THIS DATA SHEET.

COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 38. 16-Lead Lead Frame Chip Scale Package [LFCSF_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-16-17)
Dimensions shown in millimeters

08-16-2010C

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADG5408BRUZ	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5408BRUZ-REEL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5408BCPZ-REEL7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-17
ADG5409BRUZ	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5409BRUZ-REEL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5409BCPZ-REEL7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-17

¹ Z = RoHS Compliant Part.

NOTES

NOTES