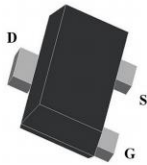


Features

- Lead free product is acquired
- Surface mount package
- P-Channel switch with low $R_{DS(on)}$
- Operated at low logic level gate drive
- ESD protected gate
- Complementary to PRZM002P02T2L Or TPM2030-3

Package and Pin Configuration

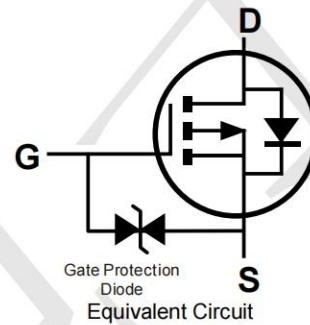


SOT723

Application

- Load/Power Switching
- Interfacing Switching
- Battery Management for Ultra Small Portable Electronics
- Logic Level Shift

Circuit diagram



Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

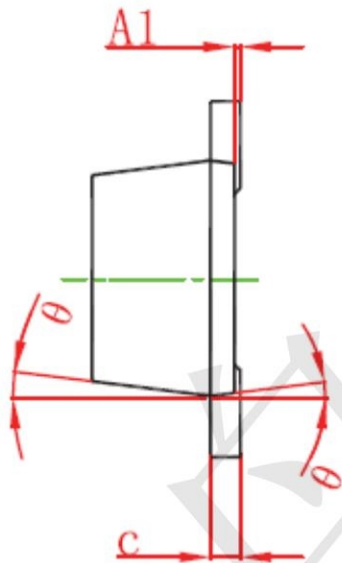
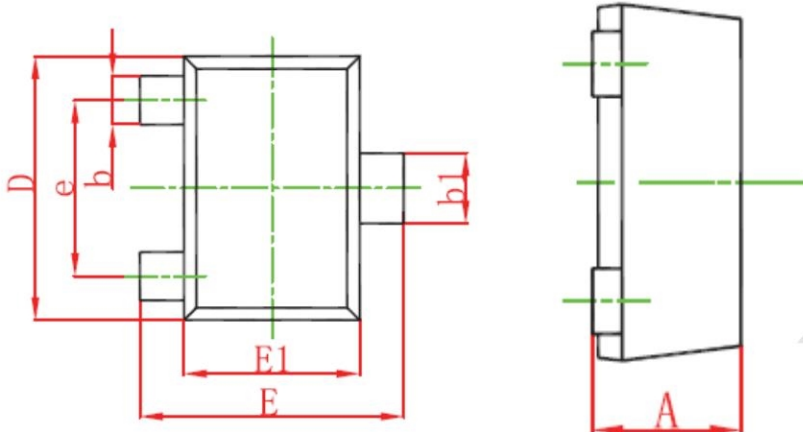
Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	-20	V
Typical gate-source voltage	V_{GS}	± 12	V
Continuous drain current (note 1)	I_D	-0.9	A
Pulsed drain current ($t_p=10\mu\text{s}$)	I_{DM}	-1.2	A
Power dissipation (note 2)	P_D	100	mW
Thermal resistance from junction to ambient (note 1)	$R_{\theta JA}$	1250	$^\circ\text{C/W}$
Junction temperature range	T_J	150	$^\circ\text{C}$
Storage temperature range	T_{STG}	-55 ~ +150	$^\circ\text{C}$
Lead temperature for soldering purposes (1/8" from case for 10s)	T_L	260	$^\circ\text{C}$

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
STATIC PARAMETERS						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-20			V
Zero gate voltage drain current	I_{DSS}	$V_{DS} = -20V, V_{GS} = 0V$			-1	μA
Gate-body leakage current	I_{GSS}	$V_{GS} = \pm 10V, V_{DS} = 0V$			± 20	μA
Gate threshold voltage (note 2)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.35		-1.1	V
Drain-source on-resistance (note 2)	$R_{DS(on)}$	$V_{GS} = -4.5V, I_D = -1A$			520	m Ω
		$V_{GS} = -2.5V, I_D = -0.8A$			700	
		$V_{GS} = -1.8V, I_D = -0.5A$		950		
Forward transconductance (note 2)	g_{FS}	$V_{DS} = -10V, I_D = -0.54A$		1.2		S
Diode forward voltage	V_{SD}	$I_S = -0.5A, V_{GS} = 0V$			-1.2	V
DYNAMIC PARAMETERS (note 4)						
Input capacitance	C_{iss}	$V_{DS} = -16V, V_{GS} = 0V, f = 1MHz$		113	170	pF
Output capacitance	C_{oss}		15	25		
Reverse transfer capacitance	C_{rss}		9	15		
SWITCHING PARAMETERS (note 4)						
Turn-on delay time (note 3)	$t_{d(on)}$	$V_{GS} = -4.5V, V_{DS} = -10V, I_D = -200mA, R_{GEN} = 10\Omega$		9		ns
Turn-on rise time (note 3)	t_r		5.8			
Turn-off delay time (note 3)	$t_{d(off)}$		32.7			
Turn-off fall time (note 3)	t_f		20.3			



SOT723-Package Outline Drawing



Symbol	DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.43	0.50	0.017	0.020
A1	0.00	0.05	0.000	0.002
b	0.17	0.27	0.007	0.011
b1	0.27	0.37	0.011	0.015
c	0.08	0.15	0.003	0.006
D	1.15	1.25	0.045	0.049
E	1.15	1.25	0.045	0.049
E1	0.75	0.85	0.03	0.033
e	0.8 typ		0.031 typ	
θ	7° REF		7° REF	

Suggested Land Pattern

