

# MSKSEMI

SEMICONDUCTOR



ESD



TVS



TSS



MOV



GDT



PLED

Product data sheet

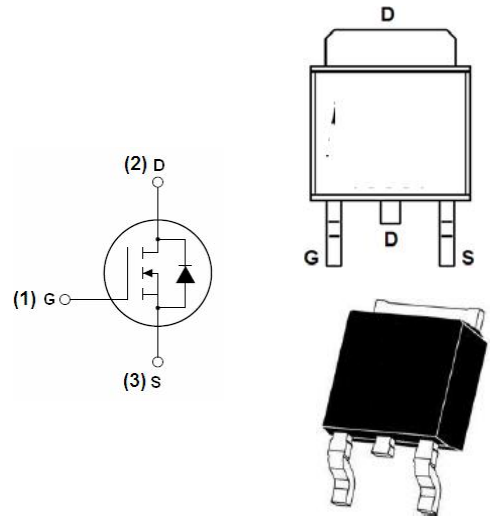
**FEATURE**

- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

**APPLICATION**

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

**Schematic diagram**



TO-252

**Maximum ratings ( $T_a=25^{\circ}\text{C}$  unless otherwise noted)**

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current	$I_D$	50	A
Pulsed Drain Current	$I_{DM}$	220	
Single Pulsed Avalanche Energy*	$E_{AS}$	115	mJ
Power Dissipation	$P_D$	1.25	W
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	100	$^{\circ}\text{C}/\text{W}$
Junction Temperature	$T_J$	150	$^{\circ}\text{C}$
Storage Temperature	$T_{stg}$	-50 ~ +150	

\* $E_{AS}$  condition:  $T_J=25^{\circ}\text{C}$ ,  $V_{DD}=50\text{V}$ ,  $L=0.5\text{mH}$ ,  $R_G=25\Omega$ , Starting  $T_J = 25^{\circ}\text{C}$

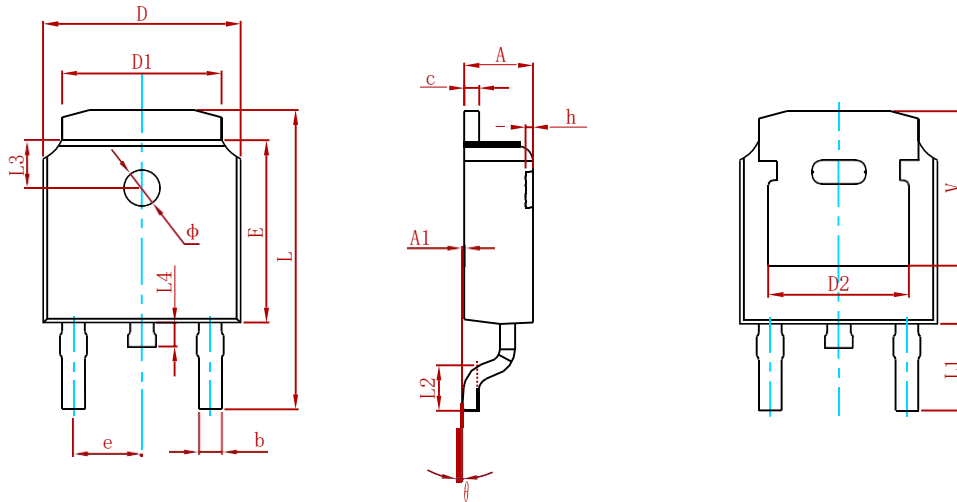
**Electrical characteristics (T<sub>a</sub>=25°C unless otherwise noted)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Off characteristics</b>						
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	60			V
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0V			1	μA
Gate-body leakage current	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V			±100	nA
<b>On characteristics (note1)</b>						
Gate-threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1.5		2.5	V
Static drain-source on-resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 20A		11.5	15	mΩ
Forward transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 25V, I <sub>D</sub> = 20A	24			S
<b>Dynamic characteristics (note 2)</b>						
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1MHz		900		pF
Output capacitance	C <sub>oss</sub>			104		
Reverse transfer capacitance	C <sub>rss</sub>			33		
<b>Switching characteristics (note 2)</b>						
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = 30V, V <sub>GS</sub> = 10V, I <sub>D</sub> = 50A		30		nC
Gate-source charge	Q <sub>gs</sub>			10		
Gate-drain charge	Q <sub>gd</sub>			5		
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 30V, I <sub>D</sub> = 2A, V <sub>GS</sub> = 10V, R <sub>G</sub> = 2.5Ω, R <sub>L</sub> = 15Ω		25		ns
Turn-on rise time	t <sub>r</sub>			5		
Turn-off delay time	t <sub>d(off)</sub>			50		
Turn-off fall time	t <sub>f</sub>			6		
<b>Drain-Source Diode Characteristics</b>						
Drain-source diode forward voltage(note1)	V <sub>SD</sub>	V <sub>GS</sub> = 0V, I <sub>S</sub> = 40A			1.2	V
Continuous drain-source diode forward current	I <sub>S</sub>				50	A
Pulsed drain-source diode forward current	I <sub>SM</sub>				220	A

**Notes:**

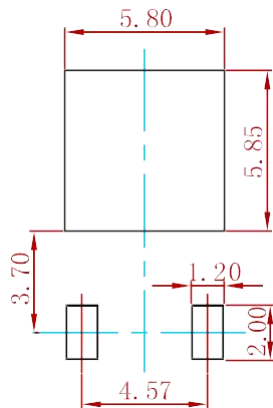
- Pulse Test : Pulse Width ≤ 300μs, duty cycle ≤ 2%.
- Guaranteed by design, not subject to production.

**PACKAGE MECHANICAL DATA**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.635	0.770	0.025	0.030
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.712	10.312	0.382	0.406
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.250 REF.		0.207 REF.	

**Suggested Pad Layout**



Note:  
 1. Controlling dimension: in millimeters.  
 2. General tolerance: ± 0.05mm.  
 3. The pad layout is for reference purposes only.

**REEL SPECIFICATION**

P/N	PKG	QTY
MS50N06	TO-252	2500

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