

# MSKSEMI

SEMICONDUCTOR



ESD



TVS



TSS



MOV



GDT



PLED

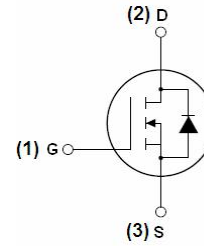
Product data sheet

**General Features**

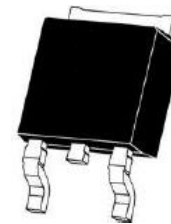
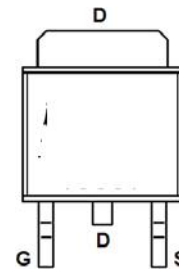
- $V_{DS} = 20V, I_D = 60A$   
 $R_{DS(ON)} < 6m\Omega @ V_{GS} = 4.5V$
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation

**Application**

- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic diagram



TO-252

**Absolute Maximum Ratings ( $T_C = 25^\circ C$  unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Drain Current-Continuous	$I_D$	60	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D (100^\circ C)$	42	A
Pulsed Drain Current	$I_{DM}$	210	A
Maximum Power Dissipation	$P_D$	60	W
Derating factor		0.48	W/ $^\circ C$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	200	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$

**Thermal Characteristic**

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	2.1	°C/W
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**Electrical Characteristics ( $T_c=25^{\circ}\text{C}$  unless otherwise noted)**

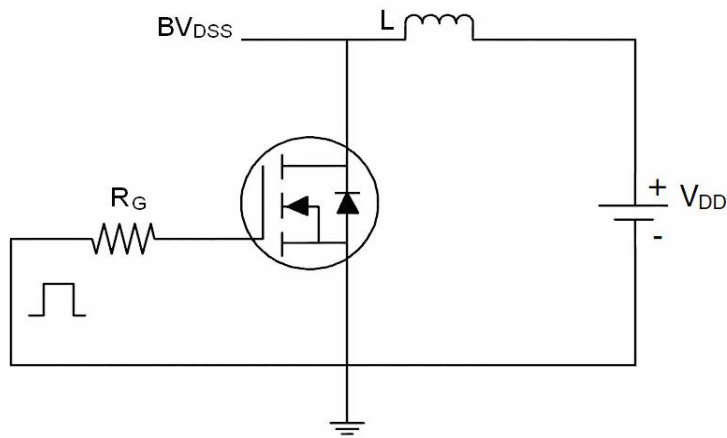
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	20	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=20V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <sup>(Note 3)</sup>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	0.75	1.0	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=20 A$	-	4.8	6	m $\Omega$
		$V_{GS}=2.5V, I_D=15A$		6.2	9	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=10V, I_D=20A$	15	-	-	S
<b>Dynamic Characteristics</b> <sup>(Note4)</sup>						
Input Capacitance	$C_{iss}$	$V_{DS}=10V, V_{GS}=0V,$ $F=1.0MHz$	-	2000	-	PF
Output Capacitance	$C_{oss}$		-	500	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	200	-	PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=10V, I_D=2A, R_L=1\Omega$ $V_{GS}=4.5V, R_G=3\Omega$	-	6.4	-	nS
Turn-on Rise Time	$t_r$		-	17.2	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	29.6	-	nS
Turn-Off Fall Time	$t_f$		-	16.8	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=10V, I_D=20A,$ $V_{GS}=10V$	-	27		nC
Gate-Source Charge	$Q_{gs}$		-	6.5		nC
Gate-Drain Charge	$Q_{gd}$		-	6.4		nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	$V_{SD}$	$V_{GS}=0V, I_S=10A$	-		1.2	V
Diode Forward Current <sup>(Note 2)</sup>	$I_S$		-	-	60	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^{\circ}\text{C}, I_F = 20A$ $di/dt = 100A/\mu s$ <sup>(Note3)</sup>	-	25	-	nS
Reverse Recovery Charge	$Q_{rr}$		-	24	-	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

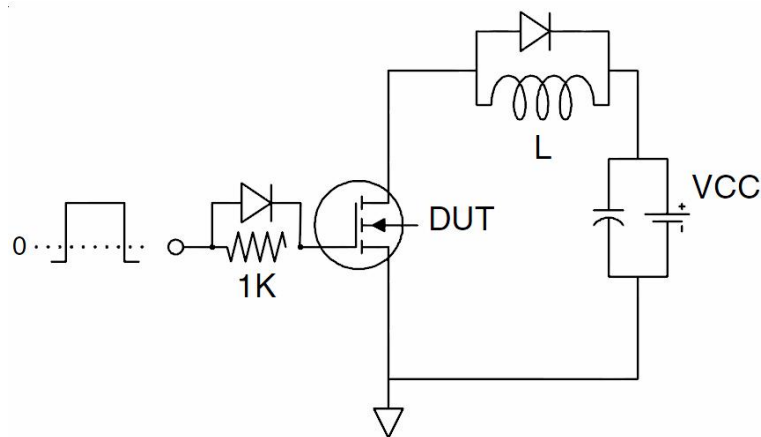
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5.  $E_{AS}$  condition :  $T_J=25^{\circ}\text{C}, V_{DD}=10V, V_G=10V, L=0.5mH, R_g=25\Omega,$

**Test circuit**

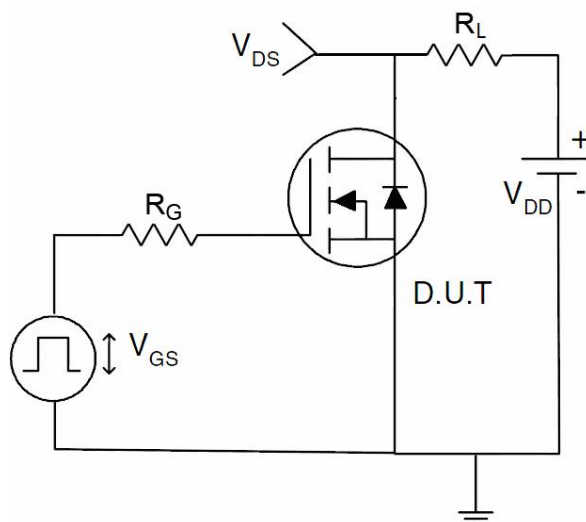
**1) E<sub>AS</sub> Test Circuit**



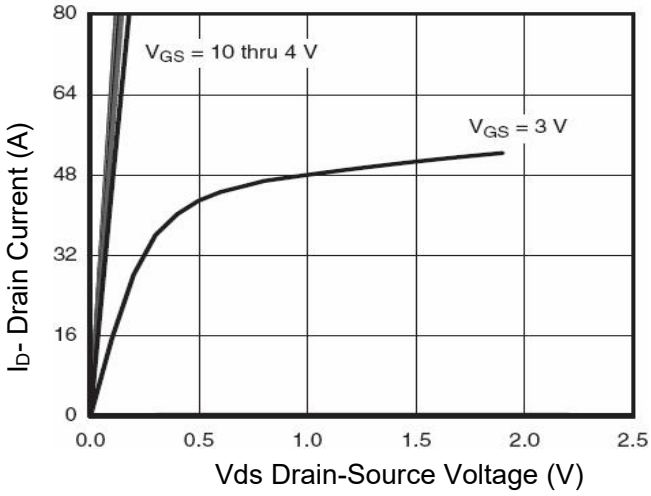
**2) Gate Charge Test Circuit**



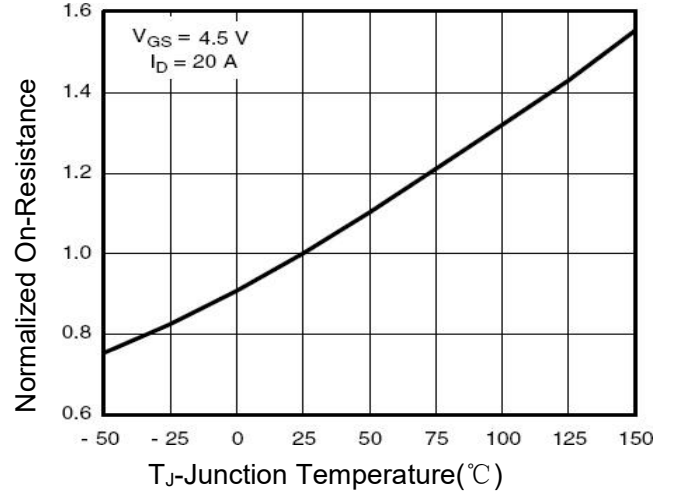
**3) Switch Time Test Circuit**



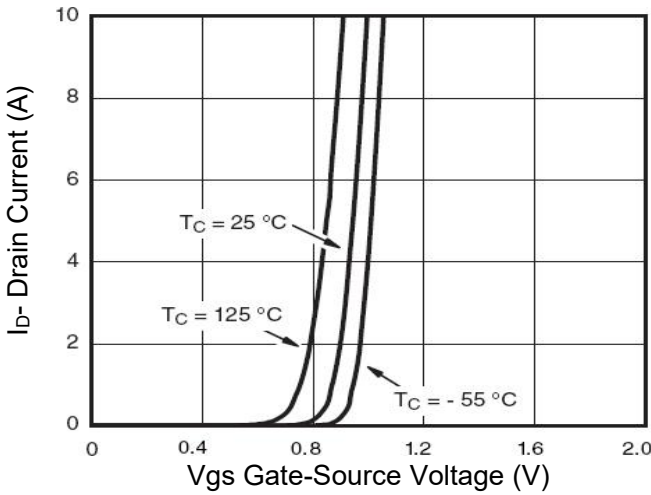
**Typical Electrical and Thermal Characteristics (Curves)**



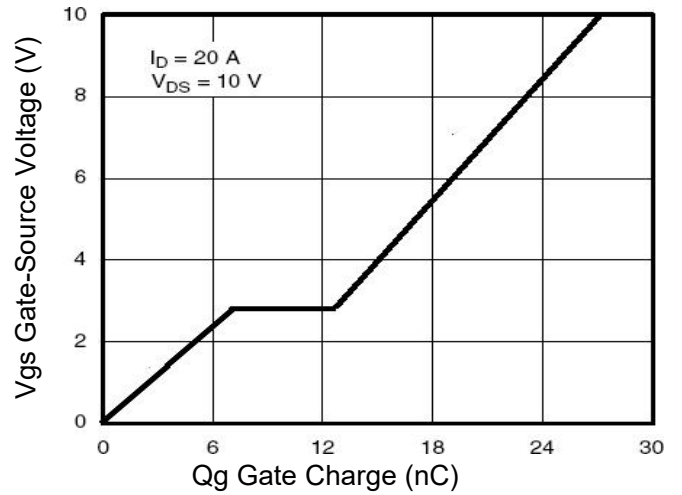
**Figure 1 Output Characteristics**



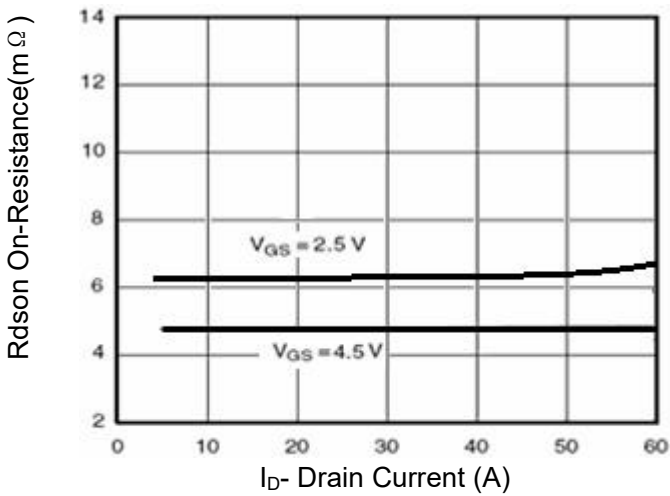
**Figure 4  $R_{dson}$ -Junction Temperature**



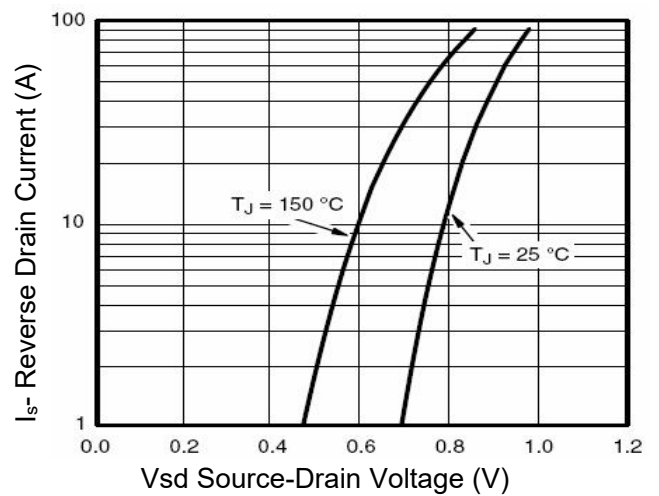
**Figure 2 Transfer Characteristics**



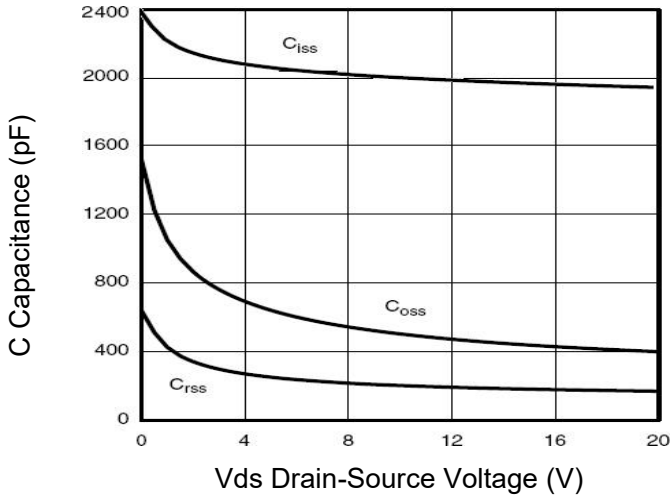
**Figure 5 Gate Charge**



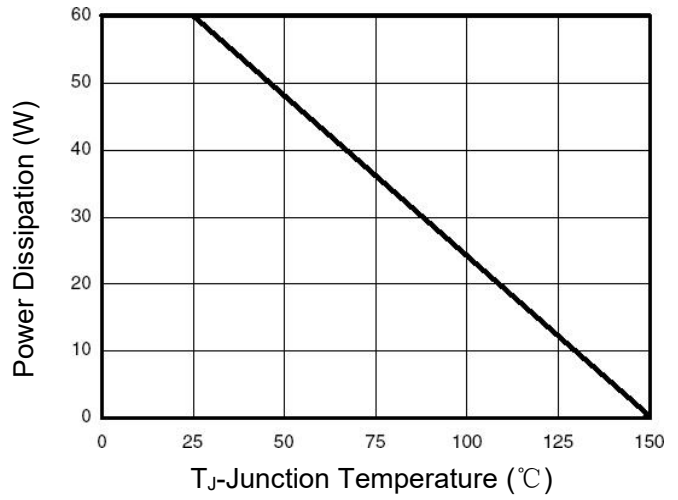
**Figure 3  $R_{dson}$ - Drain Current**



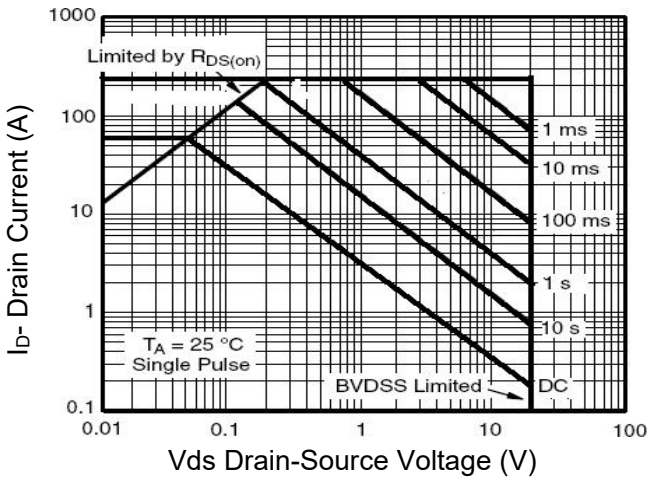
**Figure 6 Source- Drain Diode Forward**



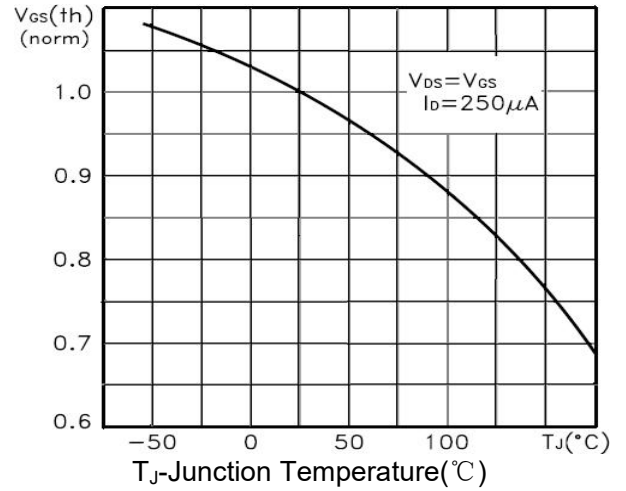
**Figure 7 Capacitance vs Vds**



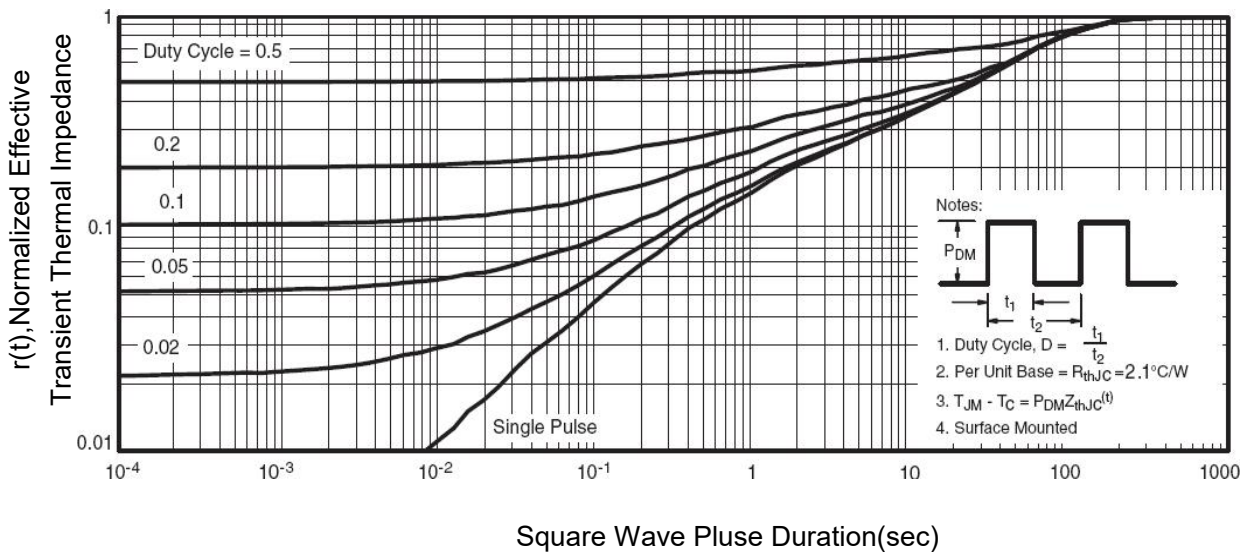
**Figure 9 Power De-rating**



**Figure 8 Safe Operation Area**

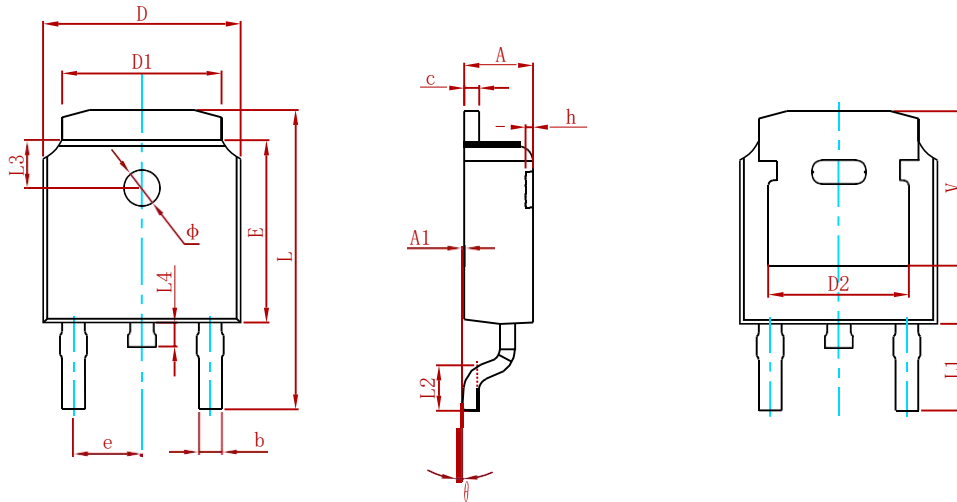


**Figure 10 VGS(th) vs Junction Temperature**



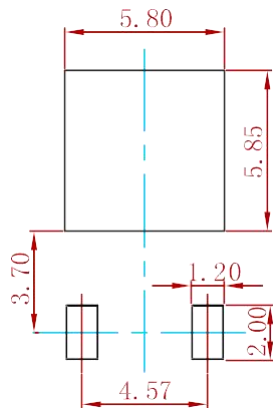
**Figure 11 Normalized Maximum Transient Thermal Impedance**

**PACKAGE MECHANICAL DATA**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.635	0.770	0.025	0.030
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.712	10.312	0.382	0.406
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.250 REF.		0.207 REF.	

**Suggested Pad Layout**



Note:  
 1. Controlling dimension: in millimeters.  
 2. General tolerance: ± 0.05mm.  
 3. The pad layout is for reference purposes only.

**REEL SPECIFICATION**

P/N	PKG	QTY
MS50N02	TO-252	2500

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