

# MOSFET - N-Channel Shielded Gate PowerTrench®

150 V, 7.3 mΩ, 101 A

## NTP7D3N15MC

### Features

- Shielded Gate MOSFET Technology
- Max  $R_{DS(on)} = 7.3 \text{ m}\Omega$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 62 \text{ A}$
- 50% Lower  $Q_{rr}$  than other MOSFET Suppliers
- Lowers Switching Noise/EMI
- 100% UIL Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	150	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	$I_D$	101	A
Power Dissipation $R_{\theta JC}$ (Note 2)			
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	$I_D$	12.1	A
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)			
Pulsed Drain Current	$I_{DM}$	574	A
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy ( $I_L = 20 \text{ A}_{pk}$ , $L = 3 \text{ mH}$ )	$E_{AS}$	600	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

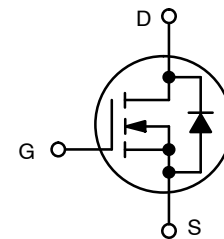
1. Surface-mounted on FR4 board using a 1 in<sup>2</sup>, 2 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.



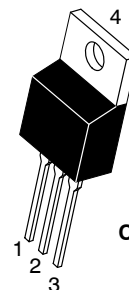
ON Semiconductor®

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$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
150 V	7.3 mΩ @ 10 V	101 A

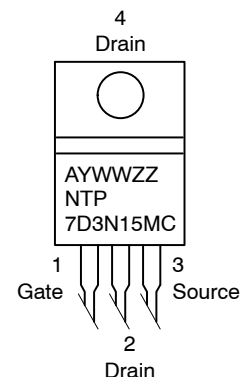


N-CHANNEL MOSFET



TO-220  
CASE 221A

### MARKING DIAGRAM



NTP7D3N15MC = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ZZ = Lot Traceability

### ORDERING INFORMATION

Device	Package	Shipping†
NTP7D3N15MC	TO-220 (Pb-Free)	800 / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTP7D3N15MC

## Thermal Resistance Maximum Ratings

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	0.9	°C/W
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	62.5	

## Electrical Characteristics (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	150			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\ \mu\text{A}, \text{ref to } 25^\circ\text{C}$		71		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 120\text{ V}$ $T_J = 25^\circ\text{C}$			1.0	μA
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			±100	nA

### ON CHARACTERISTICS

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 342\ \mu\text{A}$	2.5		4.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 342\ \mu\text{A}, \text{ref to } 25^\circ\text{C}$		-7.3		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 62\text{ A}$		6.2	7.3	mΩ
		$V_{GS} = 8\text{ V}, I_D = 31\text{ A}$		6.6	8.4	
Forward Transconductance	$g_{FS}$	$V_{DS} = 10\text{ V}, I_D = 62\text{ A}$		119		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 75\text{ V}$		4250		pF
Output Capacitance	$C_{OSS}$			1250		
Reverse Transfer Capacitance	$C_{RSS}$			15		
Gate-Resistance	$R_G$			0.8	1.6	Ω
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 75\text{ V}; I_D = 62\text{ A}$		53		nC
Threshold Gate Charge	$Q_{G(TH)}$			14		
Gate-to-Source Charge	$Q_{GS}$			23		
Gate-to-Drain Charge	$Q_{GD}$			8.5		
Plateau Voltage	$V_{GP}$			5.8		
Output Charge	$Q_{OSS}$	$V_{DD} = 75\text{ V}, V_{GS} = 0\text{ V}$		133		nC

### SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DD} = 75\text{ V}, I_D = 62\text{ A}, R_G = 4.7\ \Omega$		27		ns
Rise Time	$t_r$			8.5		
Turn-Off Delay Time	$t_{d(OFF)}$			33		
Fall Time	$t_f$			5.8		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 62\text{ A}$	$T_J = 25^\circ\text{C}$		0.93	1.2	V
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, V_{DD} = 75\text{ V}$ $di_S/dt = 300\text{ A}/\mu\text{s}, I_S = 62\text{ A}$			55		ns
Reverse Recovery Charge	$Q_{RR}$				247		nC
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, V_{DD} = 75\text{ V}$ $di_S/dt = 1000\text{ A}/\mu\text{s}, I_S = 62\text{ A}$			50		ns
Reverse Recovery Charge	$Q_{RR}$				720		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

# NTP7D3N15MC

## TYPICAL CHARACTERISTICS

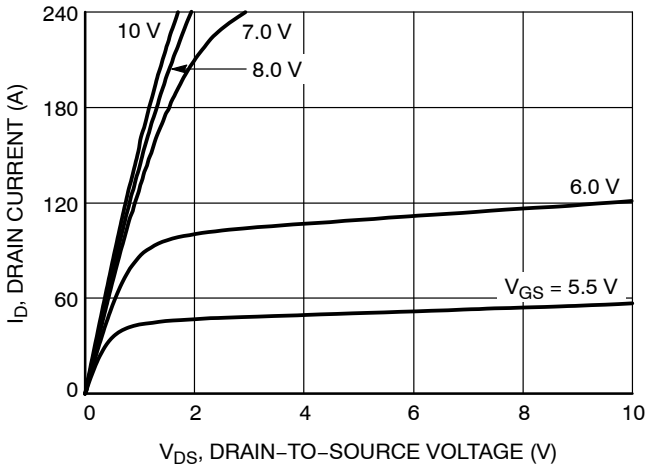


Figure 1. On-Region Characteristics

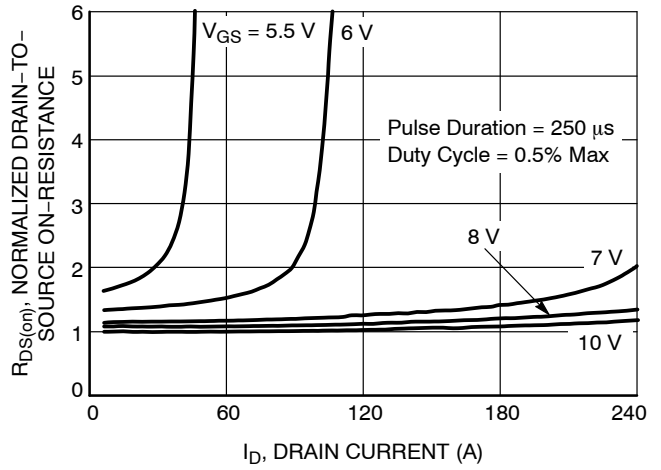


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

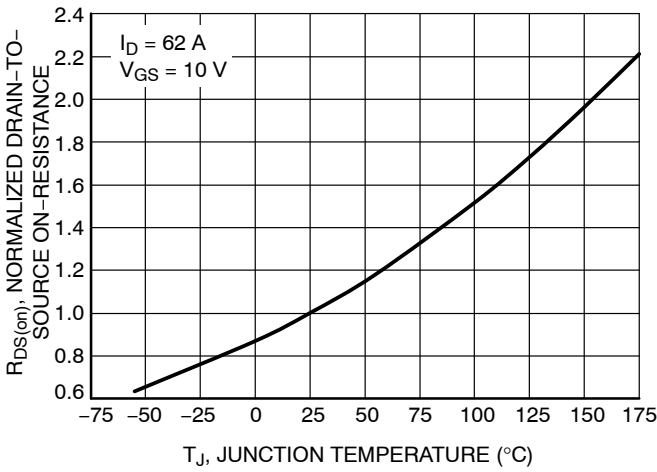


Figure 3. Normalized On-Resistance vs. Junction Temperature

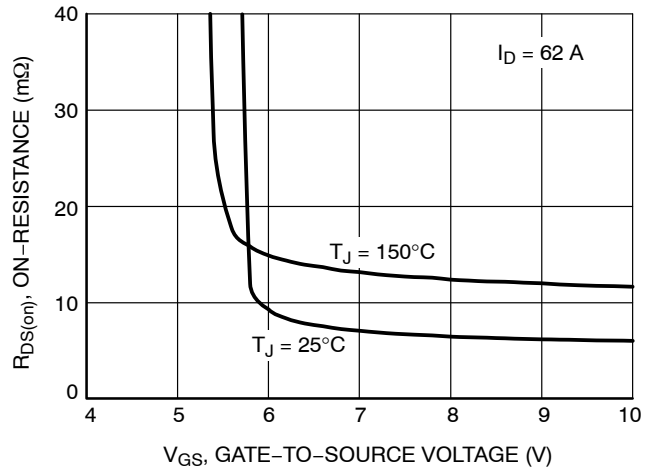


Figure 4. On-Resistance vs. Gate-to-Source Voltage

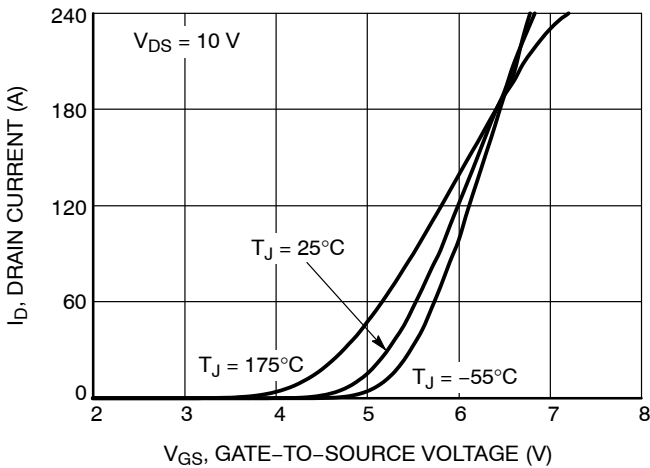


Figure 5. Transfer Characteristics

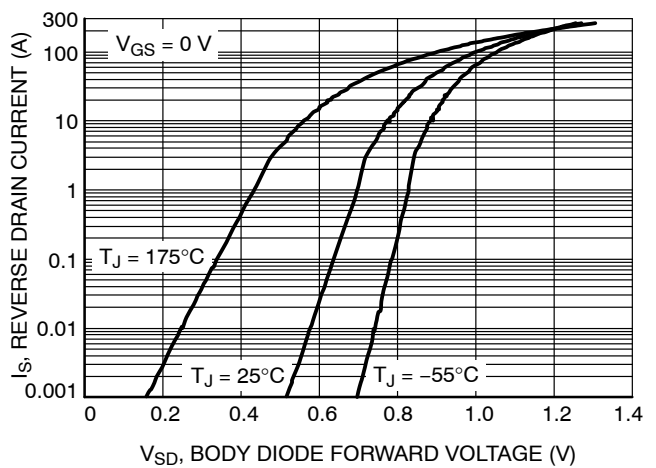


Figure 6. Source-to-Drain Diode Forward Voltage vs. Source Current

# NTP7D3N15MC

## TYPICAL CHARACTERISTICS

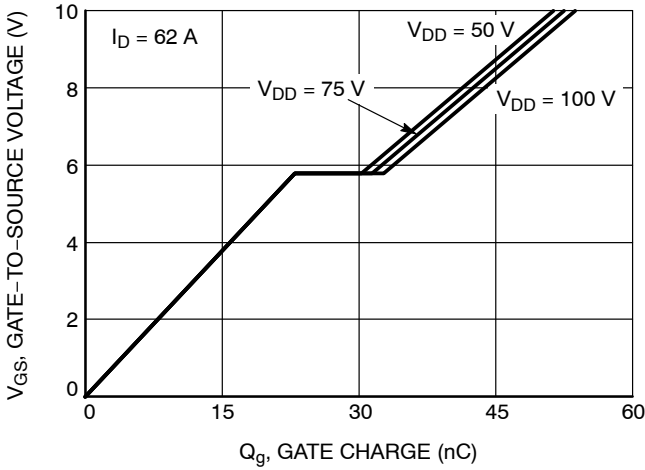


Figure 7. Gate Charge Characteristics

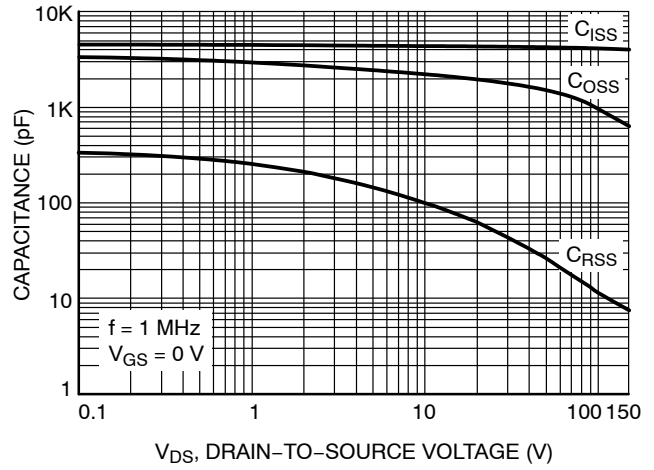


Figure 8. Capacitance vs. Drain-to-Source Voltage

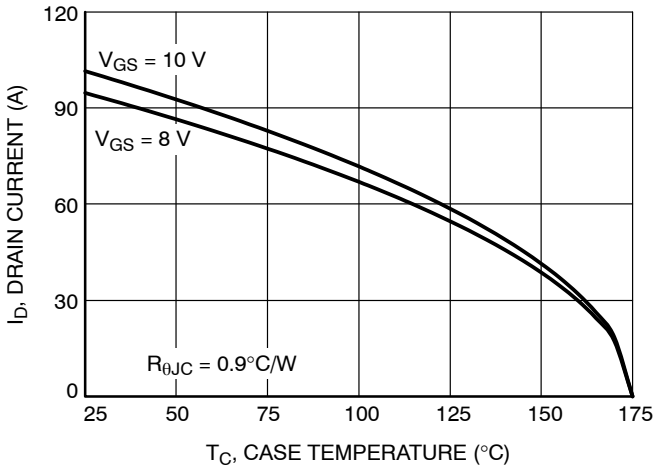


Figure 9. Drain Current vs. Case Temperature

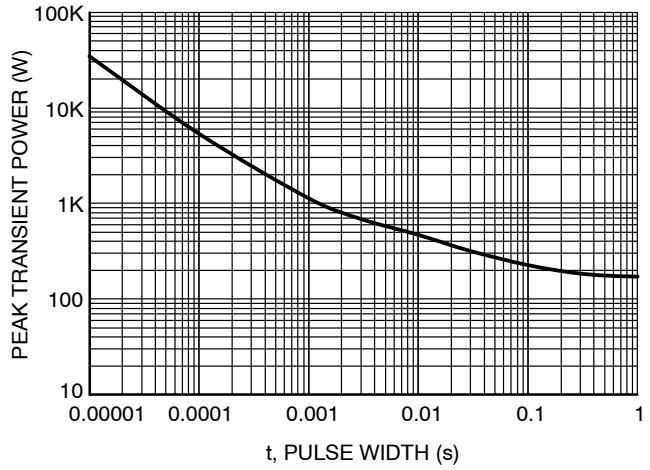


Figure 10. Peak Power

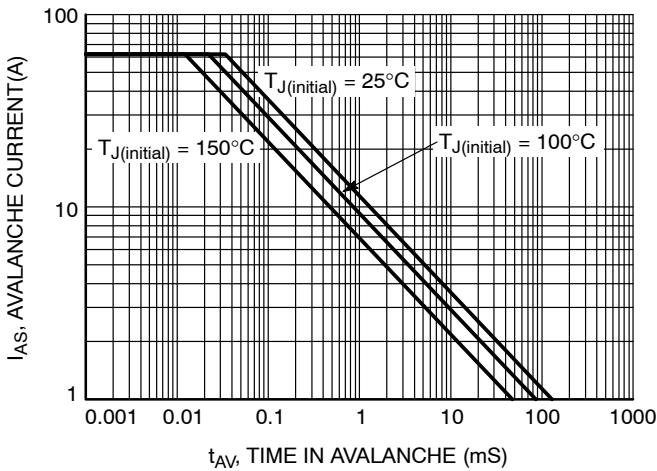


Figure 11. Unclamped Inductive Switching Capability

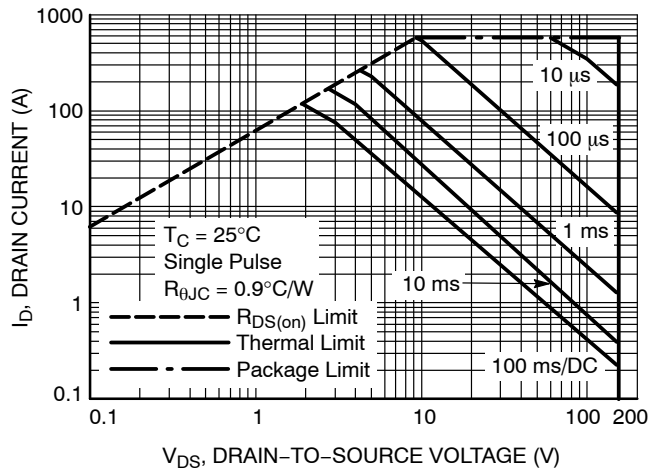


Figure 12. Forward Bias Safe Operating Area

# NTP7D3N15MC

## TYPICAL CHARACTERISTICS

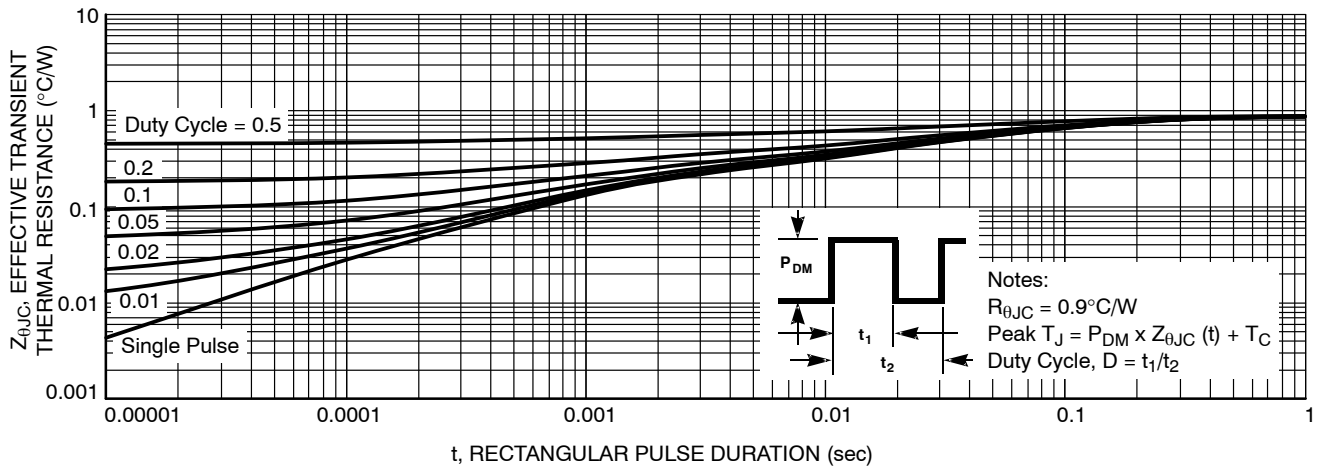


Figure 13. Transient Thermal Impedance

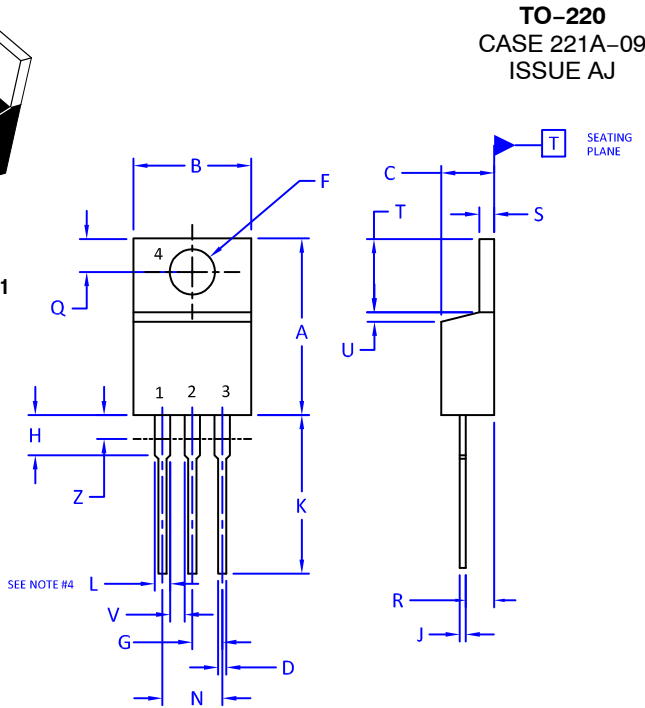
# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1



**TO-220**  
CASE 221A-09  
ISSUE AJ

DATE 05 NOV 2019

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

**STYLE 1:**

- PIN 1. BASE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

**STYLE 2:**

- PIN 1. BASE
- 2. EMITTER
- 3. COLLECTOR
- 4. EMITTER

**STYLE 3:**

- PIN 1. CATHODE
- 2. ANODE
- 3. GATE
- 4. ANODE

**STYLE 4:**

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. MAIN TERMINAL 2

**STYLE 5:**

- PIN 1. GATE
- 2. DRAIN
- 3. SOURCE
- 4. DRAIN

**STYLE 6:**

- PIN 1. ANODE
- 2. CATHODE
- 3. ANODE
- 4. CATHODE

**STYLE 7:**

- PIN 1. CATHODE
- 2. ANODE
- 3. CATHODE
- 4. ANODE

**STYLE 8:**

- PIN 1. CATHODE
- 2. ANODE
- 3. EXTERNAL TRIP/DELAY
- 4. ANODE

**STYLE 9:**

- PIN 1. GATE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

**STYLE 10:**

- PIN 1. GATE
- 2. SOURCE
- 3. DRAIN
- 4. SOURCE

**STYLE 11:**

- PIN 1. DRAIN
- 2. SOURCE
- 3. GATE
- 4. SOURCE

**STYLE 12:**

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. NOT CONNECTED

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