+12 Volt Electronic Fuse

NIS5420 Series

The NIS5420 eFuse is a cost effective, resettable fuse which can greatly enhance the reliability of a hard drive or other circuit from both catastrophic and shutdown failures.

It is designed to buffer the load device from excessive input voltage which can damage sensitive circuits. It also includes an overvoltage clamp circuit that limits the output voltage during transients but does not shut the unit down, thereby allowing the load circuit to continue operation.

Features

- Integrated Power Device
- Power Device Thermally Protected
- No External Current Shunt Required
- 8 V to 18 V Input Range
- 39 mΩ Typical
- Internal Charge Pump
- Internal Undervoltage Lockout Circuit
- Internal Overvoltage Clamp
- ESD Ratings: Human Body Model (HBM); 2000 V
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Hard Drives
- Mother Board Power Management
- Fan Drives

ON Semiconductor®

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4.6 AMP, 12 VOLT ELECTRONIC FUSE

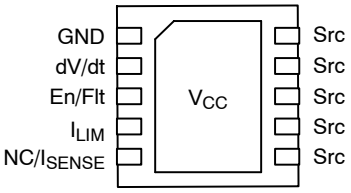
MARKING DIAGRAM

WDFN10
CASE 522AA

XXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



WDFN10
(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the ordering information section on page 11 of this data sheet.

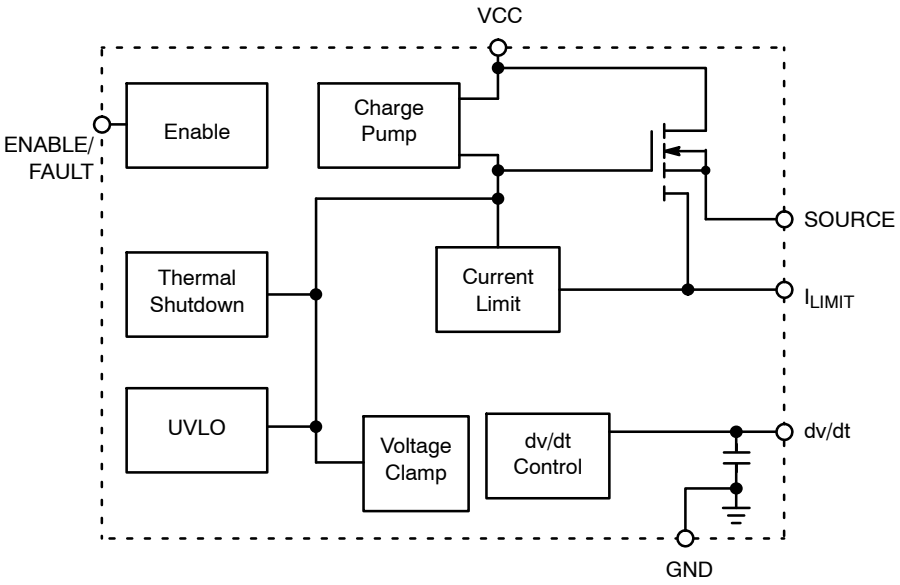


Figure 1. Block Diagram
(NIS5420MT3, NIS5420MT4, NIS5420MT5)

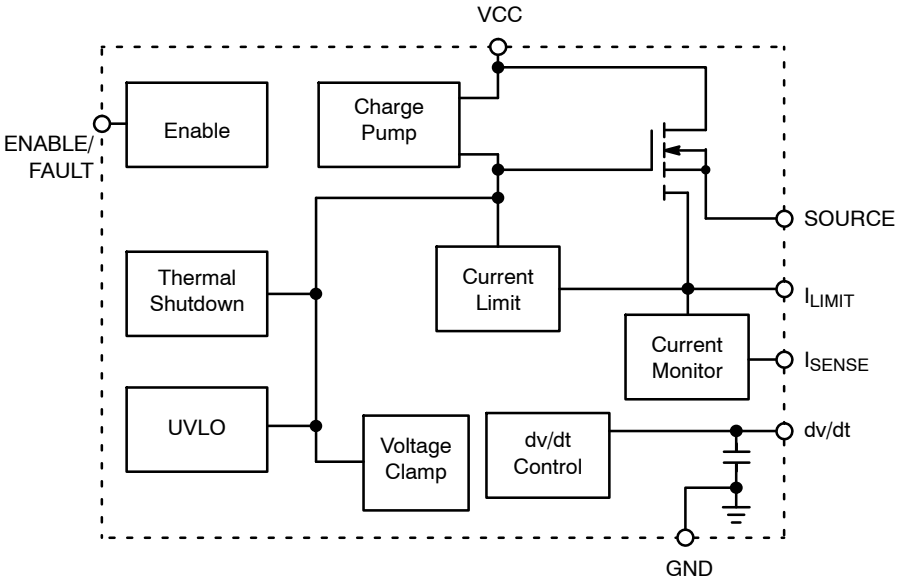


Figure 2. Block Diagram
(NIS5420MT1, NIS5420MT2, NIS5420MT6, NIS5420MT7, NIS5420MT8

Table 1. FUNCTIONAL PIN DESCRIPTION

Pin	Function	Description
1	Ground	Negative input voltage to the device. This is used as the internal reference for the IC.
2	dv/dt	The internal dv/dt circuit controls the slew rate of the output voltage at turn on. It has an internal capacitor that allows it to ramp up over a period of 2 ms. An external capacitor can be added to this pin to increase the ramp time. If an additional time delay is not required, this pin should be left open.
3	Enable/Fault	The enable/fault pin is a tri−state, bidirectional interface. It can be pulled to ground with external open−drain or open collector device to shutdown the eFuse. It can also be used as a status indicator; if the voltage level is intermediate around 1.4 V − the eFuse is in the thermal shutdown, if the voltage level is high around 3 V − the eFuse is operating normally. Do not actively drive this pin to any voltage. Do not connect a capacitor to this pin.
4	I_{Limit}	A resistor between this pin and the source pin sets the overload and short circuit current limit levels.
5	NC	For NIS5420MT3, NIS5420MT4 and NIS5420MT5
	I_{SENSE}	For NIS5420MT1, NIS5420MT2, NIS5420MT6, NIS5420MT7 and NIS5420MT8 load current monitor allows the system to monitor the load current in real time. Connect R_{SENSE} to GND.
6−10	Source	This pin is the source of the internal power FET and the output terminal of the fuse.
11 (belly pad)	V_{CC}	Positive input voltage to the device.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage, operating, steady−state (V_{CC} to GND, Note 1) Transient (100 ms)	V_{IN}	−0.6 to 18 −0.6 to 25	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Negative voltage will not damage device provided that the power dissipation is limited to the rated allowable power for the package.

Table 2. THERMAL RATINGS

Rating	Symbol	Value	Unit
Thermal Resistance, Junction−to−Air (4 layer High−K JEDEC JESD51−7 PCB, 100 mm^2, 2 oz. Cu)	θ_{JA}	90	°C/W
Thermal Characterization Parameter, Junction−to−Lead (4 layer High−K JEDEC JESD51−7 PCB, 100 mm^2, 2 oz. Cu)	Ψ_{J-L}	27.5	°C/W
Thermal Characterization Parameter, Junction−to−Board (4 layer High−K JEDEC JESD51−7 PCB, 100 mm^2, 2 oz. Cu)	Ψ_{J-B}	27.5	°C/W
Thermal Characterization Parameter, Junction−to−Case Top (4 layer High−K JEDEC JESD51−7 PCB, 100 mm^2, 2 oz. Cu)	Ψ_{J-T}	7.6	°C/W
Total Power Dissipation @ T_A = 25°C (4 layer High−K JEDEC JESD51−7 PCB, 100 mm^2, 2 oz. Cu) Derate above 25°C	P_{max}	1.39 11.1	W mW/°C
Operating Ambient Temperature Range	T_A	−40 to 125	°C
Operating Junction Temperature Range	T_J	−40 to 150	°C
Non−operating Temperature Range	T_{STG}	−55 to 155	°C
Lead Temperature, Soldering (10 Sec)	T_L	260	°C

Table 3. ELECTRICAL CHARACTERISTICS
(V_{CC} = 12 V, C_L = 100 μF, dv/dt pin open, R_{LIMIT} = 20 Ω, T_j = 25°C unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
POWER FET					
Delay Time (enabling of chip to I_D = 100 mA with 1 A resistive load)	T_{dly}	–	220	–	μs
Kelvin ON Resistance (Note 2) T_J = 140°C (Note 3)	R_{DSon}	30 –	39 60	50 –	mΩ
Off State Output Voltage (V_{CC} = 18 V_{dc}, V_{GS} = 0 V_{dc}, R_L = ∞)	V_{off}	–	–	50	mV
Continuous Current (T_A = 25°C, 100 mm^2 copper) (Note 3) (T_A = 80°C, minimum copper)	I_D I_D	– –	– –	4.6 3.5	A
THERMAL LATCH					
Shutdown Temperature (Note 3)	T_{SD}	150	175	200	°C
Thermal Hysteresis (Auto−retry part only)	T_{Hyst}	–	45	–	°C
Thermal Shutdown Response Time	T_{SDRes}	10	15	20	μs
UNDER/OVERVOLTAGE PROTECTION					
Output Clamping Voltage (NIS5420MT2, NIS5420MT7)	V_{Clamp1}	12.5	–	14.5	V
Output Clamping Voltage (NIS5420MT1, NIS5420MT4, NIS5420MT5, NIS5420MT6)	V_{Clamp2}	13.6	–	16	V
Output Clamping Response Time	T_{Clamp_Res}	–	–	10	μs
Undervoltage Lockout (NIS5420MT1, NIS5420MT3, NIS5420MT4, NIS5420MT5, NIS5420MT6)	V_{UVLO1}	7.8	8.5	9.2	V
Undervoltage Lockout (NIS5420MT2, NIS5420MT6, NIS5420MT8)	V_{UVLO2}	6	6.5	7	V
UVLO Hysteresis	V_{Hyst}	–	0.80	–	V
CURRENT LIMIT					
Kelvin Short Circuit Current Limit (R_{Limit} = 20 Ω, Note 4)	I_{Lim-SS}	1.76	2.1	2.64	A
Kelvin Overload Current Limit (R_{Limit} = 20 Ω, Note 4)	I_{Lim-OL}	–	4.2	–	A
dv/dt CIRCUIT					
Output Voltage Ramp Time (Enable to V_{OUT} = 11.7 V and 10% to 90% − V_{OUT} = 1.2 V to 10.8 V with 12Ω Load)	t_{slew}	–	2.0	–	ms
Maximum Capacitor Voltage	V_{max}	–	–	V_{CC}	V
ENABLE/FAULT					
Logic Level Low (Output Disabled)	V_{in-low}	0.35	0.58	0.81	V
Logic Level Mid (Thermal Fault, Output Disabled)	V_{in-mid}	0.82	1.4	1.95	V
Logic Level High (Output Enabled)	$V_{in-high}$	1.96	2.6	3.0	V
High State Maximum Voltage	V_{in-max}	2.51	4.6	5	V
Logic Low Sink Current (V_{enable} = 0 V)	I_{in-low}	–	−15	−25	μA
Logic High Leakage Current for External Switch (V_{enable} = 3.3 V)	$I_{in-leak}$	–	–	1.0	μA
Maximum Fanout for Fault Signal (Total number of chips that can be connected to this pin for simultaneous shutdown)	Fan	–	–	3.0	Units
TOTAL DEVICE					
Bias Current (Operational)	I_{Bias}	–	–	450	μA
Bias Current (Shutdown)	I_{Bias}	–	–	150	μA
Minimum Operating Voltage (Notes 3 and 5)	V_{min}	–	–	7.7	V
LOAD CURRENT MONITOR					
Current Monitor Sense (R_{SENSE} = 1 kΩ)	I_{SENSE}	–	1	–	mA/A
Current Monitor Sense Accuracy	I_{ACC}	−10	–	10	%

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse test: Pulse width 300 μs, duty cycle 2%.
3. Verified by design.
4. Refer to explanation of short circuit and overload conditions in application note AND9441.
5. Device will shut down prior to reaching this level based on actual UVLO trip point.
6. For output slew rate calculation with external capacitor, please refer to ”Output Slew Rate (dv/dt)” in the ”Application Information ” section

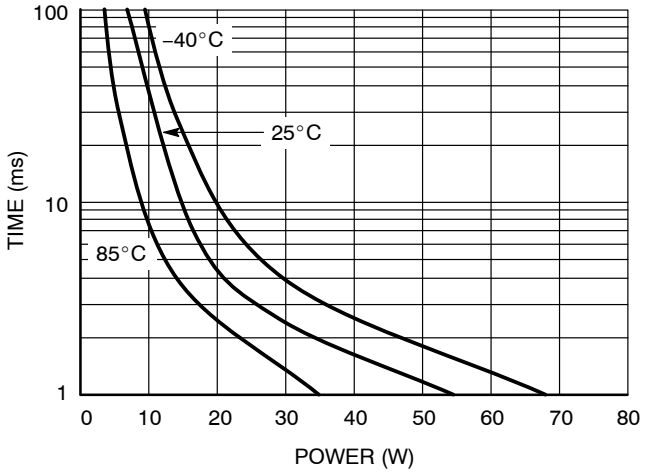


Figure 3. Thermal Trip Time vs. Power Dissipation

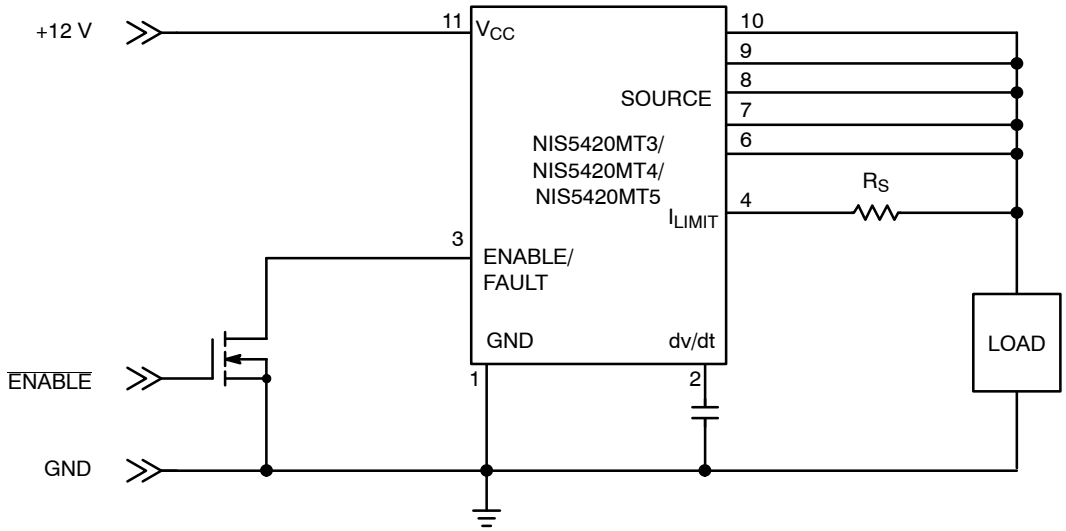


Figure 4. Application Circuit with Direct Current Sensing

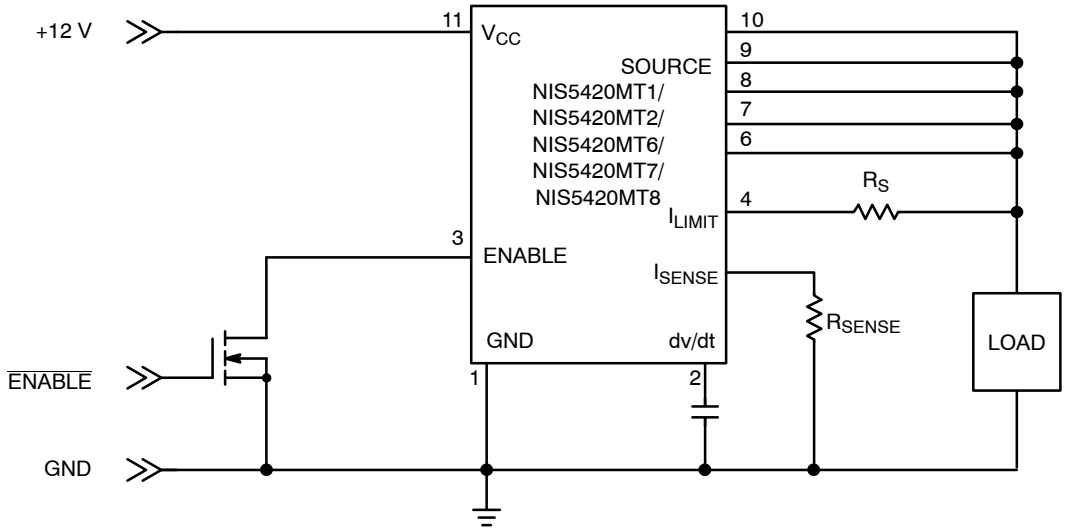


Figure 5. Application Circuit with Direct Current Sensing

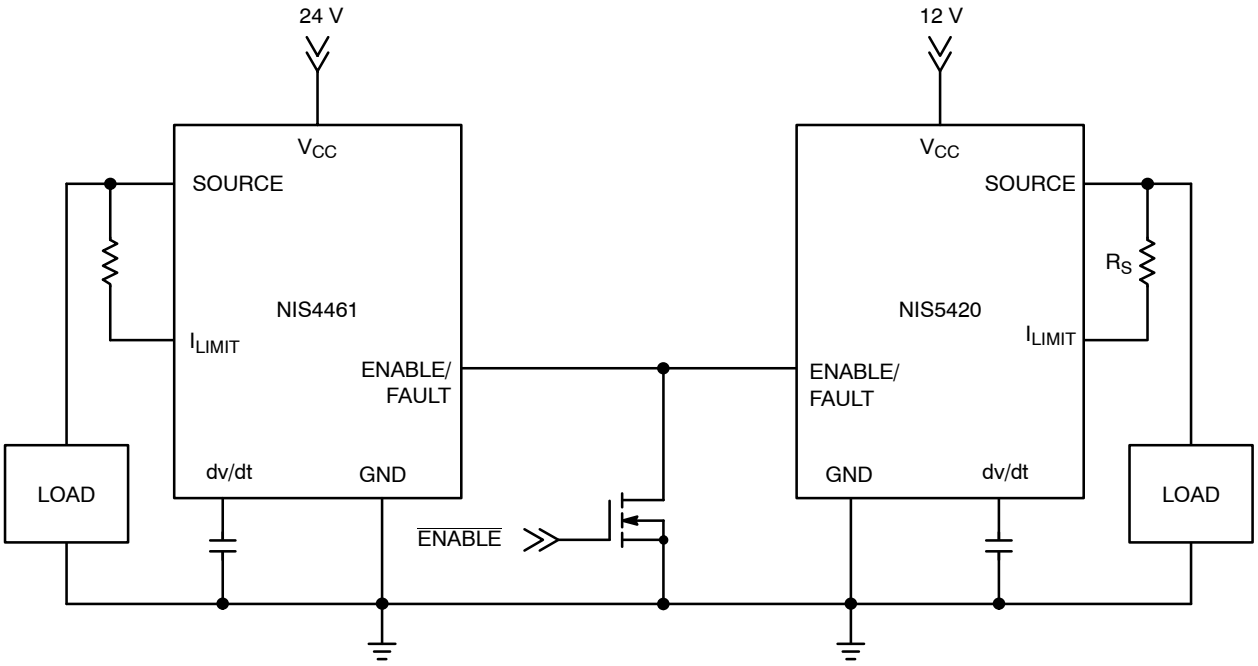


Figure 6. Common Thermal Shutdown

TYPICAL CHARACTERISTICS

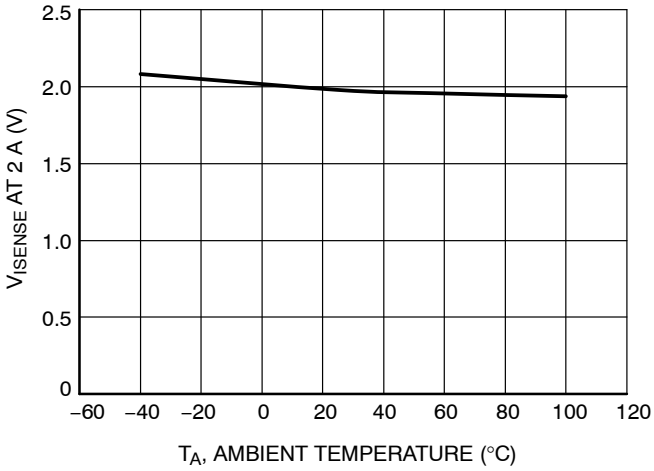


Figure 7. V_{ISENSE} vs. Ambient Temperature

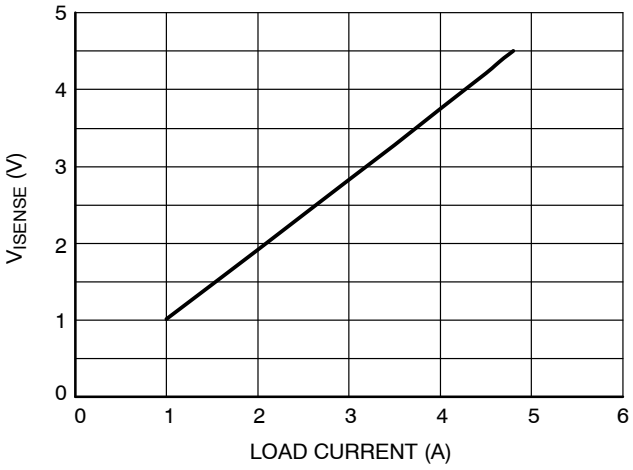


Figure 8. V_{ISENSE} vs. Load Current

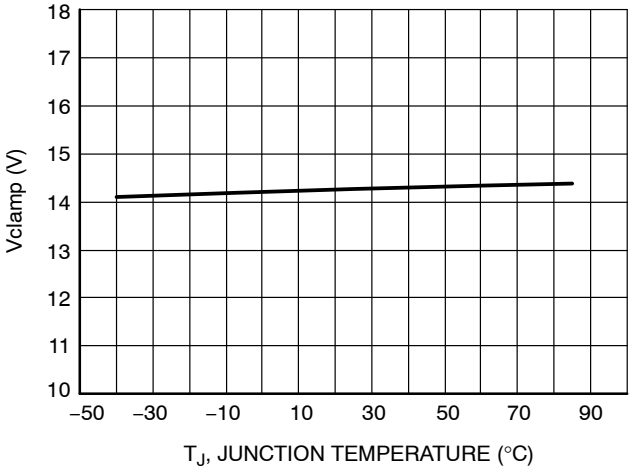


Figure 9. Vclamp vs. Junction Temperature

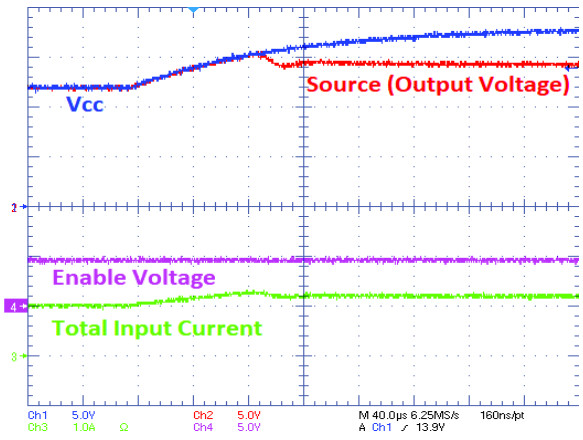


Figure 10. Vclamp Test

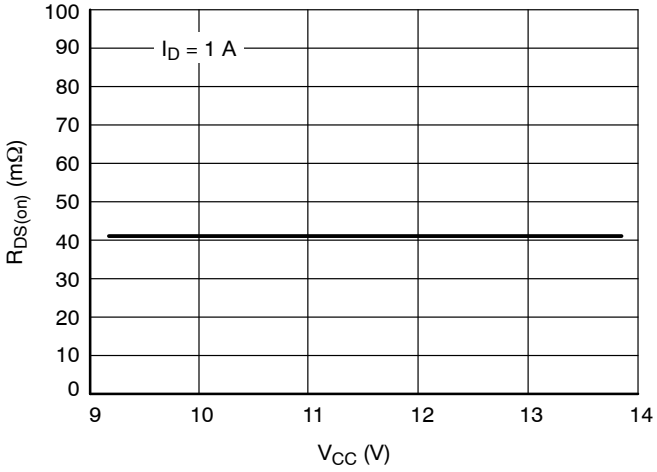


Figure 11. $R_{DS(on)}$ vs. V_{CC}

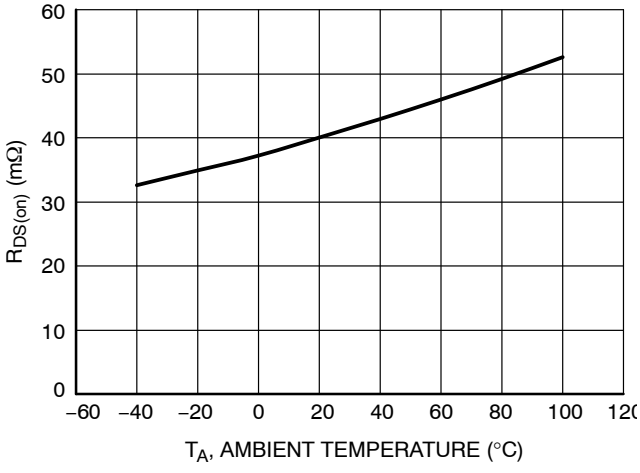


Figure 12. $R_{DS(on)}$ vs. Ambient Temperature

TYPICAL CHARACTERISTICS

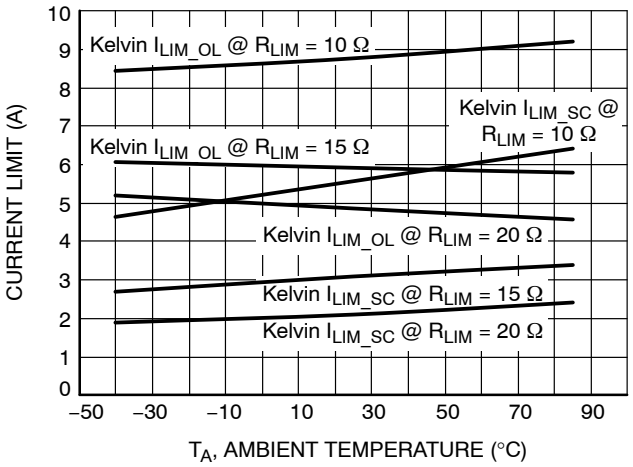


Figure 13. I_{LIM} vs. R_{LIM} over Ambient Temperature

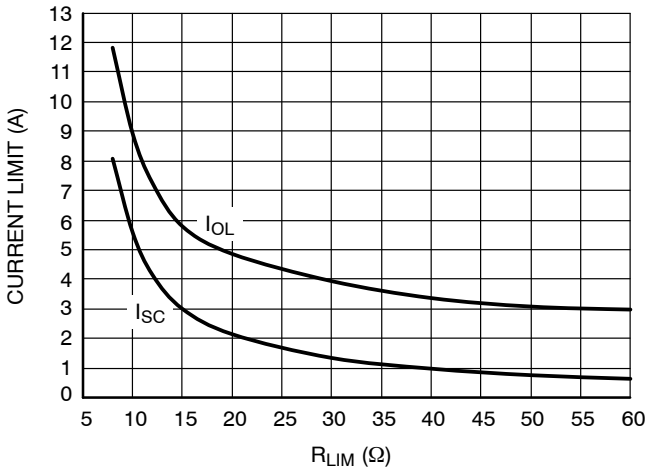


Figure 14. I_{LIM} vs. R_{LIM}

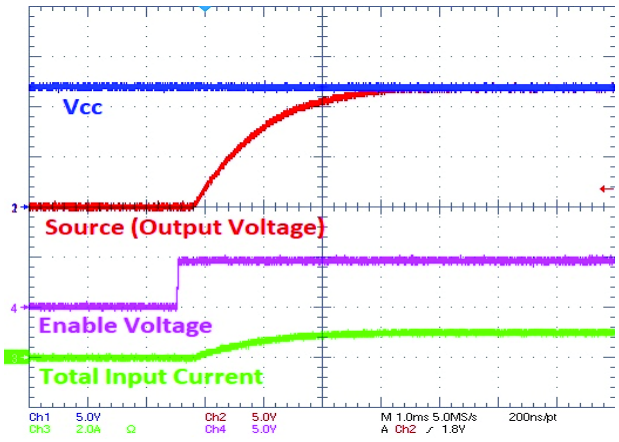


Figure 15. Slew Rate Control

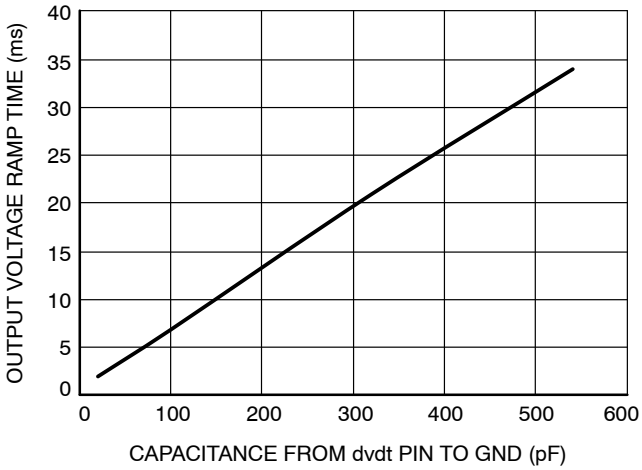


Figure 16. Tslew vs. dvdt Capacitance

APPLICATION INFORMATION

Basic Operation

This device is a self−protected, resettable, electronic fuse. It contains circuits to monitor the input voltage, output voltage, output current and die temperature.

On application of the input voltage, the device will apply the input voltage to the load based on the restrictions of the controlling circuits. The dv/dt of the output voltage will be controlled by the internal dv/dt circuit. The output voltage will slew from 0 V to the rated output voltage in 1.4 ms, unless additional capacitance is added to the dv/dt pin.

The device will remain on as long as the temperature does not exceed the 175°C limit that is programmed into the chip. The current limit circuit does not shut down the part but will reduce the conductivity of the FET to maintain a constant current at the internally set current limit level. The input overvoltage clamp also does not shutdown the part, but will limit the output voltage to 13.5/15 V in the event that the input exceeds that level.

An internal charge pump provides bias for the gate voltage of the internal n−channel power FET and also for the current limit circuit. The remainder of the control circuitry operates between the input voltage (V_{CC}) and ground.

Current Limit

The current limit circuit uses a SENSEFET along with a reference and amplifier to control the peak current in the device. The SENSEFET allows for a small fraction of the load current to be measured, which has the advantage of reducing the losses in the sense resistor as well as increasing the value and decreasing the power rating of the sense resistor. Sense resistors are typically in the tens of ohms range with power ratings of several milliwatts making them very inexpensive chip resistors.

The current limit circuit has two limiting values, one for short circuit events which are defined as the mode of operation in which the gate is high and the FET is fully enhanced. The overload mode of operation occurs when the device is actively limiting the current and the gate is at an intermediate level. For a more detailed description of this circuit please refer to application note AND9441.

There are two methods of biasing the current limit circuit for this device. They are shown in the two application figures. Direct current sensing connects the sense resistor between the current limit pin and the load. This method includes the bond wire resistance in the current limit circuit. This resistance has an impact on the current limit levels for a given resistor and may vary slightly depending on the impedance between the sense resistor and the source pins. The on resistance of the device will be slightly lower in this configuration since all five source pins are connected in parallel and therefore, the effective bond wire resistance is one fifth of the resistance for any given pin.

The other method is Kelvin sensing. This method uses one of the source pins as the connection for the current sense resistor. This connection senses the voltage on the die and therefore any bond wire resistance and external impedance on the board have no effect on the current limit levels. In this configuration the on resistance is slightly increased relative to the direct sense method since only four of the source pins are used for power.

Overvoltage Clamp

The overvoltage clamp consists of an amplifier and reference. It monitors the output voltage and if the input voltage exceeds the overvoltage value, the gate drive of the main FET is reduced to limit the output. This is intended to allow operation through transients while protecting the load. If an overvoltage condition exists for many seconds, the device may overheat due to the voltage drop across the FET combined with the load current. In this event, the thermal protection circuit would shut down the device.

Undervoltage Lockout

The undervoltage lockout circuit uses a comparator with hysteresis to monitor the input voltage. If the input voltage drops below the specified level, the output switch will be switched to a high impedance state.

Output Slew Rate dv/dt

The dv/dt circuit brings the output voltage up under a linear, controlled rate regardless of the load impedance characteristics. An internal ramp generator creates a linear ramp, and a control circuit forces the output voltage to follow that ramp, scaled by a factor.

The default ramp time is approximately 2 ms. This can be modified by adding an external capacitor at the dv/dt pin. Since the current level is very low, it is important to use a ceramic cap or other low leakage capacitor. Aluminum electrolytic capacitors are not recommended for this circuit.

The ramp time from 0 to the nominal output voltage can be determined by the following equation, where t is in seconds:

$$t_{1.2-10.8} = 6E7 \cdot (20\ pF + C_{ext}) + 0.0008$$

$$C_{ext} = \frac{t_{1.2-10.8} - 0.0008}{6E7} - 20\ pF$$

Where:
C is in Farads
t is in seconds

Any time that the unit shuts down due to a fault, enable shut−down, or recycling of input power, the timing capacitor will be discharged and the output voltage will ramp from 0 at turn on.

Enable/Fault

The Enable/Fault pin is a multi−function, bidirectional pin that can control the output of the chip as well as send information to other devices regarding the state of the chip. When this pin is low, the output of the fuse will be turned off. When this pin is high the output of the fuse will be

turned−on. If a thermal fault occurs, this pin will be pulled low to an intermediate level by an internal circuit.

To use as a simple enable pin, an open drain or open collector device should be connected to this pin. Due to its tri−state operation, it should not be connected to any type of logic with an internal pullup device.

If the chip shuts down due to the die temperature reaching its thermal limit, this pin will be pulled down to an intermediate level. This signal can be monitored by an external circuit to communicate that a thermal shutdown has occurred. If this pin is tied to another device in this family, a thermal shutdown of one device will cause both devices to disable their outputs. Both devices will turn on once the fault is removed for the auto−retry devices.

For the latching thermal device, the outputs will be enabled after the enable pin has been pulled to ground with an external switch and then allowed to go high or after the input power has been recycled. For the auto retry devices, both devices will restart as soon as the die temperature of the device in shutdown has been reduced to the lower thermal limit.

Thermal Protection

The NIS542x includes an internal temperature sensing circuit that senses the temperature on the die of the power FET. If the temperature reaches 175°C, the device will shut down, and remove power from the load. Output power can be restored by either recycling the input power or toggling the enable pin for thermally latching devices. Power will automatically be reapplied to the load for auto−retry devices once the die temperature has been reduced by 45°C.

The thermal limit has been set high intentionally, to increase the trip time during high power transient events. It is not recommended to operate this device above 150°C for extended periods of time.

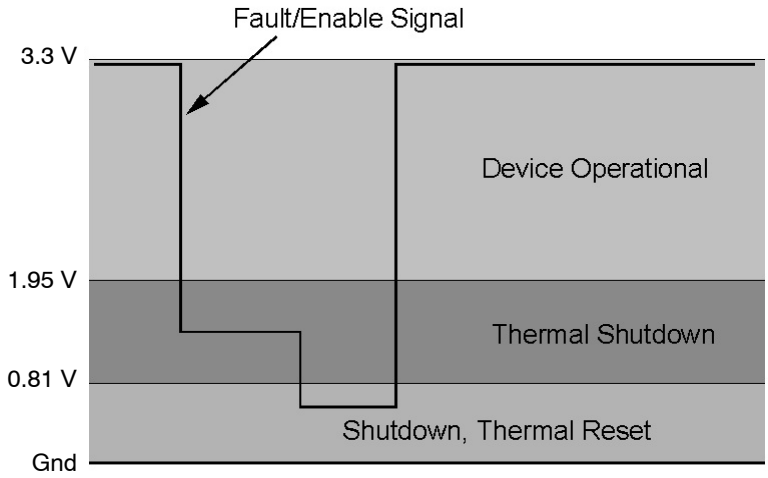


Figure 17. Fault/Enable Signal Levels

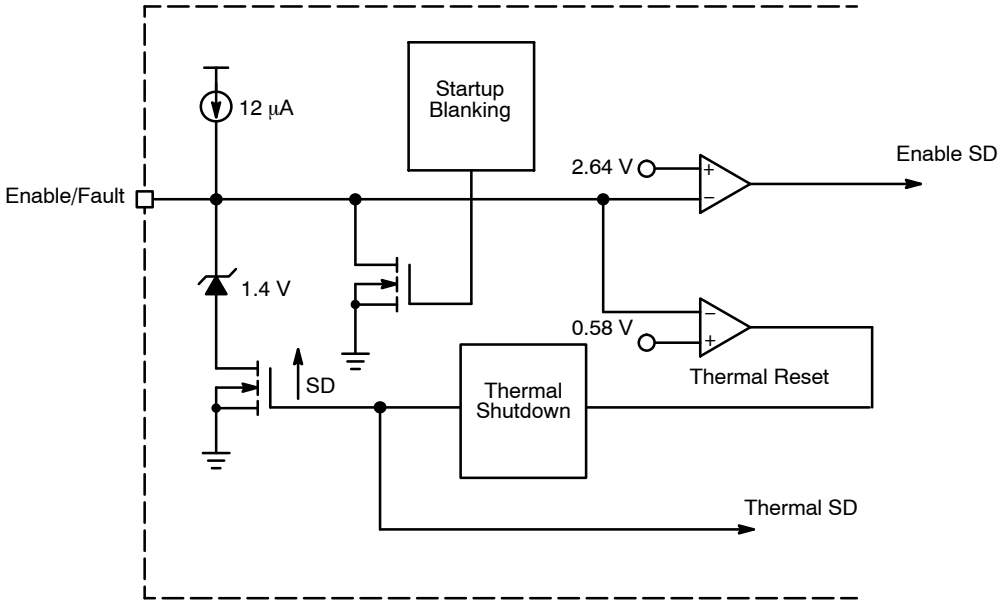


Figure 18. Enable/Fault Simplified Circuit

ORDERING INFORMATION

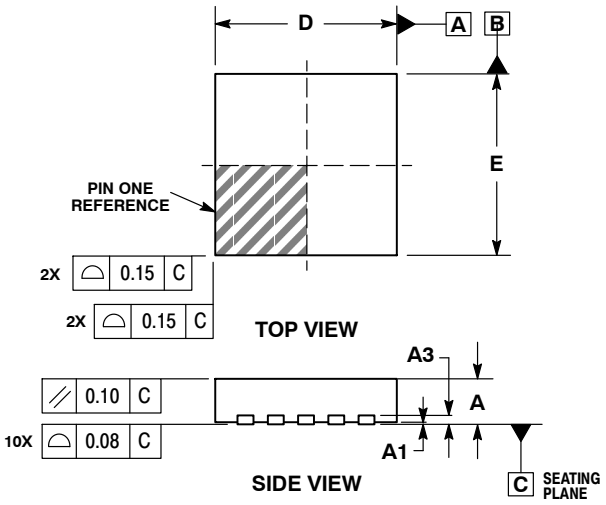
Device	Marking	Features	UVLO	VCLAMP	ISENSE	Package	Shipping†
NIS5420MT1TXG	20T1	Thermal Latching	8.5	15	Yes	WDFN10 (Pb−Free)	3000 / Tape & Reel
NIS5420MT2TXG	20T2	Thermal Latching	6.5	13.5	Yes		
NIS5420MT3TXG	20T3	Thermal Latching	8.5	NA	No		
NIS5420MT4TXG	20T4	Thermal Latching	8.5	15	No		
NIS5420MT5TXG	20T5	Auto−Retry	8.5	15	No		
NIS5420MT6TXG	20T6	Auto−Retry	8.5	15	Yes		
NIS5420MT7TXG	20T7	Auto−Retry	6.5	13.5	Yes		
NIS5420MT8TXG	20T8	Auto−Retry	6.5	NA	Yes		

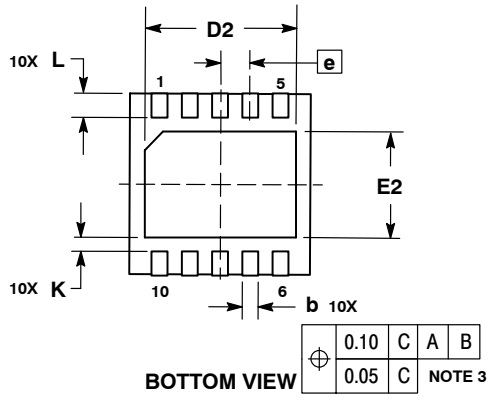
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

WDFN10, 3x3, 0.5P
CASE 522AA−01
ISSUE A

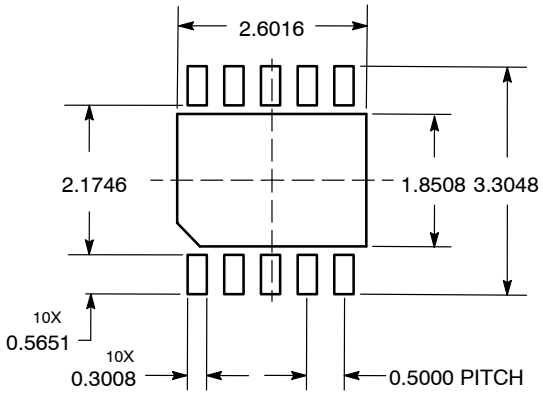
DATE 02 JUL 2007

SCALE 2:1





SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.03	0.05
A3		0.20 REF	
b	0.18	0.24	0.30
D		3.00 BSC	
D2	2.45	2.50	2.55
E		3.00 BSC	
E2	1.75	1.80	1.85
e		0.50 BSC	
K		0.19 TYP	
L	0.35	0.40	0.45

GENERIC MARKING DIAGRAM*

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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