36V Input Voltage, 200-mA, Ultra-low I_Q LDOs

LTP3558

General Description

The LTP3558 is a high voltage, low power consumption and high performance LD0. The family uses an advanced CMOS process and a P-MOSFET pass device to achieve fast start-up, with high output voltage accuracy. The LTP3558 is stable with a 1.0μ F~ 10μ F ceramic output capacitor, and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 2% over all load, line, process, and temperature variations.

Features

- Wide Input Voltage Range: up to 36V
- Output Current: 200mA
- Standard Fixed Output Voltage Options: 1.8V, 2.5V, 3.0V, 3.3V, 3.6V, and 5.0V
- Other Output Voltage Options Available on Request
- Low IQ: 1.5μA
- Low Dropout Voltage
- Short current protection: 100mA
- Excellent Load and Line Transient Response
- Line Regulation: 0.01%/V Typically
- Available Packages:

Order Information

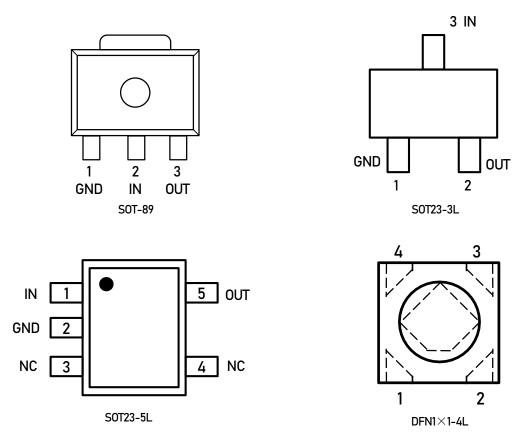
Model	Package	Ordering Number Note1	Packing Option
LTP3558	SOT23-3L	LTP3558-xxXT3	Tape and Reel, 3000
	S0T23-5L	LTP3558-xxXT5	Tape and Reel, 3000
	DFN1x1-4L	LTP3558-xxXF4	Tape and Reel, 10000
	S0T-89	LTP3558-xxXT4	Tape and Reel, 1000

Notel: xx stands for output voltage, e.g. if xx = 18, the output voltage is 1.8V; if xx = 30, the output voltage is 3.0V.

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Pin Configuration



TOP VIEW

Pin Function

Pin No.		D: N			
SOT-89	S0T23-3L	– Pin Name	Pin Function		
1	1	GND	Ground.		
2	3	IN	Supply input pin. Must be closely decoupled to GND with a $1\mu\text{F}$ or greater ceramic capacitor.		
3	2	OUT	Output pin. Bypass a $1\mu F$ or greater ceramic capacitor from this pin to ground.		

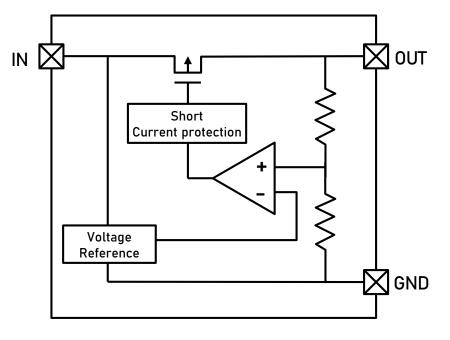


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	Pin No.		Din Mana	Dia Eurotian		
S0T2	23-5L	DFN1x1-4L	Pin Name	Pin Function		
1		3	IN	Supply input pin. Must be closely decoupled to GND with a $1\mu\text{F}$ or greater ceramic capacitor.		
2		2	GND	Ground.		
3		4	NC	No connection.		
4			NC	No connection.		
5		1	OUT	Output pin. Bypass a $1\!\mu\text{F}$ or greater ceramic capacitor from this pin to ground.		

Block Diagram



Functional Description

Input Capacitor

A 1µF-10µF ceramic capacitor is recommended to connect between Vin and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both Vin and GND.



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Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 1 μ F to 10 μ F, Equivalent Series Resistance (ESR) is from 5m Ω to 100m Ω , and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins.

Low Quiescent Current

The LTP3558, consuming only around 1.5 μ A for all input range and output loading, provides great power saving in portable and low power applications.

Short Current Limit Protection

When output current at the OUT pin is higher than current limit threshold or the OUT pin is short-circuit to GND, the short current limit protection will be triggered and clamp the output current to approximately 100mA to prevent over-current and to protect the regulator from damage due to overheating.

Absolute Maximum Ratings

Parameter	Rating	Unit		
IN pin to GND pin	-0.3 to 40	V		
OUT pin to GND pin	-0.3 to 6	V		
	SOT23-3L 360			
	SOT23-5L 250	°C /\/		
Thermal Resistance (Junction to Ambient)	DFN1X1-4L 180	– °C/W		
	SOT-89 135	_		
Operating Junction Temperature	-40 to 125	°C		
Storage Temperature	-65 to 150	°C		
Lead Temperature (Soldering, 10 sec)	300	°C		
ESD (HBM mode)	ESDA/JEDEC JS-001-2017	±2000V		





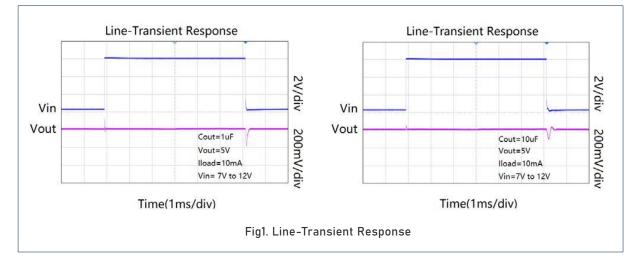
Electrical Characteristics

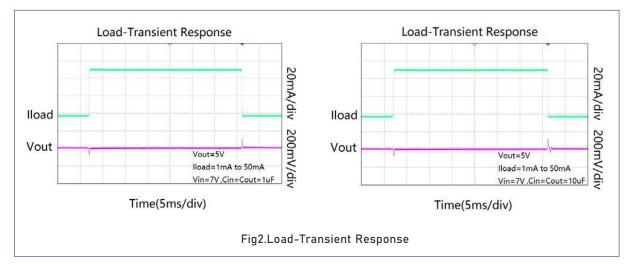
(V_{IN}= V_{0UT}+2V, T_a= 25 °C, C_{IN}=10uF, C_{0UT}=10uF unless otherwise noted)

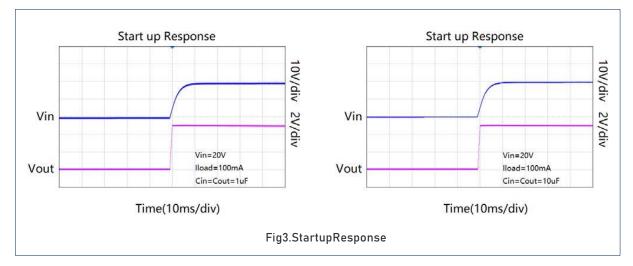
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Operation Range	V _{IN}				36	V
	V _{DROP}	V _{out} = 5V, I _{out} = 150mA		720		mV
Dropout Voltago		V _{out} = 5V, I _{out} = 100mA		420		
Dropout Voltage		V _{OUT} = 3.3 V, I _{OUT} = 150mA		820		
		V _{OUT} = 3.3 V, I _{OUT} = 100mA		520		
DC Supply Quiescent Current	Ι _α			1.5	3	μA
Regulated Output Voltage	V _{OUT}	I _{out} =1mA	V _{out} X 0.98		V _{QUT} X1.02	۷
Output Voltage Line Regulation	Reg _{LINE}	V _{IN} = V _{OUT} +1V to 30V, Iout = 10mA (△V _{OUT} /△V _{IN} /V _{OUT})		0.01	0.04	%/V
Output Voltage Load	Reg _{LOAD}	I _{out} from 1mA to 150mA V _{IN} =V _{out} +2V		5	20	mV
Regulation		l _{out} from 1mA to 150mA V _{IN} =10V		25	60	mV
Maximum Output Current	Ι _{ουτ}	V _{IN} = V _{OUT} +1V	200			mA
Short Current Protection	I _{SHORT}	OUT short to GND		100		mA
Output Noise	e _N	10Hz to 100kHz, I _{out} = 30mA,		90		μV _{rms}



TYPICAL PERFORMANCE CHARACTERISTICS









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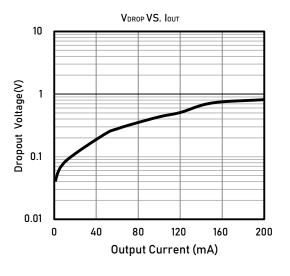
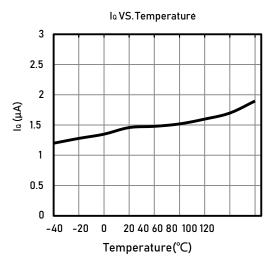


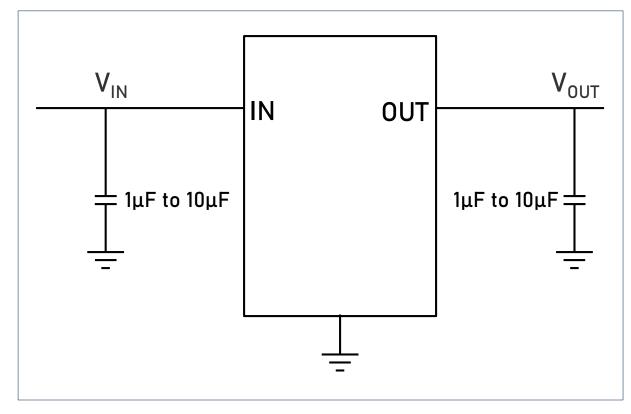
Fig4. Dropout Voltage VS Output Current







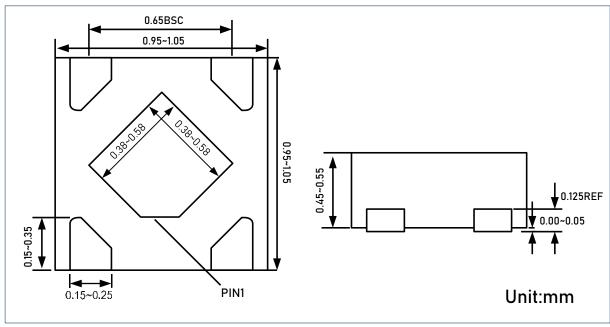
Application Circuits



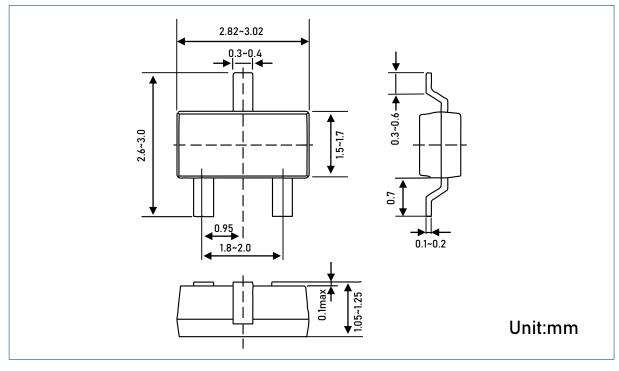


Package Dimension

DFN1x1-4L



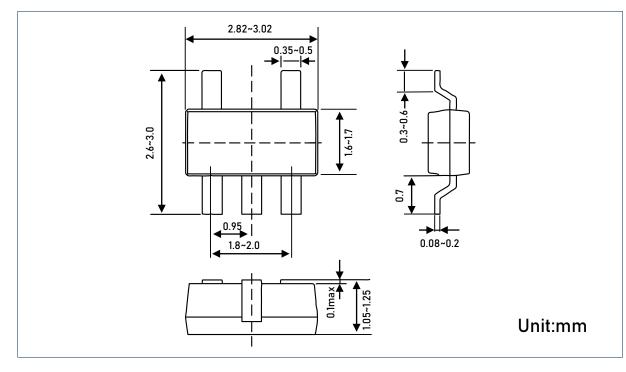
S0T23-3L



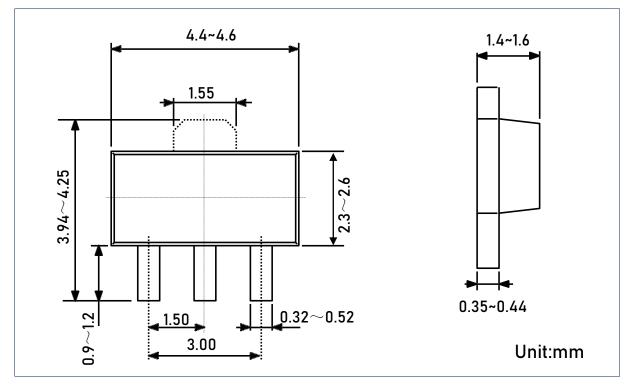
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S0T23-5L



SOT-89



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