General Description

The LTC321/LTC358/LTC324 family of single-, dual-, and quad- channel operational amplifiers is specifically designed for general-purpose cost-sensitive systems and applications. Featuring rail-to-rail input and output (RRIO) swings, and low quiescent current (typical 85 µA) combined with a wide bandwidth (1.2 MHz) and low noise (30 nV/√Hz at 1 kHz) makes this family very attractive for a variety of battery-powered applications that require a good balance between cost and performance, such as audio outputs, consumer electronics, smoke detectors, portable medical devices and white goods. The low input bias current supports these amplifiers to be used in applications with mega-ohm source impedances.

The robust design of the LTC321/LTC358/LTC324 family provides ease-of-use to the circuit designer: unity-gain stability with capacitive loads of up to 500 pF, integrated RF/EMI rejection filter, no phase reversal in overdrive conditions, and high electro-static discharge (ESD) protection (5-kV HBM). The LTC321/LTC358/LTC324 amplifiers are optimized for operation at voltages as low as +1.8 V (±0.9 V) and up to +5.5 V (±2.75 V), and over the extended temperature range of −40 °C to +125 °C.

The LTC321 (single) is available in both SOT23-5L and SC70-5L packages. The LTC358 (dual) is offered in SOIC-8L, DFN-8L and MSOP-8L packages. The quad-channel LTC324 is offered in SOIC-14L, TSSOP-14L and QFN-16L packages.

Features and Benefits

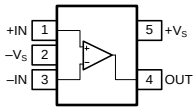
- General Purpose Amplifiers for Cost-Sensitive Systems
- 1.2 MHz GBW for Unity-Gain Stable
- Micro-Power: 85 µA Supply Current Per Amplifier
- Low Input Offset Voltage: ±3.0 mV Maximum
- Low Noise: 30 nV/√Hz at 1 kHz
- Single 1.8 V to 5.5 V Supply Voltage Range
- Rail-to-Rail Input and Output
- Internal RF/EMI Filter
- Extended Temperature Range: −40°C to +125°C

Applications

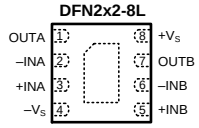
- Battery-Powered Instruments:
  - Consumer, Industrial, Medical, Notebooks
- Audio Outputs
- Wireless Sensors:
  - Home Security, Remote Sensing, Wireless Metering
- Sensor Signal Conditioning:
  - Sensor Interfaces, Loop-Powered, Active Filters

Pin Configurations (Top View)

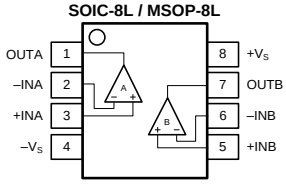
LTC321
SOT23-5L / SC70-5L



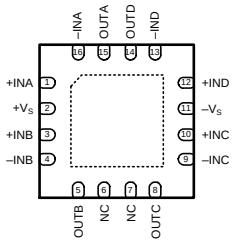
LTC358
DFN2x2-8L



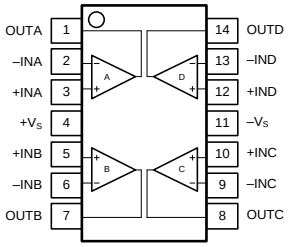
SOIC-8L / MSOP-8L



LTC324
QFN3x3-16L



LTC324
SOIC-14L / TSSOP-14L



Pin Description

Symbol	Description
–IN	Inverting input of the amplifier. The voltage range is from (V_{S-} – 0.1V) to (V_{S+} + 0.1V).
+IN	Non-inverting input of the amplifier. This pin has the same voltage range as –IN.
$+V_S$	Positive power supply.
$-V_S$	Negative power supply.
OUT	Amplifier output.

Ordering Information

Type Number	Package Name	Package Quantity	Marking Code (1)
LTC321XT5/R6	SOT23-5L	Tape and Reel, 3 000	321, 321I
LTC321XC5/R6	SC70-5L	Tape and Reel, 3 000	321
LTC358XS8/R8	SOIC-8L	Tape and Reel, 4 000	358 x, C42
LTC358XF8/R6	DFN2x2-8L	Tape and Reel, 3 000	358x, C42
LTC358XV8/R6	MSOP-8L	Tape and Reel, 3 000	358x, AG2
LTC324XS14/R5	SOIC-14L	Tape and Reel, 2 500	324 x, C44
LTC324XT14/R6	TSSOP-14L	Tape and Reel, 3 000	324 x, AG4
LTC324XF16/R6	QFN3x3-16L	Tape and Reel, 3 000	AG4x, 324x

(1) There may be multiple device markings, a varied marking character of "x", or additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

Limiting Value

In accordance with the Absolute Maximum Rating System (IEC 60134).

Parameter	Absolute Maximum Rating
Supply Voltage, V_{S+} to V_{S-}	10.0 V
Signal Input Terminals: Voltage, Current	V_{S-} – 0.5 V to V_{S+} + 0.5 V, ±10 mA
Output Short-Circuit	Continuous
Storage Temperature Range, T_{stg}	–65 °C to +150 °C
Junction Temperature, T_J	150 °C
Lead Temperature Range (Soldering 10 sec)	260 °C

ESD Rating

Parameter	Item	Value	Unit
Electrostatic Discharge Voltage	Human body model (HBM), per MIL-STD-883J / Method 3015.9 (1)	±5 000	V
	Charged device model (CDM), per ESDA/JEDEC JS-002-2014 (2)	±2 000	
	Machine model (MM), per JESD22-A115C	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible if necessary precautions are taken.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible if necessary precautions are taken.

Electrical Characteristics

V_S = 5.0V, T_A = +25°C, V_{CM} = V_S/2, V_O = V_S/2, and R_L = 10kΩ connected to V_S/2, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = −40 to +125 °C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			±0.7	±3.0	mV
V_{OS} TC	Offset voltage drift	T_A = −40 to +125 °C		**±1**	**3.5**	µV/°C
PSRR	Power supply rejection ratio	V_S = 2.0 to 5.5 V, V_{CM} < V_{S+} − 2V	80	110		dB
		T_A = −40 to +125 °C	75			
INPUT BIAS CURRENT						
I_B	Input bias current			5	50	pA
		T_A = −40 to +85 °C			200	
		T_A = −40 to +125 °C			**2000**	
I_{OS}	Input offset current			10	50	pA
NOISE						
V_n	Input voltage noise	f = 0.1 to 10 Hz		6		$µV_{P-P}$
e_n	Input voltage noise density	f = 10 kHz		27		nV/√Hz
		f = 1 kHz		30		
I_n	Input current noise density	f = 1 kHz		5		fA/√Hz
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range		V_{S-}−0.1		V_{S+}+0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V, V_{CM} = −0.1 to 5.6 V	70	83		dB
		V_{CM} = 0 to 5.3 V, T_A = −40 to +125 °C	**65**			
		V_S = 2.0 V, V_{CM} = −0.1 to 2.1 V	65	77		
		V_{CM} = 0 to 1.8 V, T_A = −40 to +125 °C	**60**			
INPUT IMPEDANCE						
C_{IN}	Input capacitance	Differential		2.0		pF
		Common mode		3.5		
OPEN-LOOP GAIN						
A_{VOL}	Open-loop voltage gain	R_L = 50 kΩ, V_O = 0.05 to 3.5 V	90	105		dB
		T_A = −40 to +125 °C	**85**			
		R_L = 2 kΩ, V_O = 0.15 to 3.5 V	85	100		
		T_A = −40 to +125 °C	**80**			
FREQUENCY RESPONSE						
GBW	Gain bandwidth product			1.2		MHz
SR	Slew rate	G = +1, C_L = 100 pF, V_O = 1.5 to 3.5 V		1		V/µs
THD+N	Total harmonic distortion + noise	G = +1, f = 1 kHz, V_O = 1 V_{RMS}		0.003		%
t_S	Settling time	To 0.1%, G = +1, 1V step		1.5		µs
		To 0.01%, G = +1, 1V step		1.8		
t_{OR}	Overload recovery time	To 0.1%, V_{IN} * Gain > V_S		2.5		µs

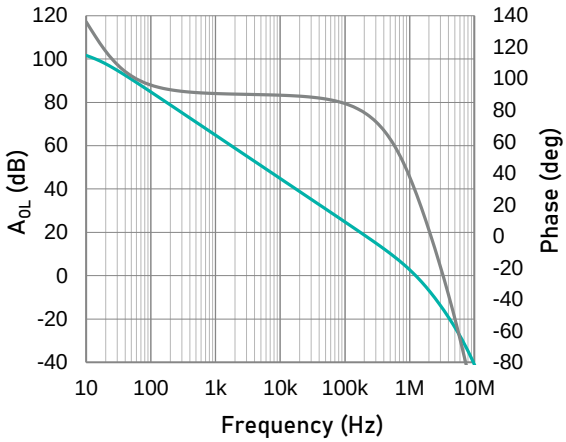
Electrical Characteristics (continued)

V_S = 5.0V, T_A = +25°C, V_{CM} = V_S/2, V_O = V_S/2, and R_L = 10kΩ connected to V_S/2, unless otherwise noted. Boldface limits apply over the specified temperature range, T_A = −40 to +125 °C.

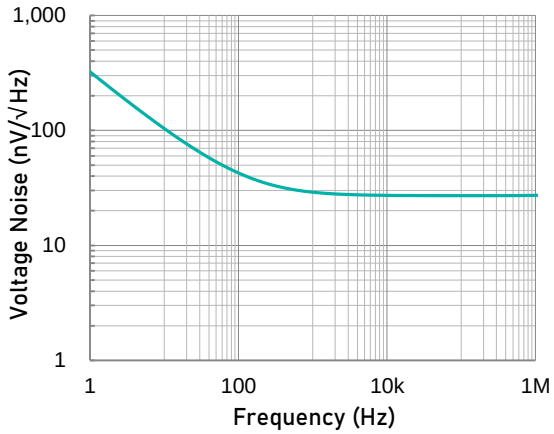
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
OUTPUT						
V_{OH}	High output voltage swing	R_L = 50 kΩ	V_{S+}−6	V_{S+}−3		mV
		R_L = 2 kΩ	V_{S+}−100	V_{S+}−65		
V_{OL}	Low output voltage swing	R_L = 50 kΩ		V_{S-}+2	V_{S-}+4	mV
		R_L = 2 kΩ		V_{S-}+42	V_{S-}+65	
I_{SC}	Short-circuit current	Source current through 10Ω		40		mA
		Sink current through 10Ω		50		
POWER SUPPLY						
V_S	Operating supply voltage		1.8		5.5	V
I_Q	Quiescent current (per amplifier)			85	120	µA
		T_A = −40 to +125 °C			**150**	
THERMAL CHARACTERISTICS						
T_A	Operating temperature range		−40		+125	°C
$θ_{JA}$	Package Thermal Resistance	SC70-5L		333		°C/W
		SOT23-5L		190		
		DFN2x2-8L		94		
		MSOP-8L		201		
		SOIC-8L		125		
		QFN3x3-16L		65		
		TSSOP-14L		112		
		SOIC-14L		115		

Typical Performance Characteristics

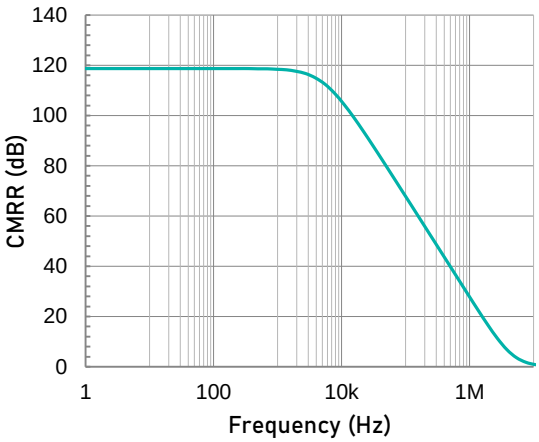
At T_A = +25°C, V_{CM} = V_S/2, and R_L = 10kΩ connected to V_S/2, unless otherwise noted.



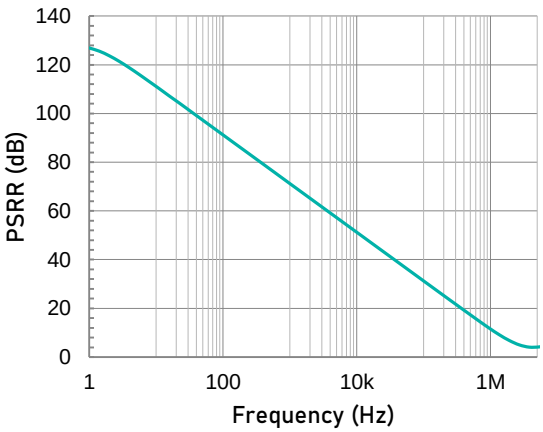
Open-loop Gain and Phase as a function of Frequency.



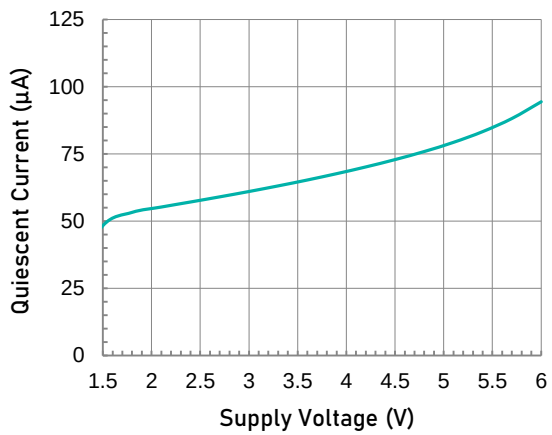
Input Voltage Noise Spectral Density as a function of Frequency.



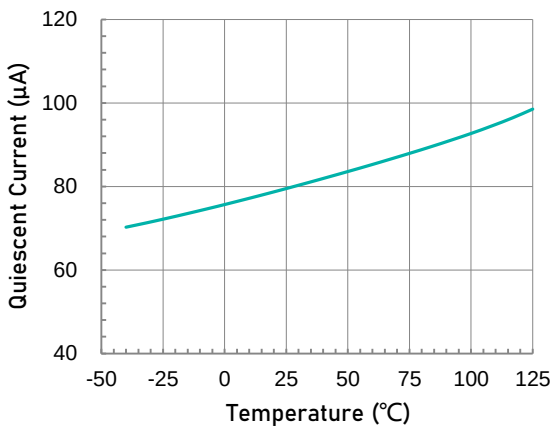
Common-mode Rejection Ratio as a function of Frequency.



Power Supply Rejection Ratio as a function of Frequency.



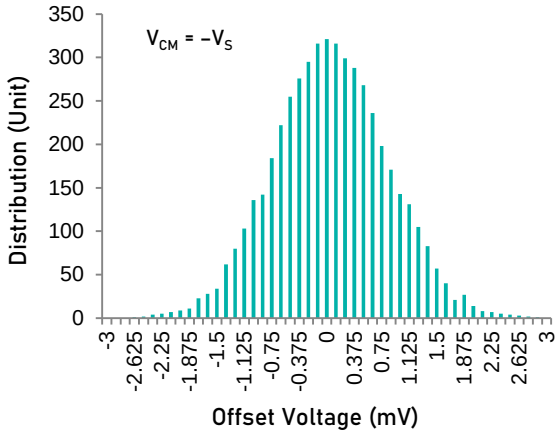
Quiescent Current as a function of Supply Voltage.



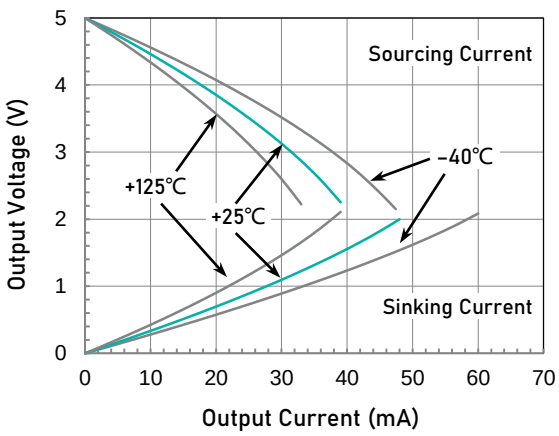
Quiescent Current as a function of Temperature.

Typical Performance Characteristics (continued)

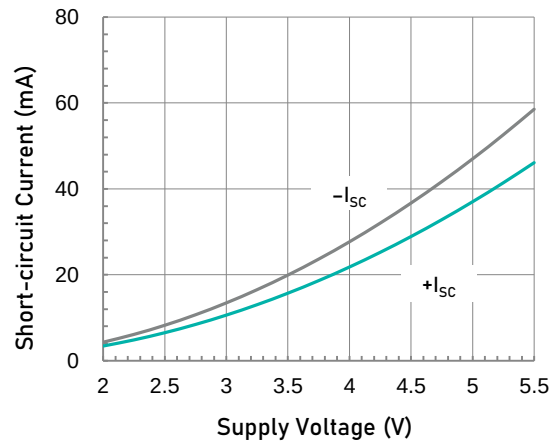
At T_A = +25°C, V_{CM} = V_S/2, and R_L = 10kΩ connected to V_S/2, unless otherwise noted.



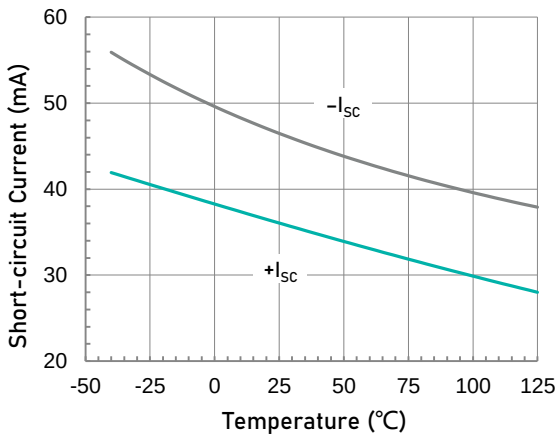
Offset Voltage Production Distribution



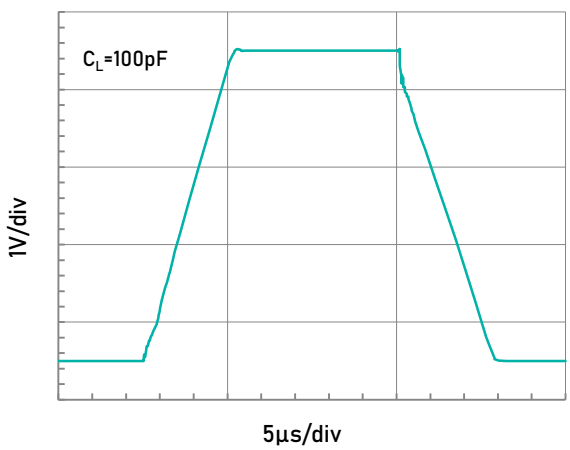
Output Voltage Swing as a function of Output Current.



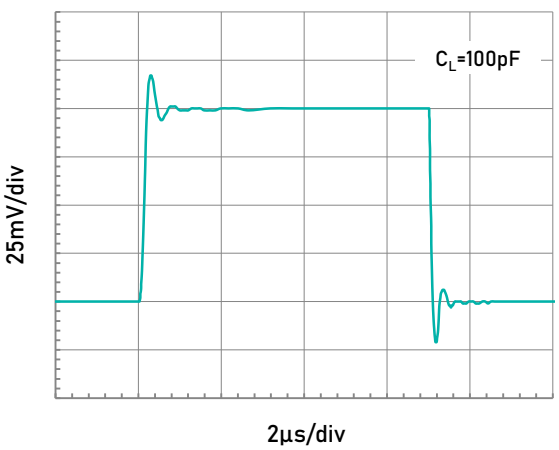
Short-circuit Current as a function of Supply Voltage.



Short-circuit Current as a function of Temperature.



Large Signal Step Response.



Small Signal Step Response.

Application Notes

The LTC321/LTC358/LTC324 is a family of low-power, rail-to-rail input and output operational amplifiers specifically designed for portable applications. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving ≤ 10-kΩ loads connected to any point between V_{S+} and ground. The input common-mode voltage range includes both rails, and allows the LTC321/LTC358/LTC324 family to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them ideal for driving sampling analog-to-digital converters (ADCs).

The LTC321/LTC358/LTC324 features 1.2-MHz bandwidth and 1-V/µs slew rate with only 85-µA supply current per amplifier, providing good ac performance at very low power consumption. DC applications are also well served with a low input noise voltage of 30-nV/√Hz at 1-kHz, low input bias current, and an input offset voltage of ±3.0-mV maximum. The typical offset voltage drift is 1-µV/°C, over the full temperature range the input offset voltage changes only 100-µV (0.7-mV to 0.8-mV).

OPERATING VOLTAGE

The LTC321/LTC358/LTC324 family is optimized for operation at voltages as low as +1.8 V (±0.9 V) and up to +5.5 V (±2.75 V). In addition, many specifications apply from –40 °C to +125 °C. Parameters that vary significantly with operating voltages or temperature are illustrated in the Typical Characteristics graphs.

NOTE: Supply voltages (V_{S+} to V_{S-}) higher than +10 V can permanently damage the device.

RAIL-TO-RAIL INPUT

The input common-mode voltage range of the LTC321/LTC358/LTC324 extends 100-mV beyond the negative and positive supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically V_{S+}–1.4 V to the positive supply, whereas the P-channel pair is active for inputs from 100-mV below the negative supply to approximately V_{S+}–1.4 V. There is a small transition region, typically V_{S+}–1.2 V to V_{S+}–1 V, in which both pairs are on. This 200-mV transition region can vary up to 200-mV with process variation. Thus, the transition region (both stages on) can range from V_{S+}–1.4 V to V_{S+}–1.2 V on the low end, up to V_{S+}–1 V to V_{S+}–0.8 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region.

The typical input bias current of the LTC321/LTC358 /LTC324 during normal operation is approximately 5-pA. In overdriven conditions, the bias current can increase significantly. The most common cause of an overdriven condition occurs when the operational amplifier is outside of the linear range of operation. When the output of the operational amplifier is driven to one of the supply rails, the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front-end input chopping switches that combine with electromagnetic interference (EMI) filter resistors to create the equivalent circuit. Notice that the input bias current remains within specification in the linear region.

INPUT EMI FILTER AND CLAMP CIRCUIT

Figure 1 shows the input EMI filter and clamp circuit. The LTC321/LTC358/LTC324 op-amps have internal ESD protection diodes (D1, D2, D3, and D4) that are connected between the inputs and each supply rail. These diodes protect the input transistors in the event of electrostatic discharge and are reverse biased during normal operation. This protection scheme allows voltages as high as approximately 500-mV beyond the rails to be applied at the input of either terminal without causing permanent damage. These ESD protection current-steering diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 20-mA as stated in the Absolute Maximum Ratings.

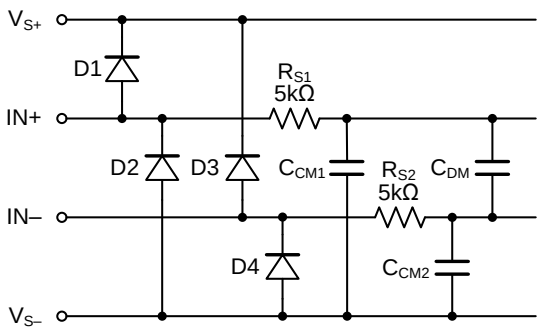


Figure 1. Input EMI Filter and Clamp Circuit

Operational amplifiers vary in susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The EMI filter of the LTC321/358/324

Application Notes (continued)

is composed of two 5-kΩ input series resistors (R_{S1} and R_{S2}), two common-mode capacitors (C_{CM1} and C_{CM2}), and a differential capacitor (C_{DM}). These RC networks set the –3 dB low-pass cutoff frequencies at 35-MHz for common-mode signals, and at 22-MHz for differential signals.

RAIL-TO-RAIL OUTPUT

Designed as a micro-power, low-noise op-amp, the LTC321/358/324 delivers a robust output drive capability. A class AB output stage with common - source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 50-kΩ, the output swings typically to within 3-mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails. For resistive loads up to 2-kΩ, the output swings typically to within 65-mV of the positive supply rail and within 42-mV of the negative supply rail.

CAPACITIVE LOAD AND STABILITY

The LTC321/LTC358/LTC324 family can safely drive capacitive loads of up to 500-pF in any configuration. As with most amplifiers, driving larger capacitive loads than specified may cause excessive overshoot and ringing, or even oscillation. A heavy capacitive load reduces the phase margin and causes the amplifier frequency response to peak. Peaking corresponds to over-shooting or ringing in the time domain. Therefore, it is recommended that external compensation be used if these op-amps must drive a load exceeding 500-pF. This compensation is particularly important in the unity-gain configuration, which is the worst case for stability.

A quick and easy way to stabilize the op-amp for capacitive load drive is by adding a series resistor, R_{ISO}, between the amplifier output terminal and the load capacitance, as shown in Figure 2. R_{ISO} isolates the amplifier output and feedback network from the capacitive load. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Note that this method results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the R_L.

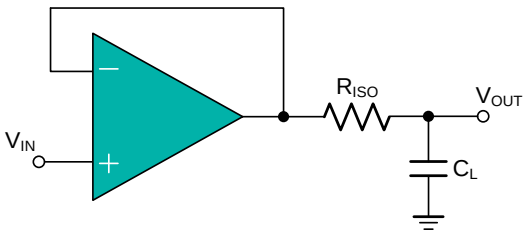


Figure 2. Indirectly Driving Heavy Capacitive Load

An improvement circuit is shown in Figure 3. It provides DC accuracy as well as AC stability. The R_F provides the DC accuracy by connecting the inverting signal with the output.

The C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

For no-buffer configuration, there are two others ways to increase the phase margin: (a) by increasing the amplifier's gain, or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

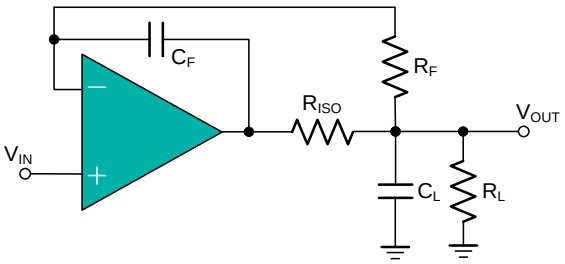


Figure 3. Indirectly Driving Heavy Capacitive Load with DC Accuracy

OVERLOAD RECOVERY

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, either because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the LTC321/LTC358/LTC324 is approximately 2.5-µs.

EMI REJECTION RATIO

Circuit performance is often adversely affected by high frequency EMI. When the signal strength is low and transmission lines are long, an op-amp must accurately amplify the input signals. However, all op-amp pins — the non-inverting input, inverting input, positive supply, negative supply, and output pins — are susceptible to EMI signals. These high frequency signals are coupled into an op-amp by various means, such as conduction, near field radiation, or far field radiation. For example, wires and printed circuit board (PCB) traces can act as antennas and pick up high frequency EMI signals.

Application Notes (continued)

Amplifiers do not amplify EMI or RF signals due to their relatively low bandwidth. However, due to the nonlinearities of the input devices, op-amps can rectify these out of band signals. When these high frequency signals are rectified, they appear as a dc offset at the output.

The LTC321/LTC358/LTC324 have integrated EMI filters at their input stage. A mathematical method of measuring EMIRR is defined as follows:

$$EMIRR = 20 \log (V_{IN\_PEAK} / \Delta V_{OS})$$

INPUT-TO-OUTPUT COUPLING

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

MAXIMIZING PERFORMANCE THROUGH PROPER LAYOUT

To achieve the maximum performance of the extremely high input impedance and low offset voltage of the LTC321/LTC358/LTC324, care is needed in laying out the circuit board. The PCB surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and provides a humidity barrier, reducing parasitic resistance on the board. The use of guard rings around the amplifier inputs further reduces leakage currents. Figure 4 shows proper guard ring configuration and the top view of a surface-mount layout. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. By setting the guard ring voltage equal to the voltage at the non-inverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PCB using Teflon standoff insulators.

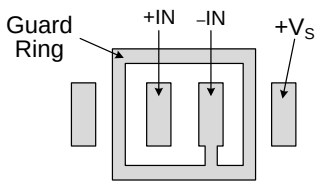


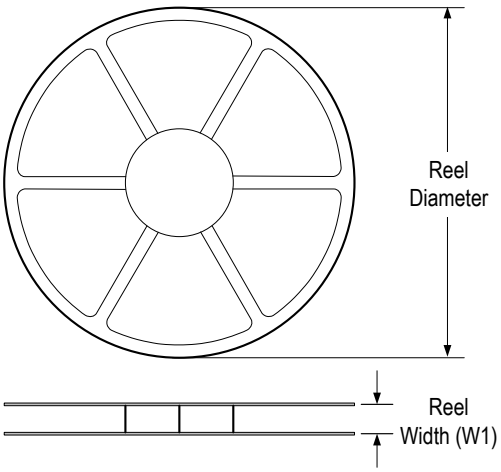
Figure 4. Use a guard ring around sensitive pins

Other potential sources of offset error are thermoelectric voltages on the circuit board. This voltage, also called Seebeck voltage, occurs at the junction of two dissimilar metals and is proportional to the temperature of the junction. The most common metallic junctions on a circuit board are solder-to-board trace and solder-to-component lead. If the temperature of the PCB at one end of the component is different from the temperature at the other end, the resulting Seebeck voltages are not equal, resulting in a thermal voltage error.

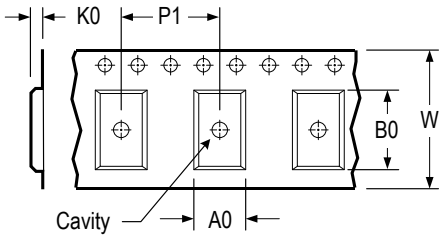
This thermocouple error can be reduced by using dummy components to match the thermoelectric error source. Placing the dummy component as close as possible to its partner ensures both Seebeck voltages are equal, thus canceling the thermocouple error. Maintaining a constant ambient temperature on the circuit board further reduces this error. The use of a ground plane helps distribute heat throughout the board and reduces EMI noise pickup.

Tape and Reel Information

REEL DIMENSIONS

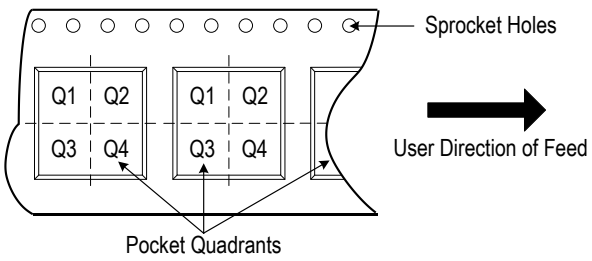


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIETATION IN TAPE

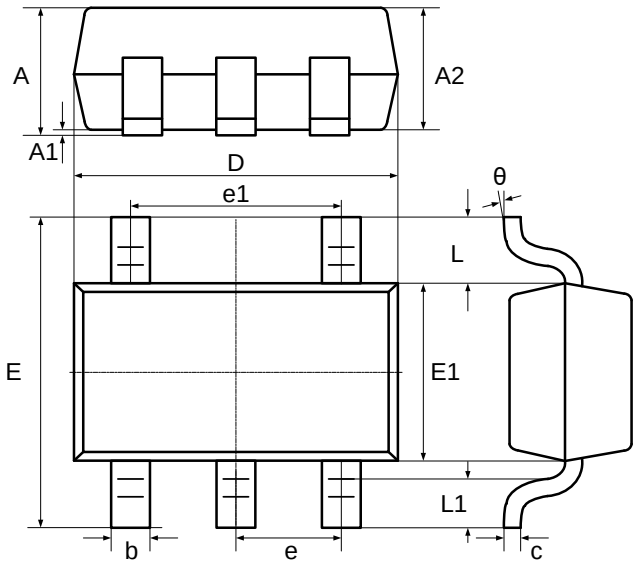


* All dimensions are nominal

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
LTC321XT5/R6	SOT23	5	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3

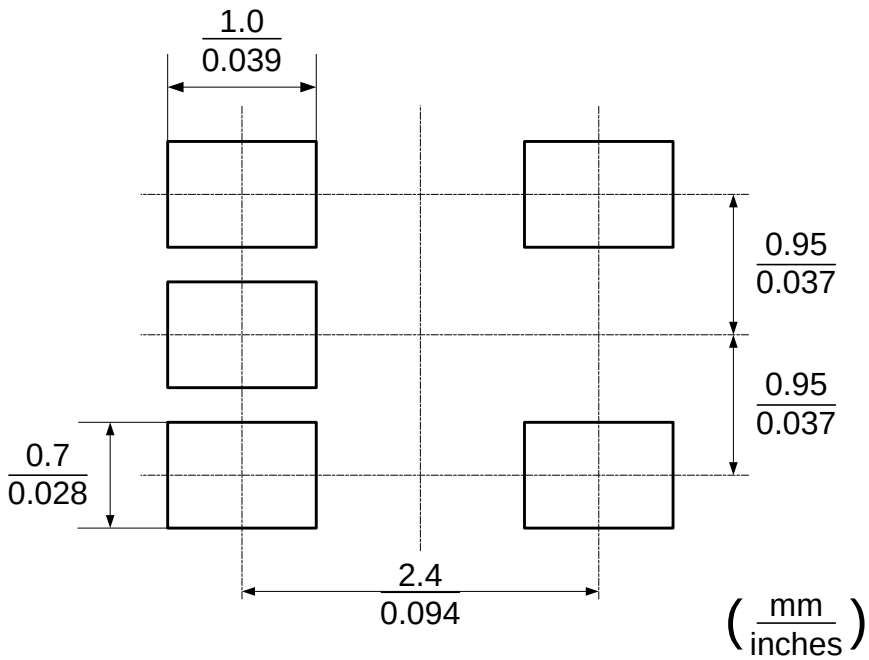
Package Outlines (continued)

DIMENSIONS, SOT23-5L



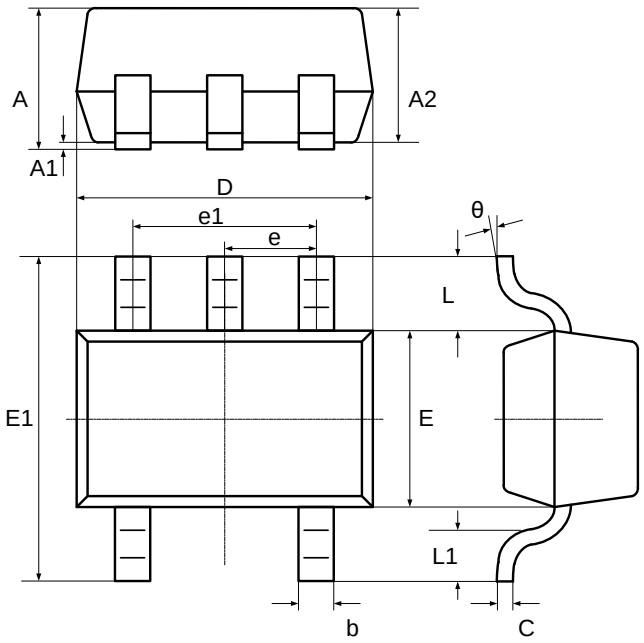
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	-	1.35	-	0.053
A1	0.00	0.15	0.000	0.006
A2	1.00	1.20	0.039	0.047
b	0.35	0.45	0.014	0.018
c	0.14	0.20	0.006	0.008
D	2.82	3.02	0.111	0.119
E1	1.526	1.726	0.060	0.068
E	2.60	3.00	0.102	0.118
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.60 REF		0.024 REF	
L1	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, SOT23-5L



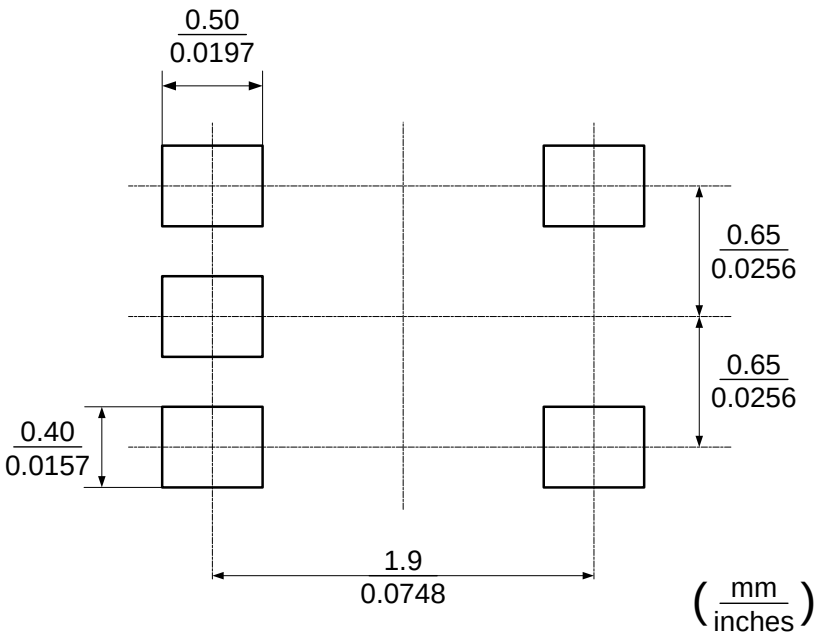
Package Outlines

DIMENSIONS, SC70-5L (SOT353)



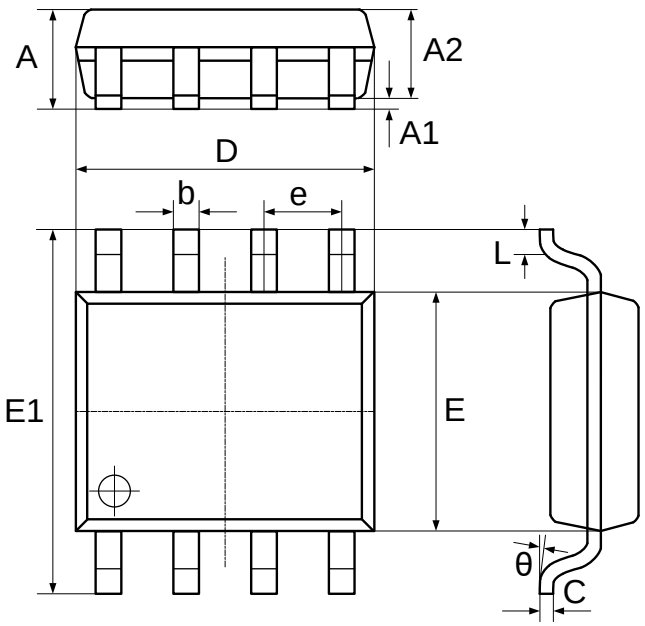
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.90	1.10	0.035	0.043
A1	0.00	0.10	0.000	0.004
A2	0.90	1.00	0.035	0.039
b	0.15	0.35	0.006	0.014
C	0.08	0.15	0.003	0.006
D	2.00	2.20	0.079	0.087
E	1.15	1.35	0.045	0.053
E1	2.15	2.45	0.085	0.096
e	0.65 typ.		0.026 typ.	
e1	1.20	1.40	0.047	0.055
L	0.525 ref.		0.021 ref.	
L1	0.26	0.46	0.010	0.018
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, SC70-5L (SOT353)



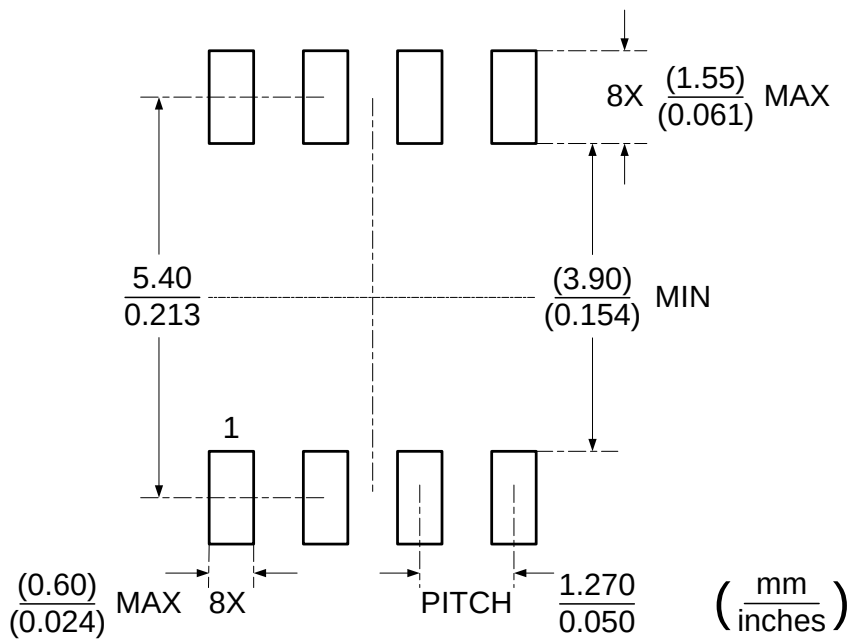
Package Outlines (continued)

DIMENSIONS, SOIC-8L



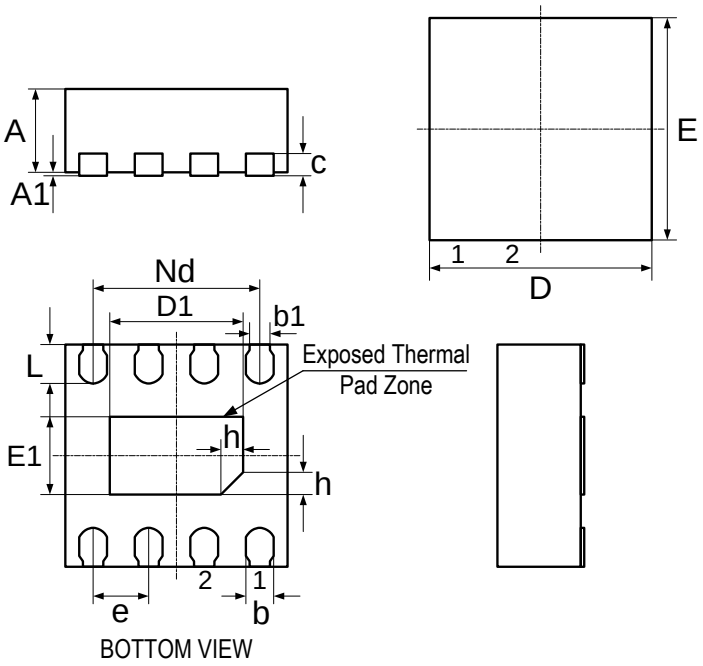
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.370	1.670	0.054	0.066
A1	0.070	0.170	0.003	0.007
A2	1.300	1.500	0.051	0.059
b	0.306	0.506	0.012	0.020
C	0.203 TYP.		0.008 TYP.	
D	4.700	5.100	0.185	0.201
E	3.820	4.020	0.150	0.158
E1	5.800	6.200	0.228	0.244
e	1.270 TYP.		0.050 TYP.	
L	0.450	0.750	0.018	0.030
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, SOIC-8L



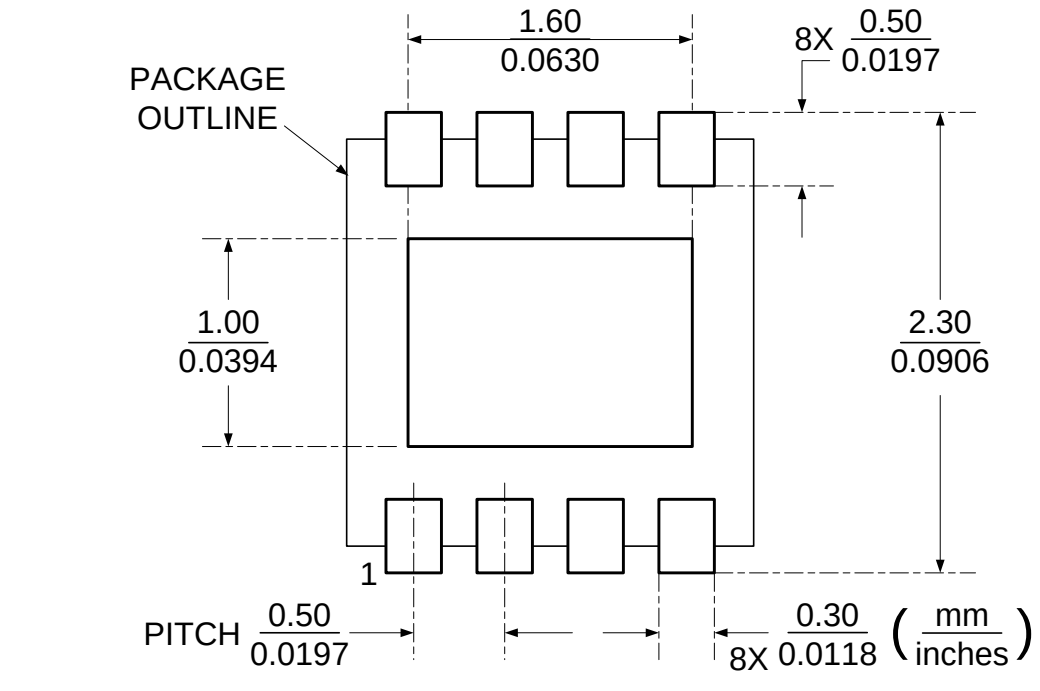
Package Outlines (continued)

DIMENSIONS, DFN2x2-8L



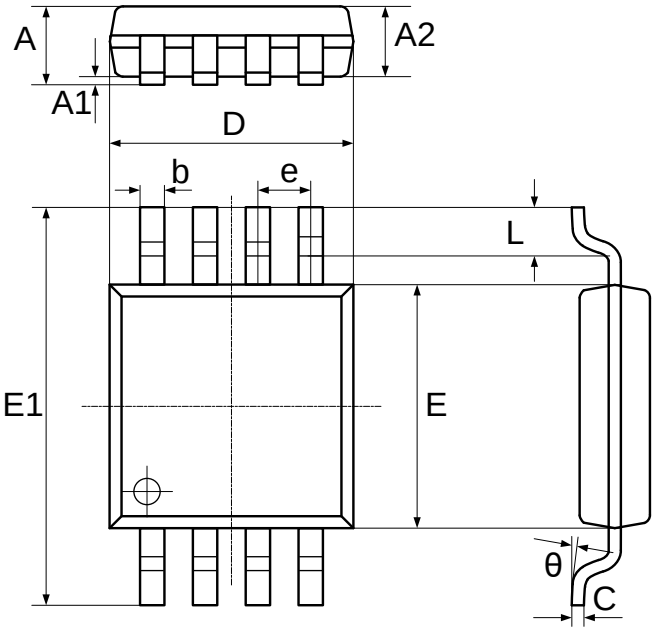
Symbol	Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.20	0.25	0.30
b1		0.18 REF	
c	0.18	0.20	0.25
D	1.90	2.00	2.10
D1	1.10	1.20	1.30
Nd		1.50BSC	
E	1.90	2.00	2.10
E1	0.60	0.70	0.80
e		0.50BSC	
L	0.30	0.35	0.40
h	0.15	0.20	0.25

RECOMMENDED SOLDERING FOOTPRINT, DFN2x2-8L



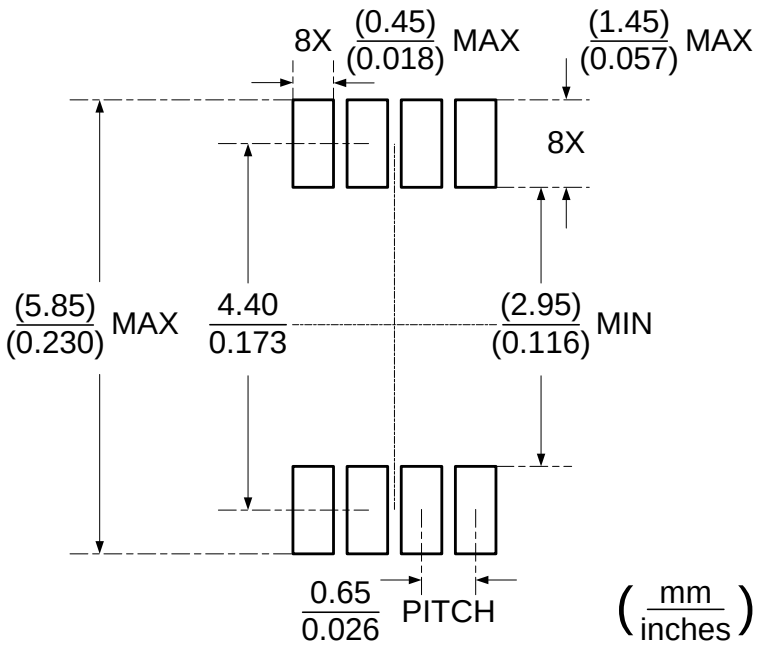
Package Outlines (continued)

DIMENSIONS, MSOP-8L



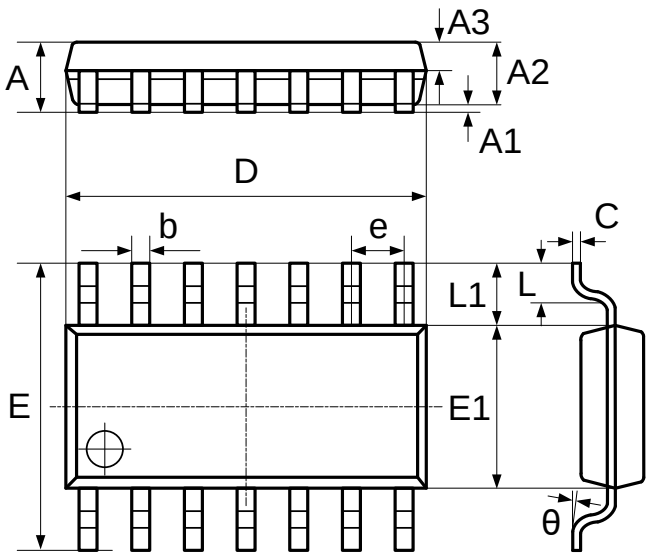
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.031	0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
b	0.290	0.380	0.011	0.015
C	0.150	0.200	0.006	0.008
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
e	0.650 TYP.		0.026 TYP.	
L	0.400	0.700	0.016	0.028
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, MSOP-8L



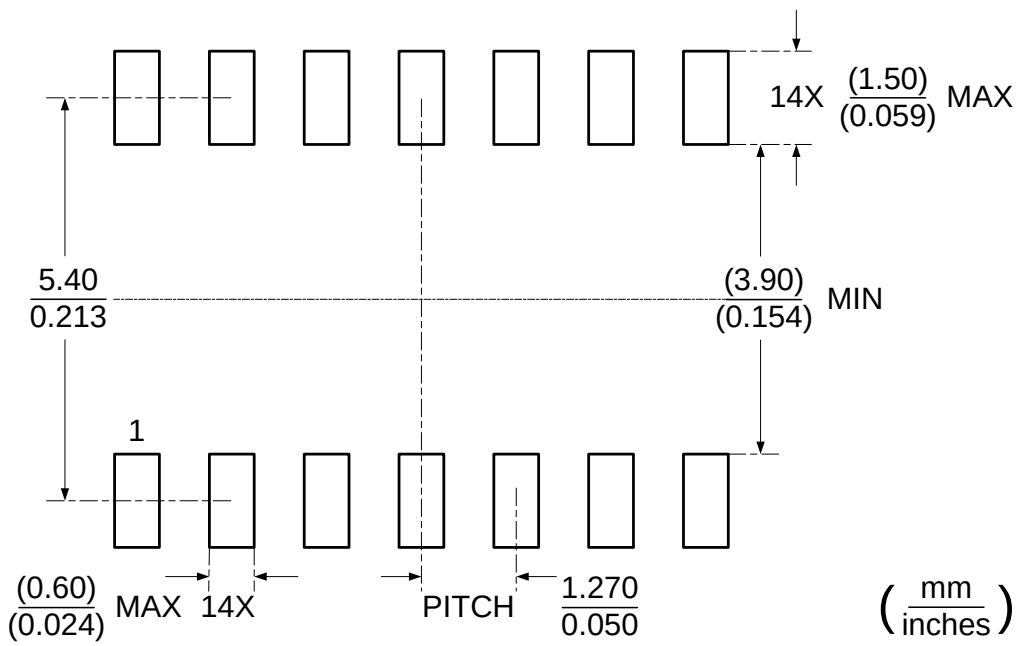
Package Outlines (continued)

DIMENSIONS, SOIC-14L



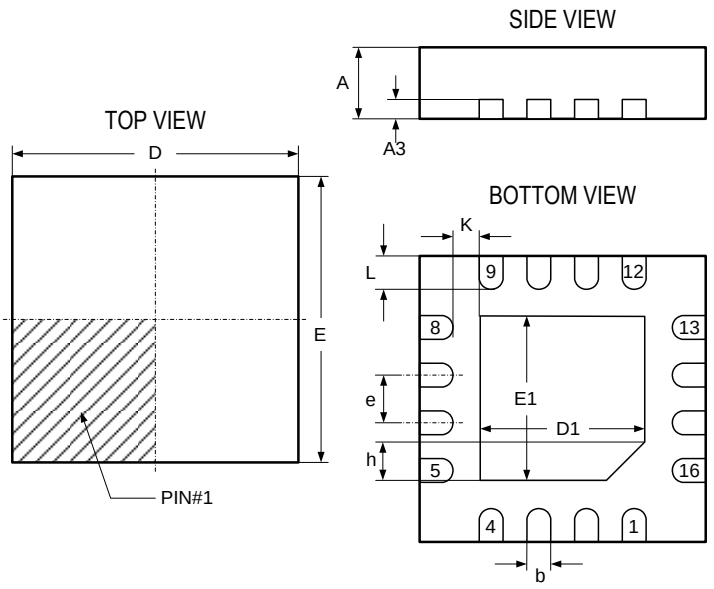
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.450	1.850	0.057	0.073
A1	0.100	0.300	0.004	0.012
A2	1.350	1.550	0.053	0.061
A3	0.550	0.750	0.022	0.030
b	0.406 TYP.		0.016 TYP.	
C	0.203 TYP.		0.008 TYP.	
D	8.630	8.830	0.340	0.348
E	5.840	6.240	0.230	0.246
E1	3.850	4.050	0.152	0.159
e	1.270 TYP.		0.050 TYP.	
L1	1.040 REF.		0.041 REF.	
L	0.350	0.750	0.014	0.030
θ	2°	8°	2°	8°

RECOMMENDED SOLDERING FOOTPRINT, SOIC-14L



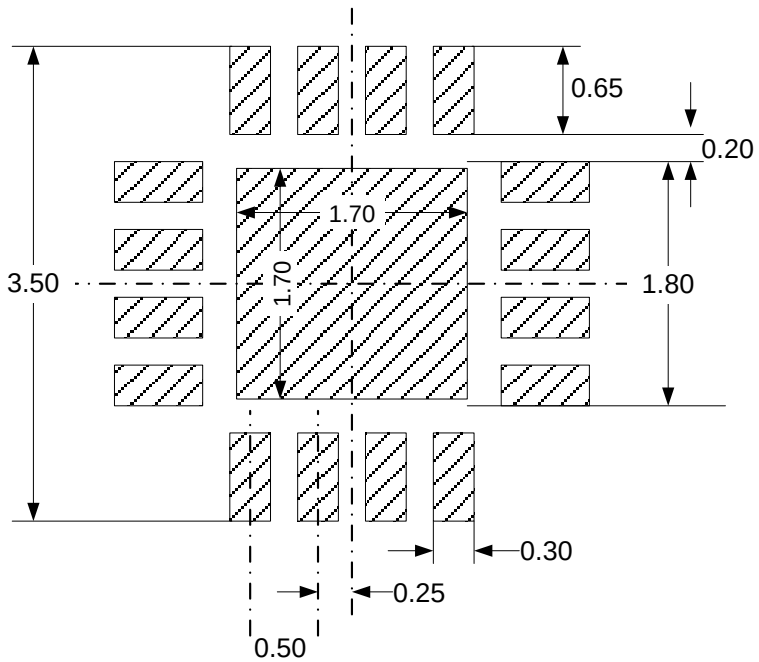
Package Outlines

DIMENSIONS, QFN3x3-16L



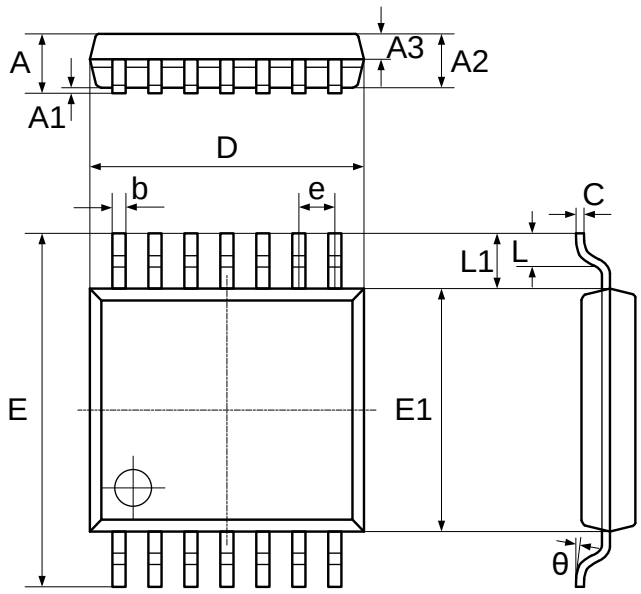
Symbol	Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A3		0.210 REF.	
b	0.20	0.25	0.30
D	2.90	3.00	3.10
D1	1.60	1.65	1.70
E	2.90	3.00	3.10
E1	1.60	1.65	1.70
e		0.50 BSC.	
h	0.20	0.25	0.30
K	0.225	0.275	0.325
L	0.35	0.40	0.45

RECOMMENDED SOLDERING FOOTPRINT, QFN3x3-16L



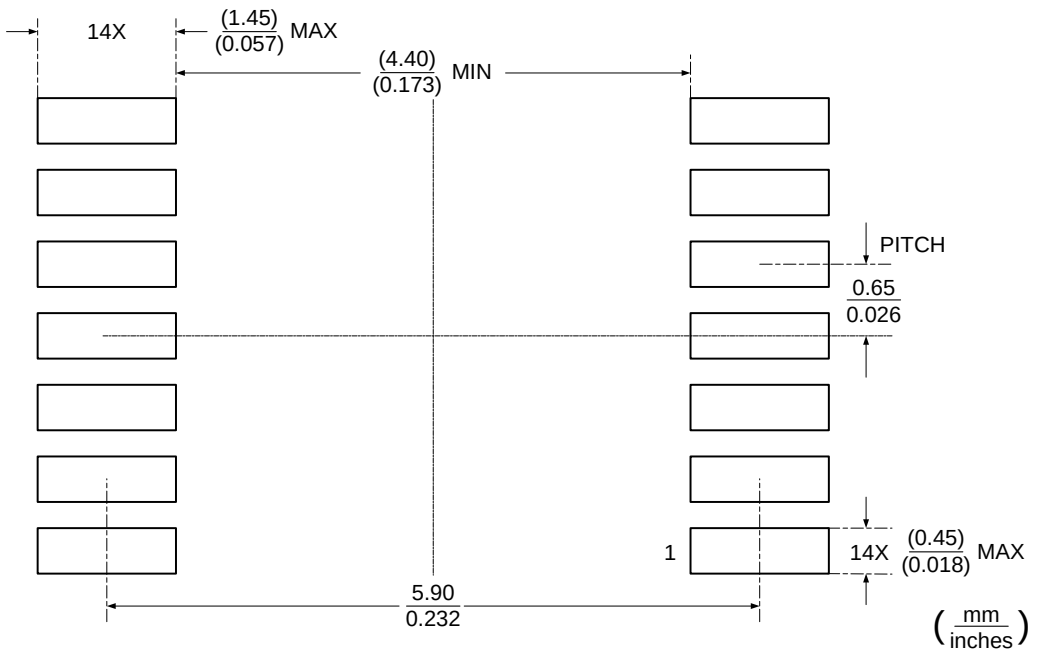
Package Outlines (continued)

DIMENSIONS, TSSOP-14L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	-	1.200	-	0.047
A1	0.050	0.150	0.002	0.006
A2	0.900	1.050	0.035	0.041
A3	0.390	0.490	0.015	0.019
b	0.200	0.290	0.008	0.011
C	0.130	0.180	0.005	0.007
D	4.860	5.060	0.191	0.199
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 TYP.		0.026 TYP.	
L1	1.000 REF.		0.039 REF.	
L	0.450	0.750	0.018	0.030
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, TSSOP-14L



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