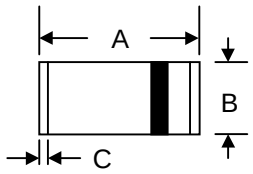
LLDB3/LLDB4

佑风电子 YFSEMI ELECTRON

SILICON BIDIRECTIONAL DIACS

Features

The three layer, two terminal, axial lead,hermetically sealed diacs are designed specifically for triggering thyristors. They demonstrate low breakover current at breakover voltage as they withstand peak pulse current, The breakover symmetry is within three volts (DB3,DB4). These diacs are intended for use in thyrisitors phase control , circuits for lamp dimming,universa motor speed control ,and heat control.



MiniMELF		
Dim	**Mln**	**Max**
A	3.30	3.70
B	1.30	1.60
C	0.28	0.50
All Dimensions in mm		

Mechanical Data

- Case: MiniMELF Glass Case (SOD-80)
- Terminals: Plated Leads Solderable per MIL-STD-202, Method 208
- Polarity: Color band denotes cathode end
- Weight: 0.05 grams (approx.)
- Mounting Position: Any
- Marking: Type Number
- **Lead Free: For RoHS / Lead Free Version**

Maximum Ratings and Electrical Characteristics @T_A=25°C

ABSOLUTE RATINGS

PARAMETERS	SYMBOL	VALUE	UNITS
		LLDB3 / LLDB4	
Power Dissipation on Printed Cir cuit(L=10mm) T_A=50℃	Pc	150	mW
Repetitive Peak on-state Current Tp=10uS f=100Hz	I_{TRM}	2.0	A
Storage and Operating Juntion Temperature	T_{STG}/T_J	-40 to +125	℃

ELECTRICAL CHARACTERISTICS

PAPRAMETERS	SYMBOLS	TEST CONDITIONS		VALUE		UNITS
				LLDB3	LLDB4	
Breakover Voltage*	V_{BO}	C=22nf** See Diagram 1	Min	28	35	V
			Typ	32	45	
			Max	36	45	
Breakover Voltage Symmetry	1+V_{BO}I- 1-V_{BO}I	C=22nf** See Diagram 1	Max	±3		V
Dynamic Breakover Voltage	1±△V1	△I=(I_{BO} to IF=10mA) See FIG 1	Min	5		V
Output Voltage*	V_O	See FIG 2	Min	5		V
Breakover Current*	I_{BO}	C=22nf**	Max	100		uA
Rise Time*	tr	See FIG 3	Typ	1.5		uS
Leakage Current*	I_B	I_B=0.5 V_{BO} MAX See FIG 3	Max	10		uA

NOTE:* Electrical characteristics applicable in both forward and reverse directions.

** Connected in parallel with the devices.

LLDB3/LLDB4

FIG.1-CURRENT-VOLTAGE CHARACTERISTICS

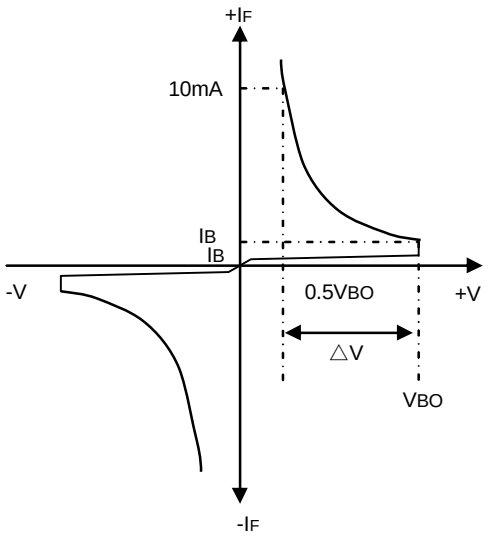


FIG.2-TEST CIRCUIT FOR OUTPUT VOLATGE

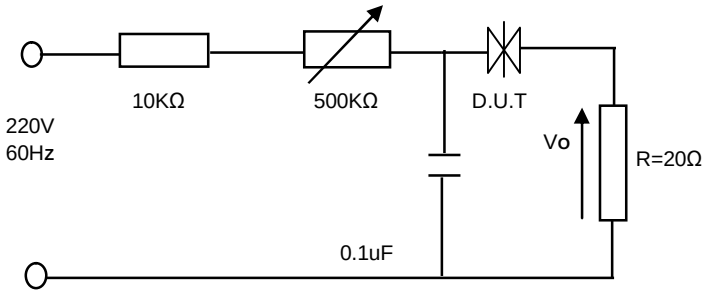


FIG.3-TEST CIRCUIT SEE FIG.2 ADJUST R
FOR Ip=0.5A

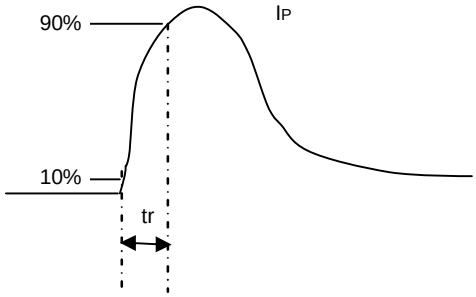


FIG.4-TEST CIRCUIT FOR OUTPUT

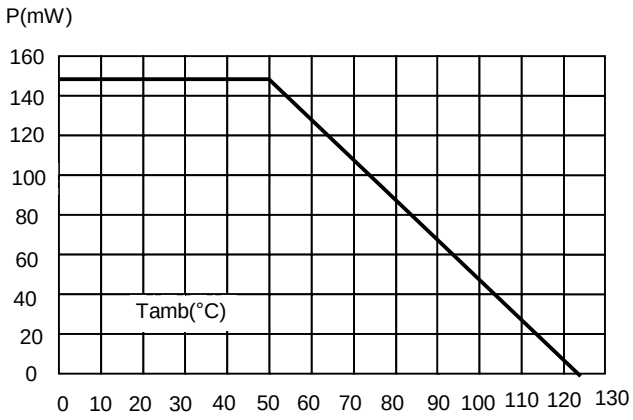


FIG.5-RELATIVE VARIATION OF VBO VERSUS
JUNCTION TEMPERATURE(TYPICAL VALUES)

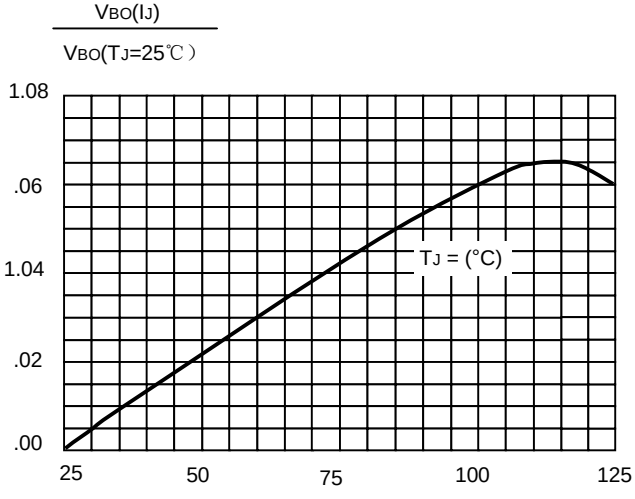


FIG.6-PEAK PULSE CURRENT VERSUS PULSE
DURATION (MAXIMUM VALUES)