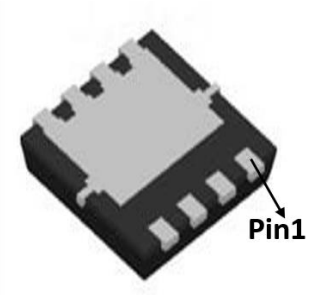
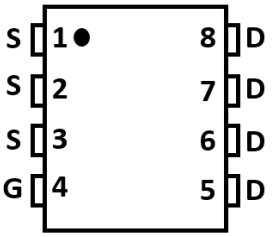
SKQ50N03BD

N-Channel Enhancement Mode Field Effect Transistor

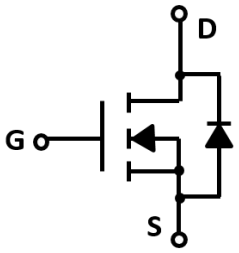
Product Summary

- V_{DS} 30V
- I_D 50A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜6.0 mohm
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜8.0 mohm
- 100% UIS Tested
- 100% ▽V_{DS} Tested





DFN3.3X3.3



General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

- High current load applications
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply
- **Marking**: Q50N03B

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	30	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_C=25℃	I_D	50	A
	T_C=100℃		35	
Pulsed Drain Current [A]		I_{DM}	190	A
Total Power Dissipation	T_C=25℃	P_D	30	W
	T_C=100℃		15	W
Single Pulse Avalanche Energy [B]		E_{AS}	225	mJ
Thermal Resistance Junction-to-Case [C]		$R_{\theta JC}$	5	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+175	℃

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D=15A		4.9	6.0	mΩ
		V_{GS}= 4.5V, I_D=15A		6.3	8.0	
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V			1.2	V
Maximum Body-Diode Continuous Current	I_S				50	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=15V,V_{GS}=0V,f=1MHZ		2150		pF
Output Capacitance	C_{oss}			435		
Reverse Transfer Capacitance	C_{rss}			252		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=15V,I_D=20A		52.8		nC
Gate-Source Charge	Q_{gs}			12.3		
Gate-Drain Charge	Q_{gd}			10.8		
Reverse Recovery Chrage	Q_{rr}	I_F=25A, di/dt=100A/us		28		
Reverse Recovery Time	t_{rr}			27		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=20V, I_D=4A,R_L=1Ω R_{GEN}=3Ω		9		
Turn-on Rise Time	t_r			15.5		
Turn-off Delay Time	$t_{D(off)}$			29		
Turn-off fall Time	t_f			9		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. T_j=25℃, V_{DS}=30V V_{DD}=25V V_{GS}=10V L=1mH.

C. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

Typical Performance Characteristics

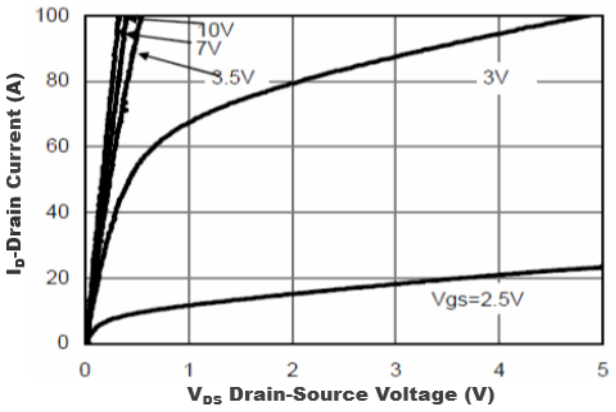


Figure1. Output Characteristics

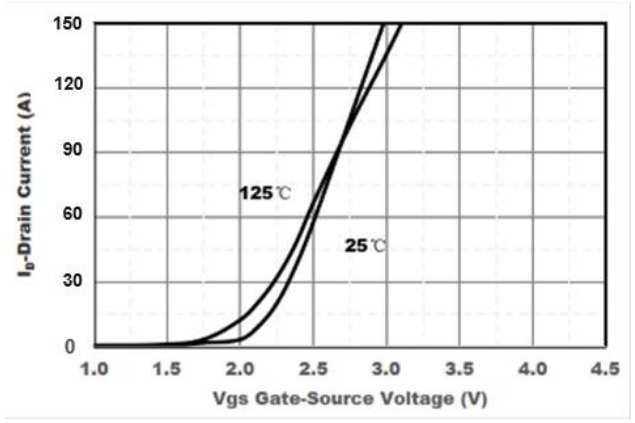


Figure2. Transfer Characteristics

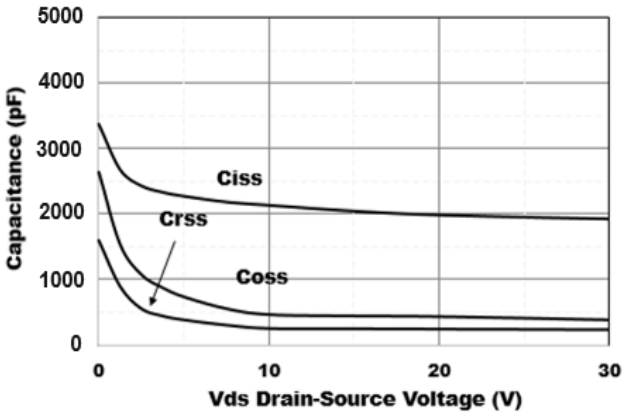


Figure3. Capacitance Characteristics

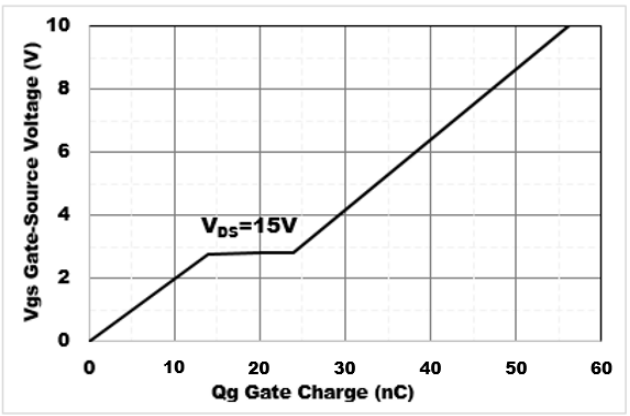


Figure4. Gate Charge

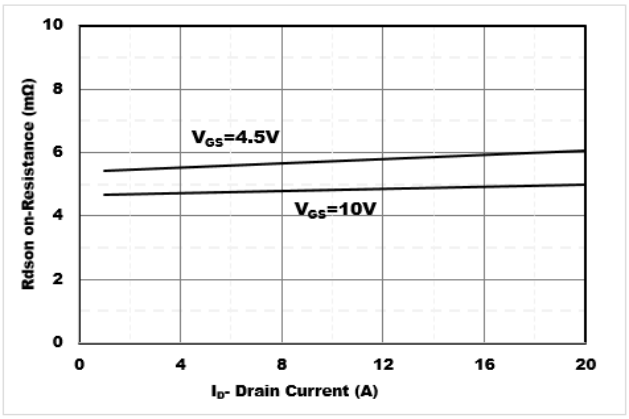


Figure5. Drain-Source on Resistance

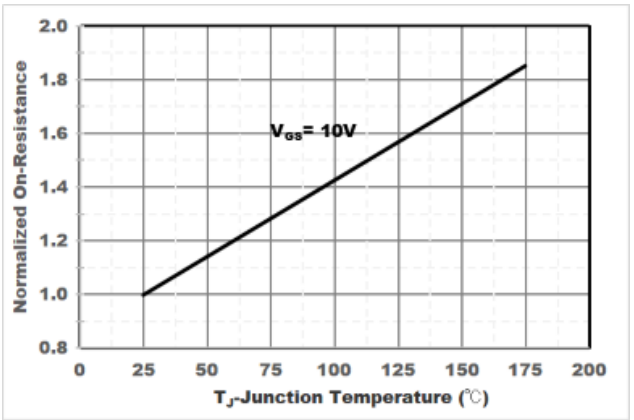


Figure6. Drain-Source on Resistance

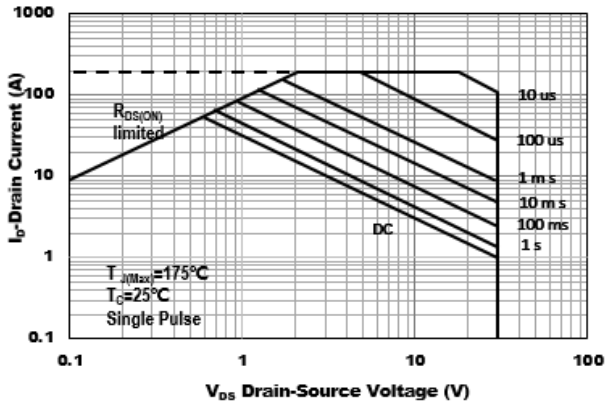


Figure7. Safe Operation Area

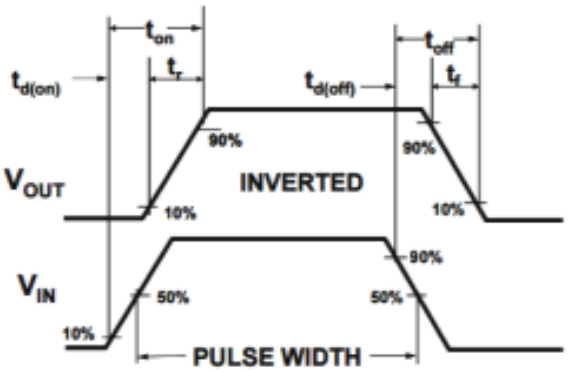
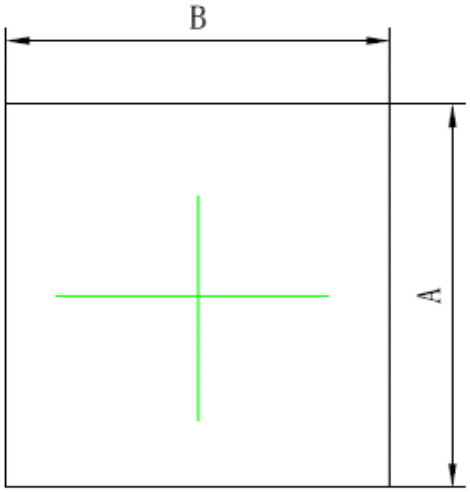
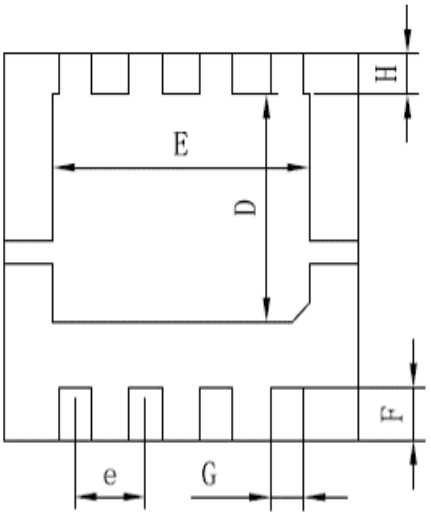


Figure8. Switching wave

DFN3.3X3.3 Package information





A	B	C	C1
3.25±0.05	3.25±0.05	0.8±0.05	0.2±0.02
C2	D	E	F
0.05Max	1.9±0.1	2.35±0.15	0.45±0.05
G	H	e	
0.3±0.05	0.35±0.05	0.65±0.05	
： mm