PL133-37

Low-Power, 1.62V to 3.63V, 1 MHz to 150 MHz, Inverting 1:3 Fanout Buffer IC

Features

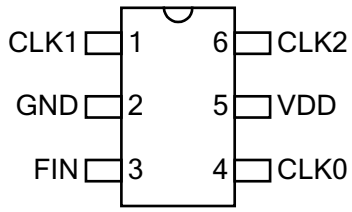
- 3 LVCMOS Inverted Outputs
- 12 mA Output Drive Strength
- Input/Output Frequency:
  - Reference Clock: 1 MHz to 150 MHz
- Supports LVCMOS or Sine Wave Input Clock
- Very Low Jitter and Phase Noise
- Low Current Consumption
- Single 1.8V, 2.5V, or 3.3V ±10% Power Supply
- Operating Temperature Range
  - 0°C to +70°C (Commercial)
  - –40°C to +85°C (Industrial)
- Available in 6-Lead SOT23 GREEN/RoHS-Compliant Package

General Description

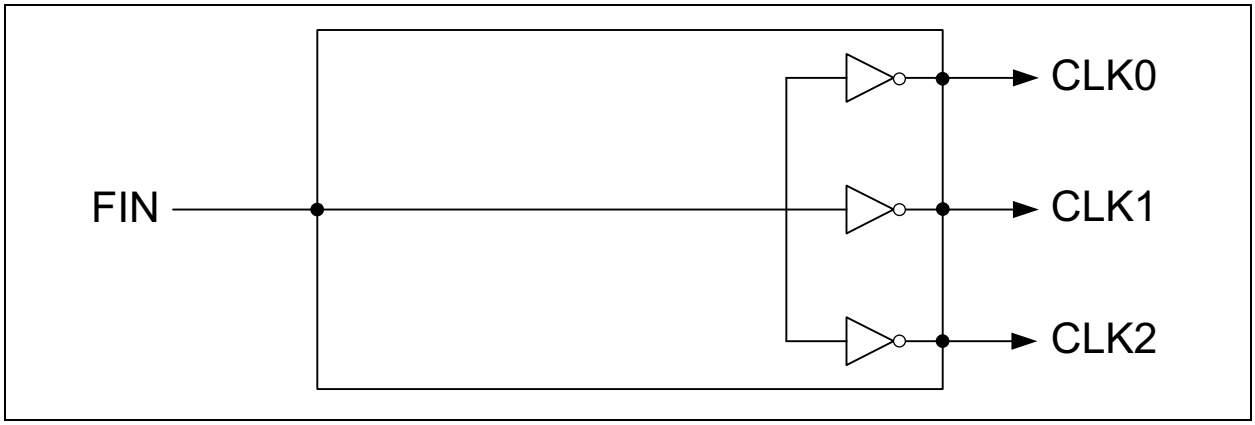
The PL133-37 is an advanced fanout buffer design for high performance, low-power, small form-factor applications. The PL133-37 accepts a reference clock input of 1 MHz to 150 MHz and produced three inverted outputs of the same frequency. Reference clock inputs may be LVCMOS or sine-wave signals (the inputs are internally AC-coupled). Offered in a small 3 mm x 3 mm 6-lead SOT23, the PL133-37 offers the best phase noise, jitter performance, and lowest power consumption of any comparable IC.

Package Type

PL133-37
6-Lead SOT23 (T)
(Top View)



Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{DD}) ..... –0.5V to +4.6V
DC Input Voltage (V_I) ..... –0.5V to V_{DD} + 0.5V
DC Output Voltage (V_O) ..... –0.5V to V_{DD} + 0.5V
Storage Temperature (T_S) ..... –65°C to +150°C
Ambient Operating Temperature (Note 1) ..... –40°C to +85°C

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

AC SPECIFICATIONS

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Frequency	f_{IN}	1	—	150	MHz	2.5V and 3.3V operation
		1	—	100	MHz	1.8V operation
Input Signal Amplitude	f_{IN}	0.8	—	V_{DD}	V_{PP}	Internally AC-coupled, ≤150 MHz, V_{DD} = 2.5V and 3.3V
		0.5	—	V_{DD}	V_{PP}	Internally AC-coupled, ≤100 MHz, All V_{DD}s
		0.1	—	V_{DD}	V_{PP}	Internally AC-coupled, 3.3V ≤50 MHz, 2.5V ≤40 MHz, 1.8V ≤15 MHz,
Output Enable Time	t_{EN}	—	—	10	ns	OE function, T_A = +25°C, 15 pF load
Output Rise Time	t_r	—	2	3	ns	15 pF load, 10/90% V_{DD}, 3.3V
Output Fall Time	t_f	—	2	3	ns	15 pF load, 10/90% V_{DD}, 3.3V
Duty Cycle	—	45	50	55	%	Input duty cycle is 50%
Output-to-Output Skew	t_{OOSK}	—	—	250	ps	All outputs equally loaded

DC SPECIFICATIONS

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Current, Dynamic	I_{DD}	—	1.2	—	mA	V_{DD} = 3.3V, 25 MHz, no load
		—	0.9	—	mA	V_{DD} = 2.5V, 25 MHz, no load
		—	0.6	—	mA	V_{DD} = 1.8V, 25 MHz, no load
Supply Current, Standby	I_{DD_SB}	—	0.3	—	mA	OE pin pulled low, V_{DD} = 3.3V
Operating Voltage	V_{DD}	1.62	—	3.63	V	—
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 12 mA, V_{DD} = 3.3V
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OL} = –12 mA, V_{DD} = 3.3V
Output Current	I_{OSD}	12	—	—	ma	V_{OL} = 0.4V, V_{OH} = 2.4V, V_{DD} = 3.3V

NOISE CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Additive Phase Jitter	t_{JITTER}	—	70	—	fs	V_{DD} = 3.3V, Frequency = 26 MHz, Offset = 12 kHz ~ 5 MHz
		—	80	—	fs	V_{DD} = 3.3V, Frequency = 100 MHz, Offset = 12 kHz ~ 20 MHz

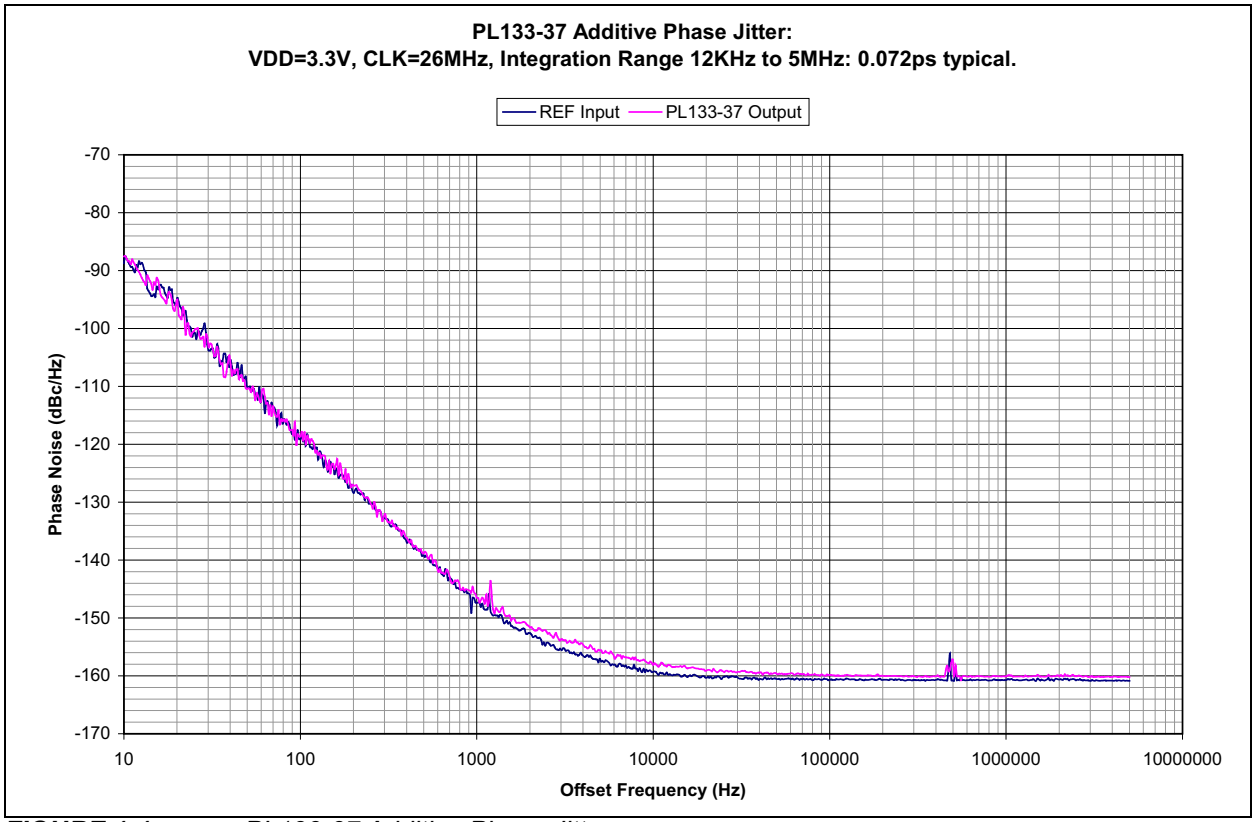


FIGURE 1-1: *PL133-37 Additive Phase Jitter.*

When a buffer is used to pass a signal, the buffer adds a little bit of its own noise. The phase noise on the output of the buffer will be a little bit more than the phase noise in the input signal. To quantify the noise addition in the buffer, we compare the phase jitter numbers from the input and the output. The difference is called Additive Phase Jitter. The formula for additive phase jitter is as follows:

EQUATION 1-1:

$$\text{Additive Phase Jitter} = \sqrt{\text{Output Phase Jitter}^2 - \text{Input Phase Jitter}^2}$$

2.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Pin Type	Description
1	CLK1	O	Output clock (inverted).
2	GND	P	Ground connection.
3	FIN	I	Reference clock input.
4	CLK0	O	Output clock (inverted).
5	VDD	P	Power supply.
6	CLK2	O	Output clock (inverted).

LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance-optimized PCB design.

Signal Integrity and Termination Considerations

- Keep traces short.
- Trace = Inductor. With a capacitive load, this equals ringing.
- Long trace = Transmission line. Without proper termination, this will cause reflections that look like ringing.
- Design long traces as striplines or microstrips with defined impedance.
- Match trace at one side to avoid reflections bouncing back and forth.

Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the VDD pin to limit noise from the power supply.
- Multiple VDD pins should be decoupled separately for best performance.
- The addition of a ferrite bead in series with VDD can help prevent noise from other board sources.
- The value of the decoupling capacitor is frequency dependent. The typical value to use is 0.1 µF.

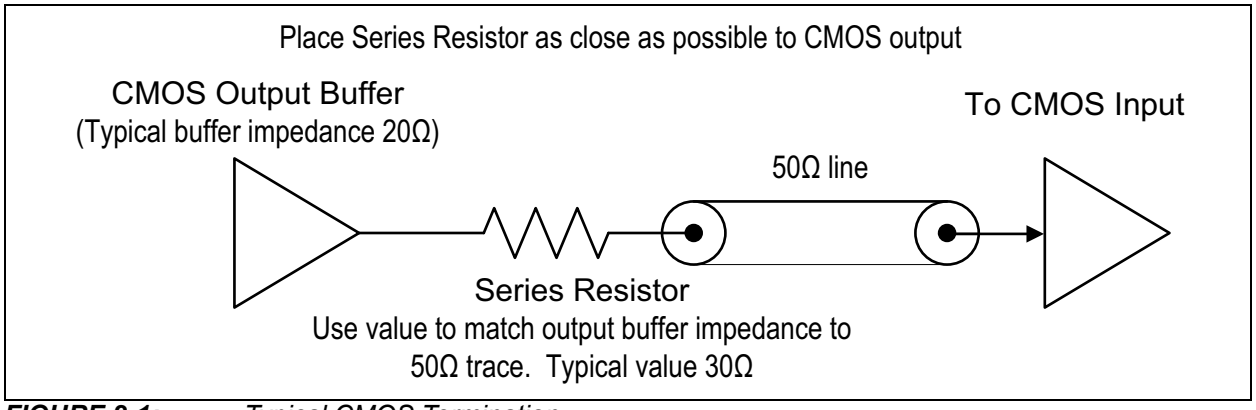
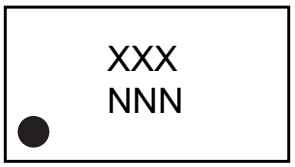


FIGURE 2-1: *Typical CMOS Termination.*

3.0 PACKAGING INFORMATION

3.1 Package Marking Information

6-Lead SOT23*



Example

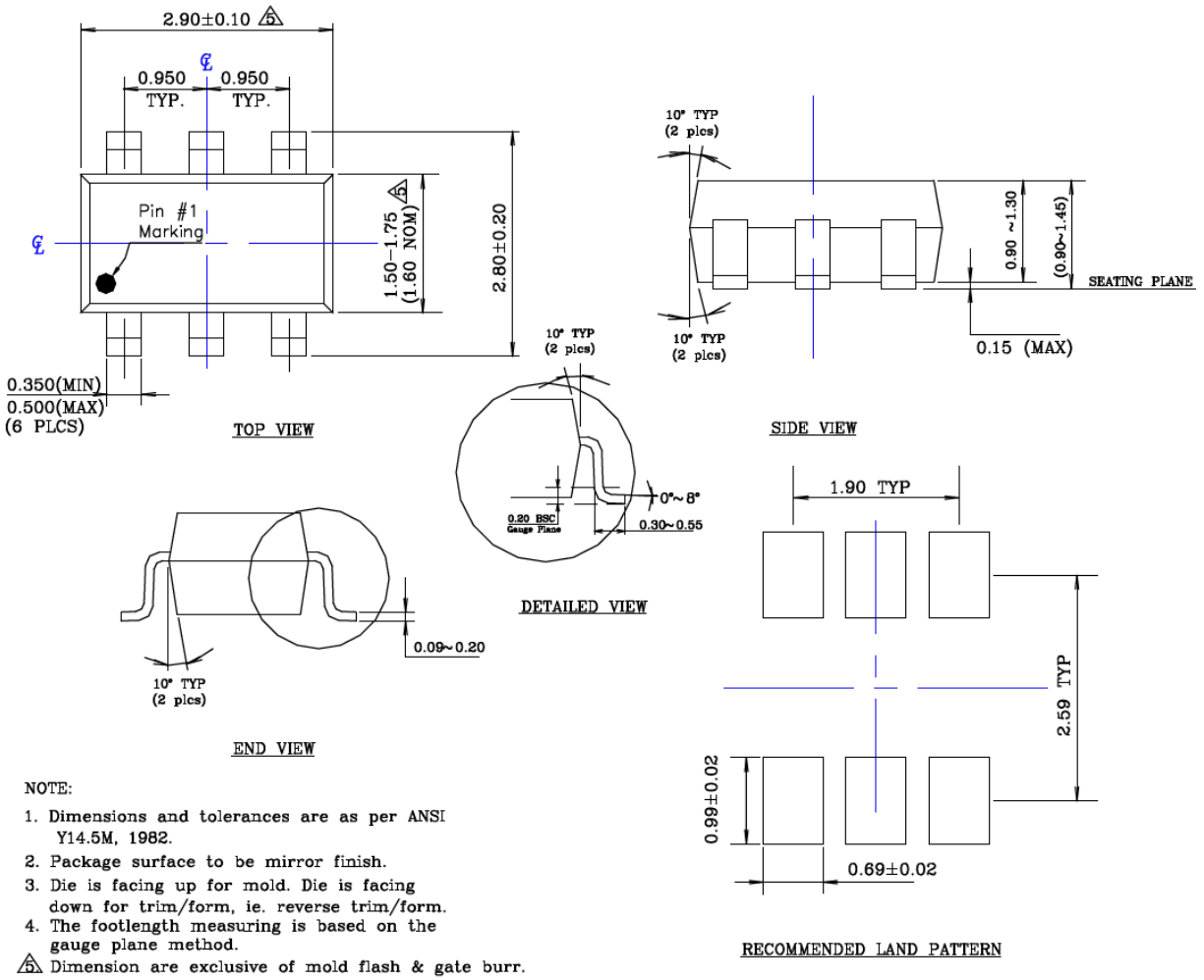
Note: Industrial temperature versions of this part contain a capital letter “I” after the alphanumerical traceability code.

Legend:	XX...X	Product code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

6-Lead SOT23 Package Outline and Recommended Land Pattern

TITLE
6 LEAD SOT23 PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	SOT23-6LD-PL-1	UNIT	MM



NOTE:

1. Dimensions and tolerances are as per ANSI Y14.5M, 1982.
2. Package surface to be mirror finish.
3. Die is facing up for mold. Die is facing down for trim/form, ie. reverse trim/form.
4. The footlength measuring is based on the gauge plane method.

5 Dimension are exclusive of mold flash & gate burr.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

APPENDIX A: REVISION HISTORY

Revision A (September 2020)

- Converted Micrel document PL133-37 to Microchip data sheet template DS20006403A.
- Minor grammatical text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	-X
Device	Package	Temperature Range	Media Type

Device:	PL133-37:	Low-Power, 1.62V to 3.63V, 1 MHz to 150 MHz, Inverting 1:3 Fanout Buffer IC	
Package:	T	=	6-Lead 3 mm x 3 mm SOT23
Temperature Range:	C	=	0°C to +70°C
	I	=	–40°C to +85°C
Media Type:	(blank)	=	20/Bag
	R	=	3,000/Reel

Examples:

a) PL133-37TC: PL133-37, 6-Lead SOT23, 0°C to +70°C Temperature Range, 20/Bag

b) PL133-37TC-R: PL133-37, 6-Lead SOT23, 0°C to +70°C Temperature Range, 3,000/Reel

c) PL133-37TI: PL133-37, 6-Lead SOT23, –40°C to +85°C Temperature Range, 20/Bag

d) PL133-37TI-R: PL133-37, 6-Lead SOT23, –40°C to +85°C Temperature Range, 3,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
- Microchip is willing to work with any customer who is concerned about the integrity of its code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable." Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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ISBN: 978-1-5224-6699-4