NCP1589C

Low Voltage Synchronous Buck Controller

The NCP1589C is a low cost PWM controller designed to operate from a 5 V or 12 V supply. This device is capable of producing an output voltage as low as 0.8 V. This device is capable of converting voltage from as low as 2.5 V. This 10−pin device provides an optimal level of integration to reduce size and cost of the power supply. Features include a 1.5 A gate driver design and an internally set 300 kHz oscillator. In addition to the 1.5 A gate drive capability, other efficiency enhancing features of the gate driver include adaptive non−overlap circuitry. The NCP1589C also incorporates an externally compensated error amplifier. Protection features include programmable short circuit protection and undervoltage lockout (UVLO).

Features

- V_{CC} Range from 4.5 V to 13.2 V
- 300 kHz Internal Oscillator
- Boost Pin Operates to 30 V
- Voltage Mode PWM Control
- Precision 0.8 V Internal Reference
- Adjustable Output Voltage
- Internal 1.5 A Gate Drivers
- 80% Max Duty Cycle
- Input Under Voltage Lockout
- Programmable Current Limit
- This is a Pb−Free Device

Applications

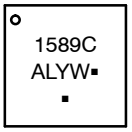
- Graphics Cards
- Desktop Computers
- Servers / Networking
- DSP & FPGA Power Supply
- DC−DC Regulator Modules

ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM

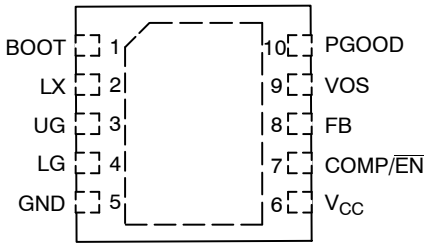
DFN10
CASE 485C



1589C	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Device

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1589CMNTWG	DFN10 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

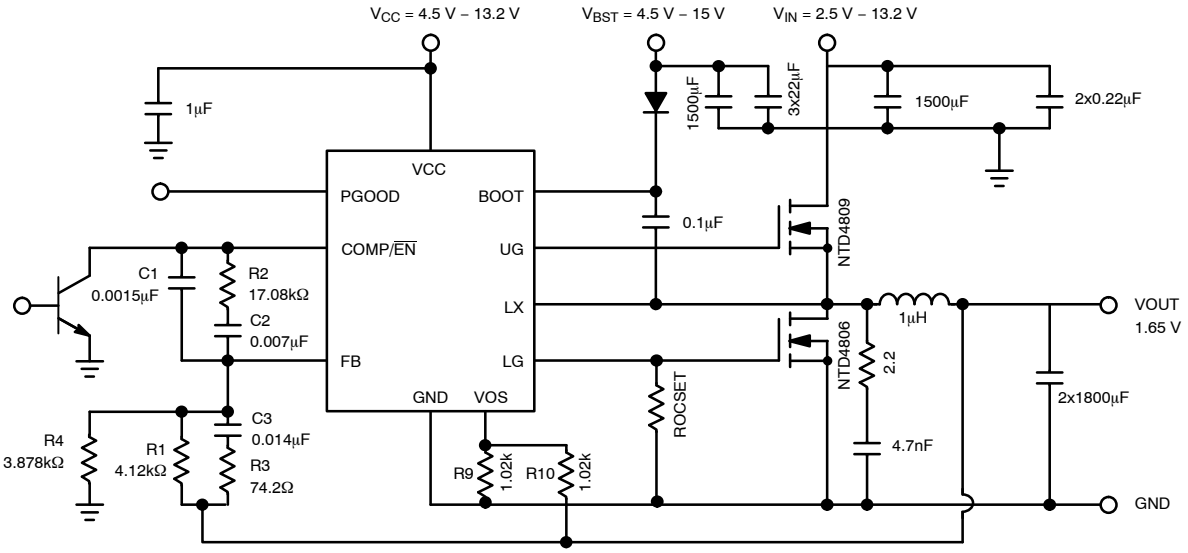


Figure 1. Typical Application Diagram

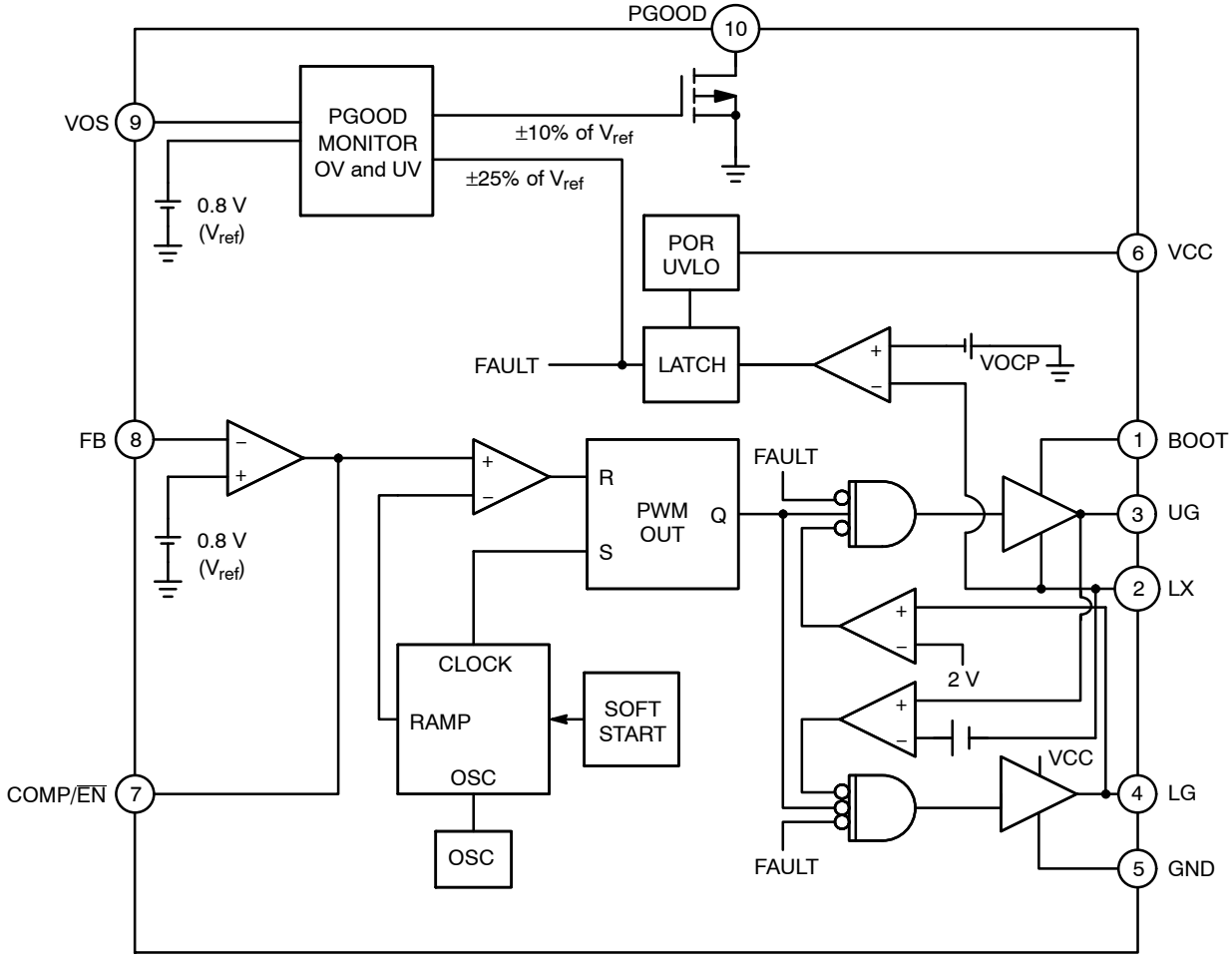


Figure 2. Detailed Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Description
1	BOOT	Supply rail for the floating top gate driver. To form a boost circuit, use an external diode to bring the desired input voltage to this pin (cathode connected to BOOT pin). Connect a capacitor (C_{BOOT}) between this pin and the LX pin. Typical values for C_{BOOT} range from 0.1 μF to 1 μF. Ensure that C_{BOOT} is placed near the IC.
2	LX	Switch node pin. This is the reference for the floating top gate driver. Connect this pin to the source of the top MOSFET.
3	UG	Top gate MOSFET driver pin. Connect this pin to the gate of the top N−channel MOSFET.
4	LG	Bottom gate MOSFET driver pin. Connect this pin to the gate of the bottom N−channel MOSFET.
5	GND	IC ground reference. All control circuits are referenced to this pin.
6	VCC	Supply rail for the internal circuitry. Operating supply range is 4.5 V to 13.2 V. Decouple with a 1 μF capacitor to GND. Ensure that this decoupling capacitor is placed near the IC.
7	COMP/$\overline{EN}$	Compensation Pin. This is the output of the error amplifier (EA) and the non−inverting input of the PWM comparator. Use this pin in conjunction with the FB pin to compensate the voltage−control feedback loop. Pull this pin low for disable.
8	FB	This pin is the inverting input to the error amplifier. Use this pin in conjunction with the COMP pin to compensate the voltage−control feedback loop. Connect this pin to the output resistor divider (if used) or directly to V_{out}.
9	VOS	Voltage Offset Sense
10	PGOOD	Power Good output. Pulled Low if VOS is ±10% of 0.8 V V_{ref}.

ABSOLUTE MAXIMUM RATINGS

Pin Name	Symbol	V_{MAX}	V_{MIN}
Main Supply Voltage Input	VCC	15 V	−0.3 V
Bootstrap Supply Voltage Input	BOOT	35 V wrt/GND 40 V < 100 ns 15 V wrt/LX	−0.3 V −0.3 V −0.3 V
Switching Node (Bootstrap Supply Return)	LX	35 V 40 V for < 100 ns	−5 V −10 V for < 200 ns
High−Side Driver Output (Top Gate)	UG	30 V wrt/GND 15 V wrt/LX 40 V for < 100 ns	−0.3 V wrt/LX −2 V for < 200 ns
Low−Side Driver Output (Bottom Gate)	LG	V_{CC} + 0.3 V	−0.3 V −5 V for < 200 ns
Feedback, VOS	FB, VOS	5.0 V	−0.3 V
COMP/$\overline{EN}$	COMP/$\overline{EN}$	3.6 V	−0.3 V
PGOOD	PGOOD	7 V	−0.3 V

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	165	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	45	°C/W
Operating Junction Temperature Range	T_J	−20 to 150	°C
Operating Ambient Temperature Range	T_A	−20 to 70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Moisture Sensitivity Level	MSL	1	−

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
This device is ESD sensitive. Use standard ESD precautions when handling.

ELECTRICAL CHARACTERISTICS (T_A = 25°C; 4.5 V < [BST−PHASE] < 13.2 V, 4.5 V < BST < 30 V, 0 V < PHASE < 21 V, C_{TG} = C_{BG} = 1.0 nF, for min/max values unless otherwise noted.)

Characteristic	Conditions	Min	Typ	Max	Unit
Input Voltage Range		4.5		13.2	V
Boost Voltage Range	13.2 V wrt LX	4.5		30	V
Supply Current					
Quiescent Supply Current	V_{FB} = 1.0 V, No Switching, V_{CC} = 13.2 V	1.0		8.0	mA
Boost Quiescent Current	V_{FB} = 1.0 V, No Switching	0.1			μA
Undervoltage Lockout					
UVLO Threshold	V_{CC} Rising	3.8	4.0	4.2	V
UVLO Threshold	V_{CC} Falling	3.4	3.6	3.8	V
UVLO Hysteresis	V_{CC} Rising or V_{CC} Falling		0.4		V
Switching Regulator					
VFB Feedback Voltage	(FB Tied to Comp. Measure FB Pin.)	0.7936	0.8	0.8064	V
Oscillator Frequency		270	300	330	kHz
Ramp−Amplitude Voltage			1.1		V
Minimum Duty Cycle			0		%
Maximum Duty Cycle		70	75	80	%
LG Minimum on Time			500		ns
Error Amplifier					
Open Loop DC Gain (Note 1)		70	80		dB
Output Source Current Output Sink Current	V_{fb} < 0.8 V V_{fb} > 0.8 V	2.0 2.0			mA
Input Offset Voltage (Note 1)		−2.0	0	2.0	mV
Input Bias Current			0.1	1.0	μA
Unity Gain Bandwidth (Note 1)		15			Mhz
Disable Threshold		0.6	0.8		V
Output Source Current During Disable			10	40	μA
Gate Drivers					
Upper Gate Source	V_{CC} = 5 V, VUG − VLX = 2.5 V	1.5			A
Upper Gate Sink			1.4		Ω
Lower Gate Source		1.5			A
Lower Gate Sink	V_{CC} = 12 V		1.0		Ω
UG Falling to LG Rising Delay	V_{CC} = 12 V, UG−LX < 2.0 V, LG > 2.0 V	12.4	18		ns
LG Falling to UG Rising Delay	V_{CC} = 12 V, LG < 2.0 V, UG > 2.0 V	12.4	18		ns
Soft−Start					
Soft−Start time		3.0		7.0	ms
Power Good					
Output Voltage	Logic Low, Sinking 4 mA			0.4	V
OVP Threshold to PGOOD Output Low	Ramp VOS from 0.7 to 1.2. Monitor when PGOOD goes Low		0.88	1.0	V
OVP Threshold to Part Disable	Ramp VOS from 0.8 to 1.2. Monitor when outputs disable		1.0	1.2	V
UVP Threshold to PGOOD Output Low	Ramp VOS from 800 mV to 500 mV. Monitor when PGOOD goes Low	0.65	0.72		V
UVP Threshold to Part Disable	Ramp VOS from 800 mV to 500 mV. Monitor when utputs stop switching	0.5	0.6		V
Overcurrent Protection					
OC Current Source (Note 1)	Sourced from LG pin, before SS	9.0	10	11	μA

1. Guaranteed by design but not tested in production.

TYPICAL CHARACTERISTICS

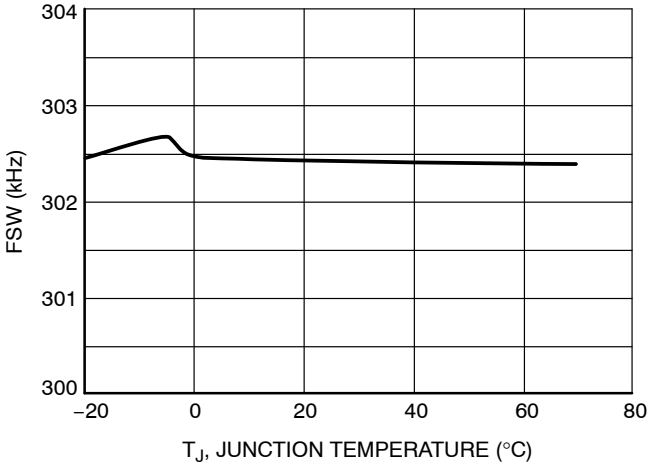


Figure 3. Oscillator Frequency

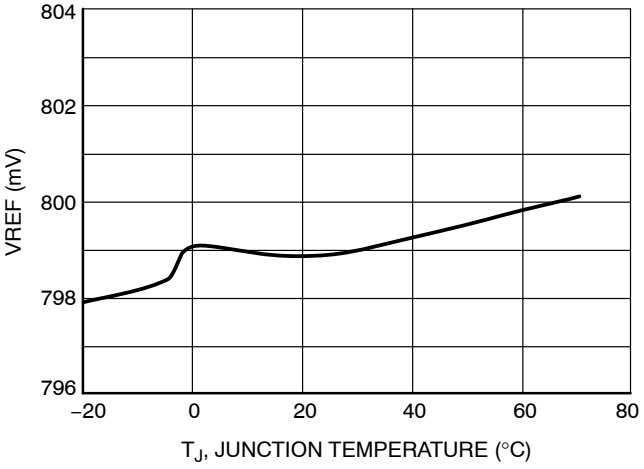


Figure 4. Reference Voltage

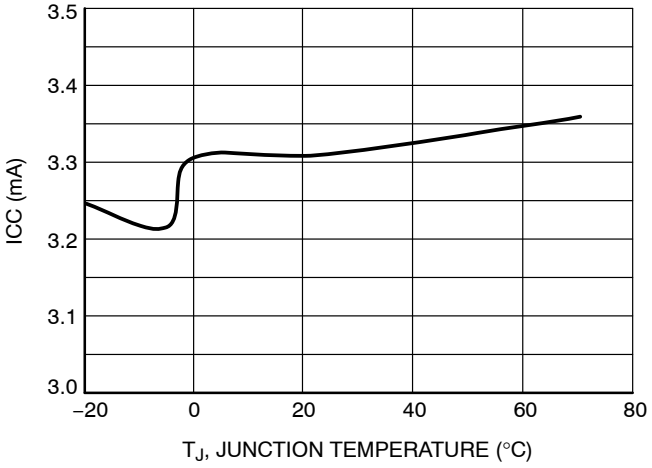


Figure 5. ICC, VCC = 13.2 V

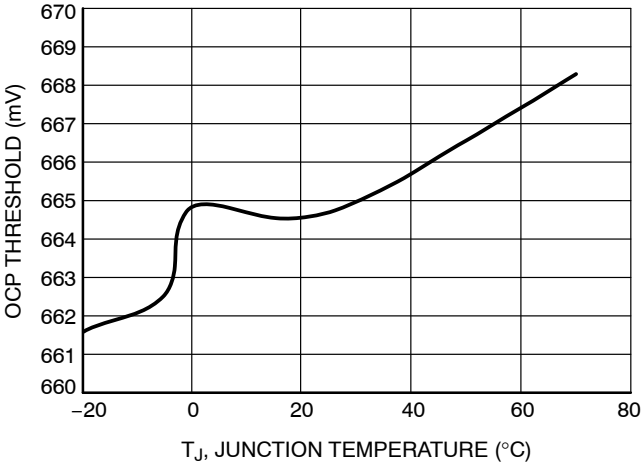


Figure 6. OCP Threshold, LG Open

APPLICATIONS INFORMATION

Over Current Protection (OCP)

The NCP1589C monitors the voltage drop across the low side mosfet and uses this information to determine if there is excessive output current. The voltage across the low side mosfet is measured from the LX pin, and is referenced to ground. The over current measurement is timed to occur at the end of the low side mosfet conduction period, just before the bottom mosfet is turned off.

If the voltage drop across the bottom mosfet exceeds the over current protection threshold, then an internal counter is incremented. If the voltage drop does not exceed the over current protection threshold, then the internal counter is reset. The NCP1589C will latch the over current protection fault condition only if the over current protection threshold is exceeded for four consecutive cycles.

When the NCP1589C latches an over current protection fault, both the high side and low side mosfets are turned off. To reset the over current protection fault, the power to the VCC pin must be cycled.

The over current threshold voltage can be externally, by varying the value of the ROCSET resistor. The ROCSET resistor is a resistor connected between the LG pin (low side mosfet gate) and ground.

During startup, after the VCC and BOOT pins reach the under voltage lock out threshold, the NCP1589C will source 10 μA of current out of the LG pin. This current will flow through the ROCSET resistor and produce a voltage that is sampled and then used as the over current protection threshold voltage. For example, if ROCSET is set to 10 kΩ, the 10 μA of current will yield a 100 mV threshold, and if the voltage drop across the low side mosfet exceeds 100 mV at the end of its conduction period, then an over current event will be detected.

If the ROCSET resistor is not present, then the over current protection threshold will max out at 640 mV. The valid range for ROCSET is 5 kΩ to 55 kΩ which yields a threshold voltage range of 50 mV to 550 mV.

Internal Soft-Start

To prevent excess inrush current during startup, the NCP1589C uses a calibrated current source with an internal soft start capacitor to ramp the reference voltage from 0 to 800 mV over a period of 4 ms. The softstart ramp generator will reset if the input power supply voltages reach the under voltage lockout threshold, or if the NCP1589C is disabled by having the COMP pin pulled low.

Startup into a Precharged Load

During a startup and soft start sequence the NCP1589C will detect a residual charge on the output capacitors and not forcefully discharge the capacitors before beginning the softstart sequence, instead, the softstart ramping of the output will begin at the voltage level of the residual charge. For example, if the NCP1589C is configured to provide a regulated output voltage of 2.5 V, the normal softstart sequence will ramp the output voltage from 0 to 2.5 V in 4.2 ms; however if the output capcitors already have a 1.2 V charge on them, the NCP1589C will not discharge the capacitors, instead the softstart sequence will begin at 1.2 V and then ramp the output to 2.5 V.

Power Good

The PGOOD pin is an open drain active high output pin that signals the condition of the VOS (Voltage Output Sense) pin. PGOOD is pulled low during soft start cycle, and if there is a latched over current, over voltage, or under voltage fault. If the voltage on the VOS pin is within ±10% of Vref (800 mV) then the PGOOD pin will not be pulled low. The PGOOD pin does not have an internal pull-up resistor.

Overvoltage Protection

If the voltage on the VOS pin exceeds the over voltage threshold the NCP1589C will latch an over voltage fault. During an over voltage fault the UG pin will be pulled low, and the LG pin will be high while the until the voltage on the VOS pin goes below $V_{ref}/2$ (400 mV). The NCP1589C will continue drive the LG pin, LG will go high if VOS exceeds 1 V and then go low when VOS goes below 400 mV. The power to the NCP1589C must be cycled to reset the over voltage protection fault.

Under Voltage Protection

If the voltage on the VOS pin falls below the under voltage threshold after the soft start cycle completes, then the NCP1589C will latch an under voltage fault. During an under voltage fault, both the UG and LG pins will be pulled low. The power to the NCP1589C must be cycled to reset the under voltage protection fault.

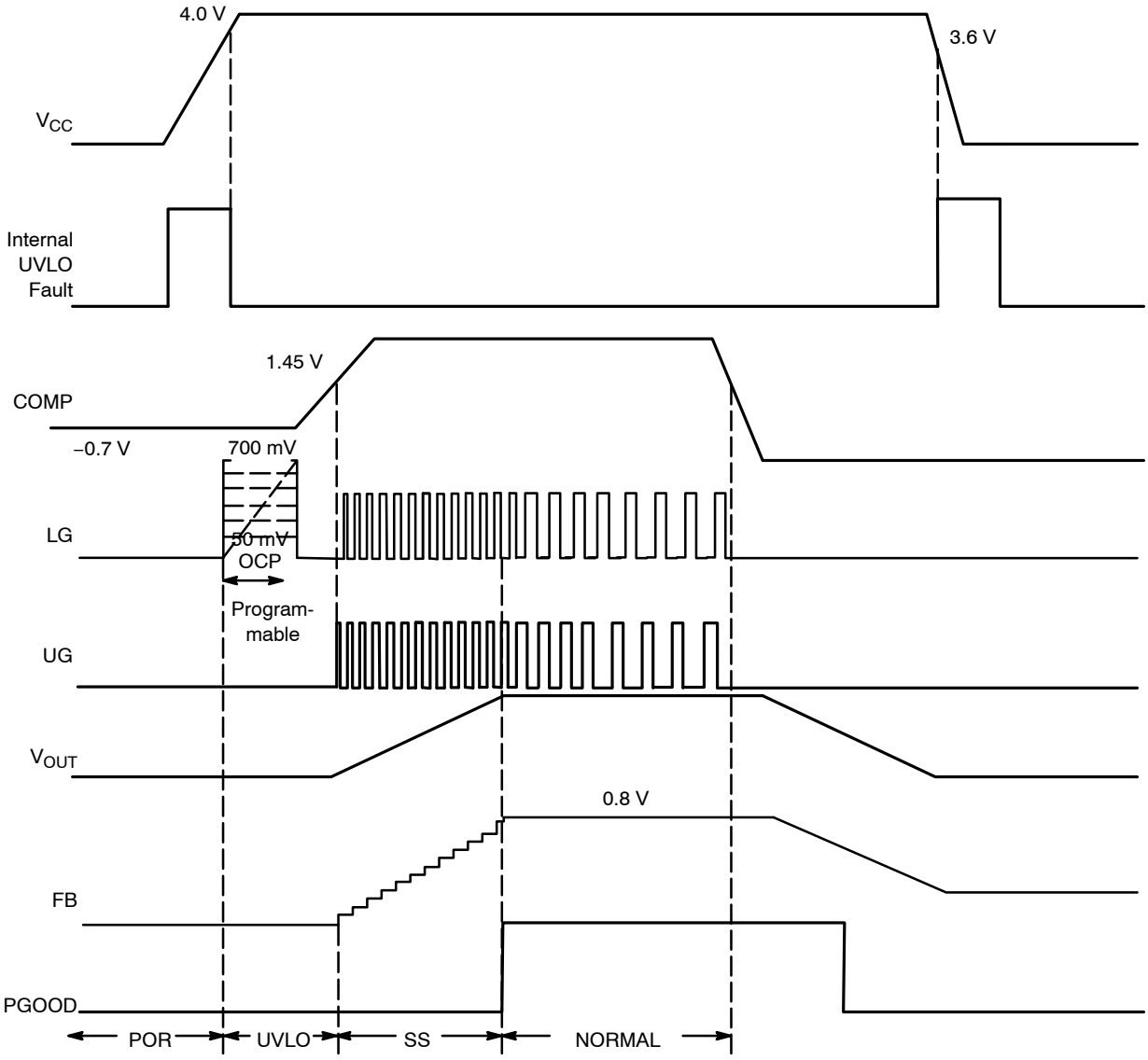


Figure 7. Typical Startup Sequence

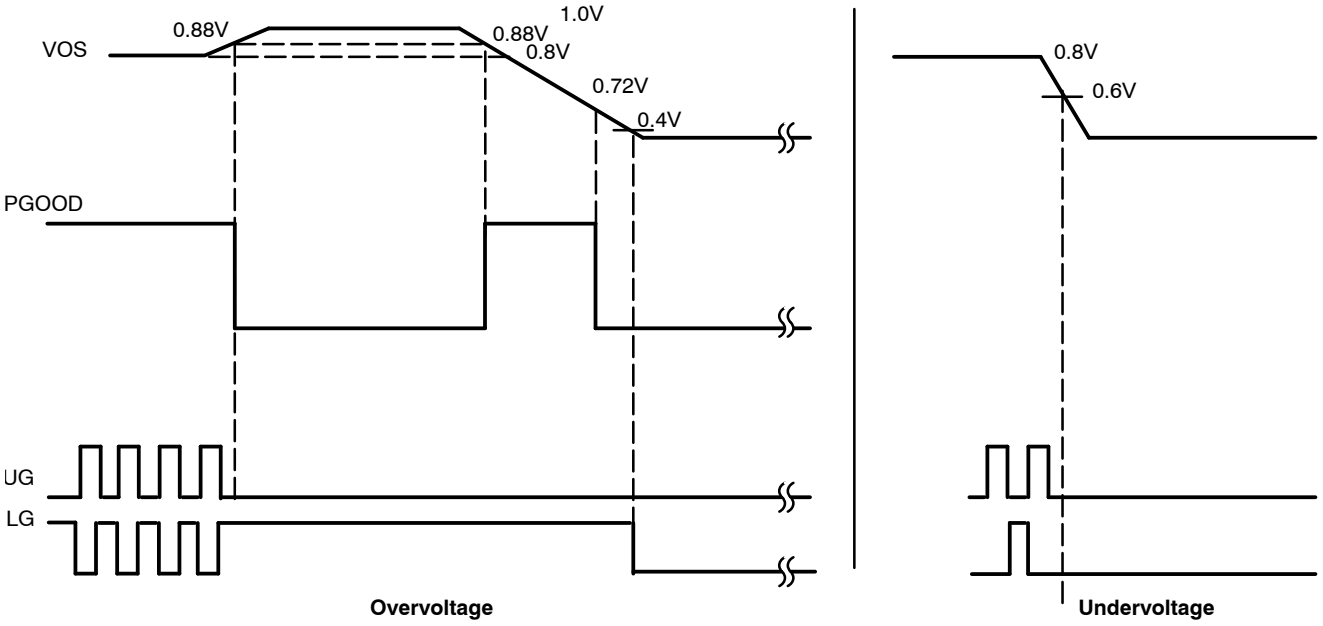


Figure 8. Typical Power Good Function

Feedback and Compensation

The NCP1589C allows the output voltage to be adjusted from 0.8 V to 5.0 V via an external resistor divider network. The controller will try to maintain 0.8 V at feedback pin. Thus, if a resistor divider circuit was placed across the feedback pin to V_{OUT}, the controller will regulate the output voltage proportional to the resistor divider network in order to maintain 0.8 V at the FB pin. The same formula applies to the VOS pin and the controller will maintain 0.8 V at the VOS pin.

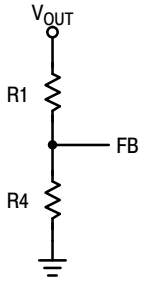


Figure 9.

The relationship between the resistor divider network above and the output voltage is shown in the following equation:

$$R_4 = R_1 \times \left(\frac{V_{REF}}{V_{OUT} - V_{REF}}\right)$$

The same formula can be applied to the feedback resistors at VOS.

$$R_9 = R_{10} \times \left(\frac{V_{REF}}{V_{OUT} - V_{REF}}\right)$$

Design Example

Voltage Mode Control Loop with TYPE III Compensation

Converter Parameters:

Input Voltage: V_{IN} = 5 V
Output Voltage: V_{OUT} = 1.65 V
Switching Frequency: 300 kHz
Total Output Capacitance: C_{OUT} = 3600 μF
Total ESR: ESR = 6 mΩ
Output Inductance: L_{OUT}: 1 μH
Ramp Amplitude: V_{RAMP} = 1.1 V

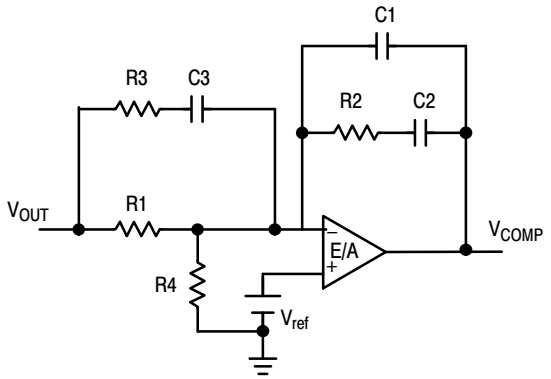


Figure 10.

a.. Set a target for the close loop bandwidth at $1/6^{th}$ of the switching frequency.

$F_{cross\_over} := 50$ kHz

b.. Output Filter Double Pole Frequency

$$F_{lc} := \frac{1}{2 \cdot \pi \cdot \sqrt{L_{OUT} \cdot C_{OUT}}}$$

$$F_{lc} = 2.653\ \text{kHz}$$

c.. ESR Zero Frequency:

$$F_{ESR} := \frac{1}{2 \cdot \pi \cdot C_{OUT} \cdot C_{ESR}}$$

$$F_{ESR} = 7.368\ \text{kHz}$$

Step 1: Set a value for R1 between 2 kΩ and 5 kΩ

$$R1 := 4.12\ \text{k}\Omega$$

Step 2: Pick compensation DC gain (R2/R1) for desired close loop bandwidth.

$$V_{RAMP} := 1.1\ \text{V}$$

$$R2 := R1 \cdot \left(\frac{V_{RAMP}}{V_{IN}}\right) \cdot \left(\frac{F_{cross\_over}}{F_{lc}}\right)$$

$$R2 = 17.085\ \text{k}\Omega$$

Step 3: Place 1st zero at half the output filter double pole frequency.

$$C2 := \frac{2 \cdot \sqrt{L_{OUT} \cdot C_{OUT}}}{R2}$$

$$C2 = 7.024 \times 10^{-3}\ \mu\text{F}$$

Step 4: Place 1st pole at ESR zero frequency.

$$C1 := \frac{C2}{C2 \cdot R2 \cdot 2 \cdot \pi \cdot F_{ESR} - 1}$$

$$C1 = 1.542 \times 10^{-3}\ \mu\text{F}$$

Step 5: Place 2nd zero at the output filter double pole frequency.

$$R3 := \frac{R1}{\frac{F_{SW}}{2 \cdot F_{lc}} - 1}$$

$$R3 = 74.169\ \Omega$$

Step 6: Place 2nd pole at half the switching frequency.

$$C3 := \frac{1}{\left(\pi \cdot R3 \cdot F_{SW}\right)}$$

$$C3 = 0.014\ \mu\text{F}$$

Step 7: R4 is sized to maintain the feedback voltage to V_{ref} = 0.8 V.

$$R4 := \frac{V_{REF} \cdot R1}{V_{OUT} - V_{REF}}$$

$$R4 = 3.878\ \text{k}\Omega$$

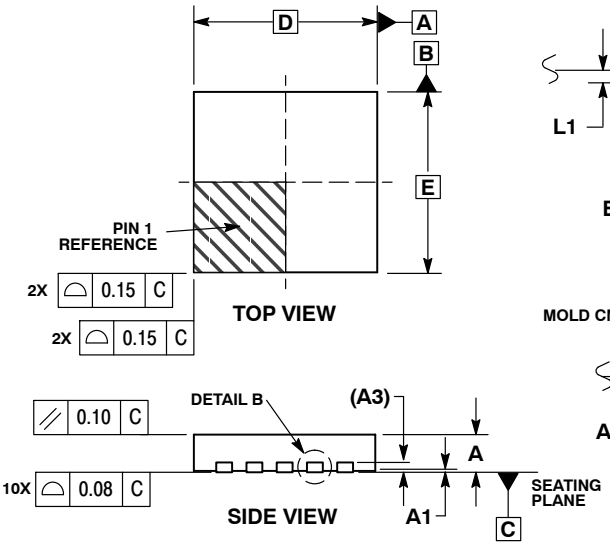
The Component values for Type III Compensation are:

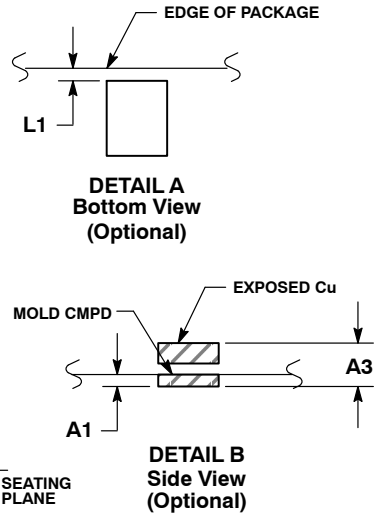
R1 = 4.12 kΩ
R2 = 17.085 kΩ
R3 = 74.169 Ω
R4 = 3.878 kΩ
C1 = 0.0015 μF
C2 = 0.007 μF
C3 = 0.014 μF

NOTE: Recommend to change values to industry standard component values.

PACKAGE DIMENSIONS

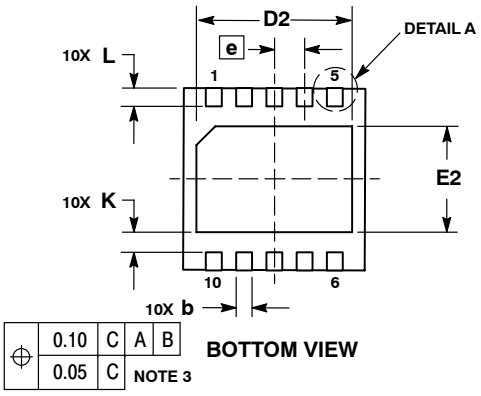
DFN10, 3x3, 0.5P
CASE 485C−01
ISSUE B



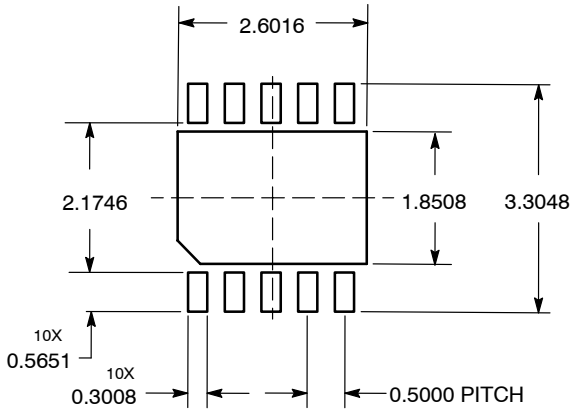


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASHING MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL b.
6. DETAILS A AND B SHOW OPTIONAL VIEWS FOR END OF TERMINAL LEAD AT EDGE OF PACKAGE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	2.40	2.60
E	3.00 BSC	
E2	1.70	1.90
e	0.50 BSC	
K	0.19 TYP	
L	0.35	0.45
L1	0.00	0.03



SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
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