FOUNDER

eMMC MKEMA008GT1E-C Datasheet

Version 01.00

Document Control Center

2020/5/28

Contents

List of Figures

List of Table

1. Foreword

This document has been produced by MK Founder Technology Co., Ltd., should the company modifies the contents of this specification, it will be re-released with an identifying change of release date and an increase in revision number as follows:

Revision mn.xy, where:

- mn the first two digit are incremented for major changes of substance, e.g., functional changes.
- xy the second two digits are incremented when minor changes have been incorporated into the specification, i.e., enhancements, corrections, updates, etc.

2. Revision History

Revision	Date	Modified By	Description
01.00	2020/05/28	Document Control Center	Preliminary version eMMC MKEMA008GT1E-C Datasheet

3. Statement of Scope

This Datasheet document is described the MK eMMC's methods and abstractions of reliability. The contents include the concept and measurement methodologies.

4. General Description

eMMC MKEMA008GT1E-C Datasheet is the MK eMMC of MK Founder Technology Co. Ltd. which is an embedded non-volatile memory system package into BGA. It has high performance, low power consumption features and supports eMMC4.5, eMMC5.01 and eMMC5.1 specifications.

4.1. Product list

Capacities	Part Number	Flash Type	User Density	Package Size (mm)	Package Type
8GB	MKEMA008GT1E-C	64Gb MLCx1	90 %	11.5x13x1.0	153FBGA

Table 4-1 eMMC product list

4.2. Feature

- Fully compatible with eMMC standard specification v4.5/v5.01/5.1
  - Support command class 0, 2, 4, 5, 6, 7, 8, 9, 10 and 11
  - Boot, RPMB, Reset Pin, Write Protection, DDR timing, HS200, Multi Partitioning, Security Erase/Security Trim, Trim, High Priority Interrupt, Background Operation, Enhance Reliable Write, Discard Command, Security Features, Partition types, Context ID, Data Tag, Package Commands, Real Time Clock, Dynamic Device Capacity, Power Off Notification and Cache
  - Extended Security Protocols, HS400, Field Firmware Update, Product State Awareness, Security Removal Type Device Heal Report, Command Queuing, Enhance Strobe, Cache Flushing Report, BKOPS Control, Cache Barrier, RPMB Throughput Improve, Security Write Protect
- Bus mode
  - Data bus width: 1 bit, 4 bits and 8 bits
  - Bus Speed Mode: Backward compatibility for legacy MMC card mode, High Speed SDR, DDR, HS200 and HS400
  - eMMC clock frequency: 0 ~ 200MHz
- eMMC voltage range
  - VCCQ (I/O) : 1.70V~1.95V and 2.7V~3.6V
  - VCC (NAND) : 2.7V~3.6V
- Error correction engine
  - Proprietary ECC engine with hard-decision and soft-decision decode
- Temperature
  - Operation : -25℃~85℃
  - Storage : -40℃~85℃
- Low power consumption
- Manufacturing utility ready

5. eMMC Function Block Diagram

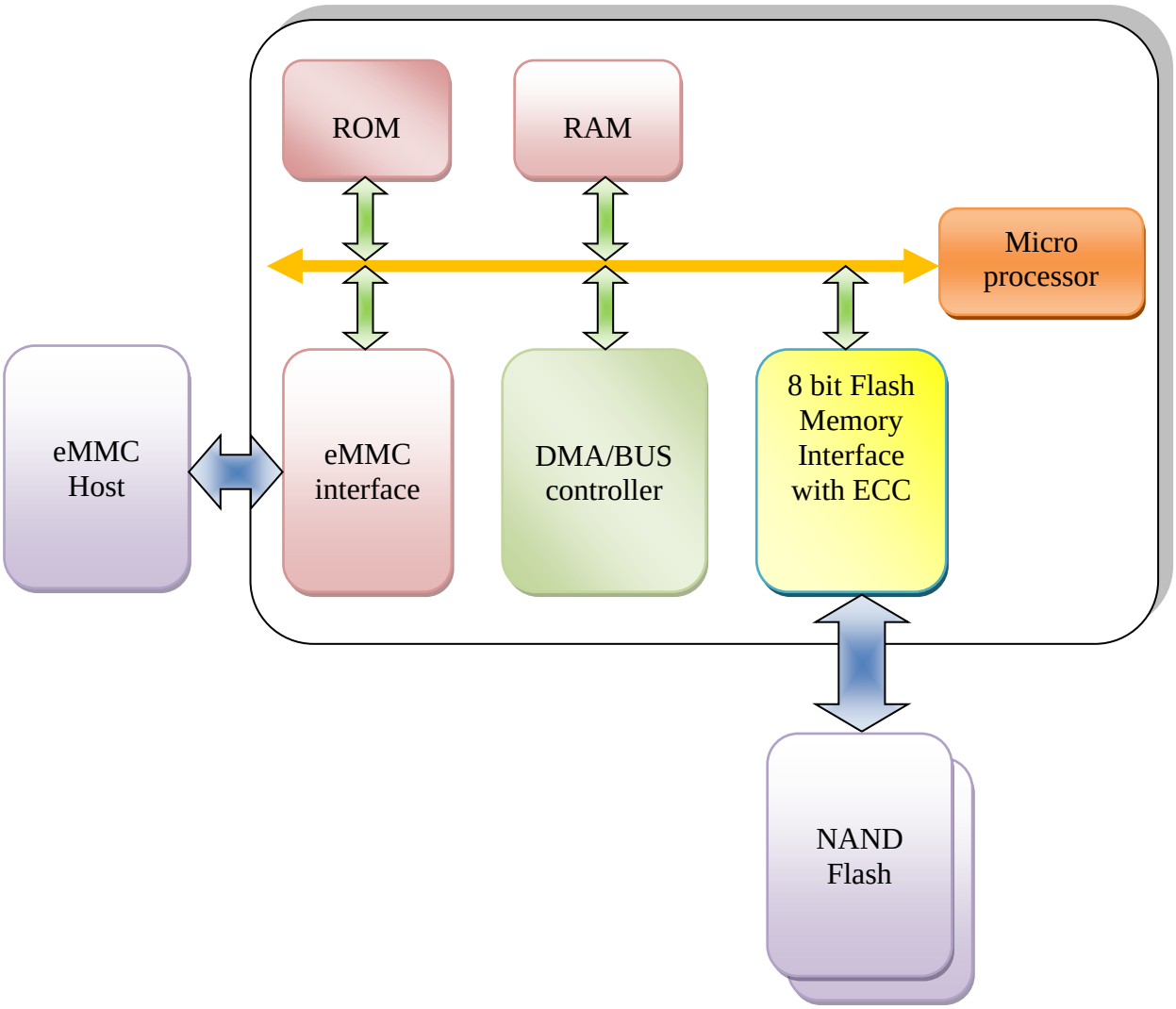


Figure 5-1 eMMC Function Block Diagram

6. Pin Description

6.1. eMMC 153 Ball Pin Assignment

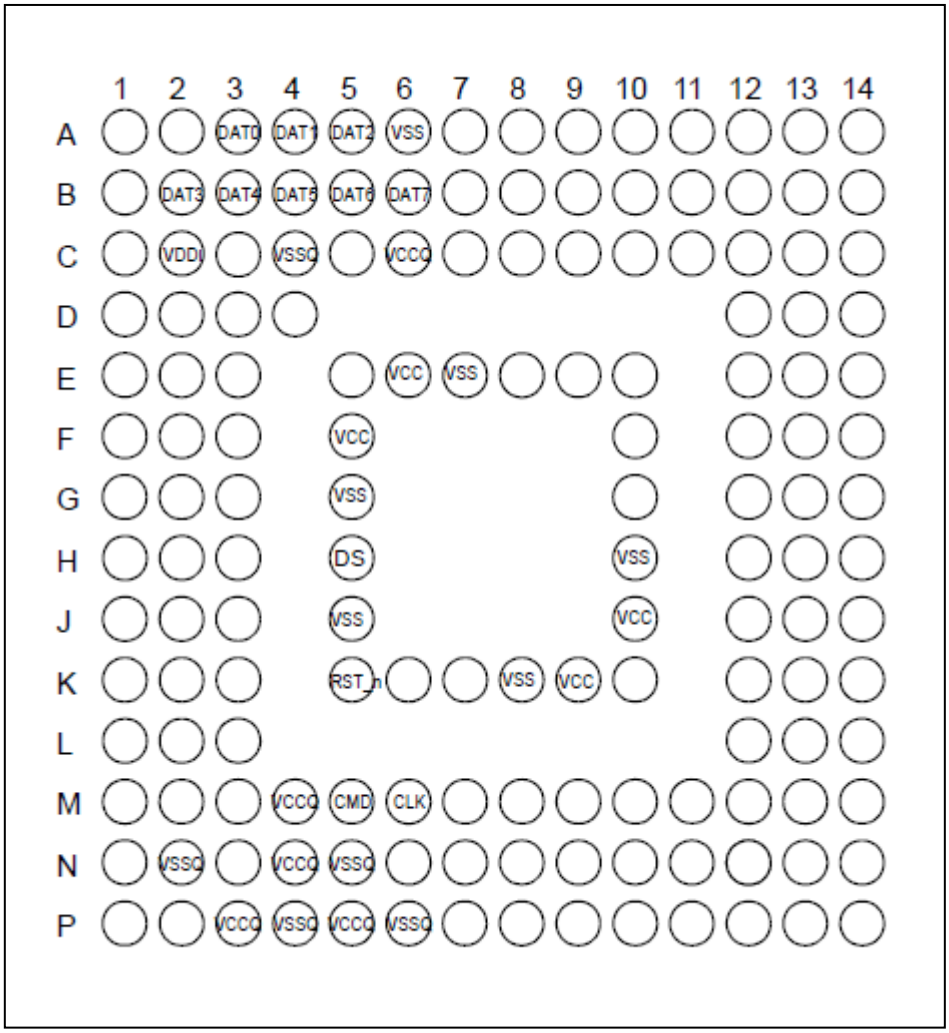


Figure 6-1 eMMC 153 ball pin assignment (Top view)

6.2. eMMC Pin Description

Pin Name	Direction	Description	Pin Number
CLK	I	eMMC clock input	M6
CMD	I/O	eMMC command line	M5
DAT0	I/O	eMMC data line	A3
DAT1			A4
DAT2			A5
DAT3			B2
DAT4			B3
DAT5			B4
DAT6			B5
DAT7			B6
RST_n	I	eMMC reset input	K5
DS	O	eMMC data strobe output	H5
VDDi	Power out	Power supply for core	C2
VCCQ	Power in	Power supply for controller and IO pad	C6, M4, N4, P3, P5
VSSQ	Ground	Ground for controller and IO pad	C4, N2, N5, P4, P6
VCC	Power in	Power supply for NAND flash device	E6, F5, J10, K9
VSS	Ground	Ground for NAND flash device	A6, E7, G5, H10, J5, K8

Table 6-1 eMMC Pin Description

7. Electrical Characteristics

The MK eMMC is used to provide an interface between on-chip bus and external (off-chip) memory devices.

7.1. General operating conditions

Parameter	Symbol	Min.	Max.	Unit	Remark
Peak voltage on all lines	-	-0.5	V_{CCQ}+0.5	V	
All Inputs					
Input leakage current (before initialization)	-	-100	100	μA	
Input leakage current (after initialization)	-	-2	2	μA	
All Outputs					
Output leakage current (before initialization)	-	-100	100	μA	
Output leakage current (after initialization)	-	-2	2	μA	

Table 7-1 General Operating Conditions

7.2. Device Power Diagram

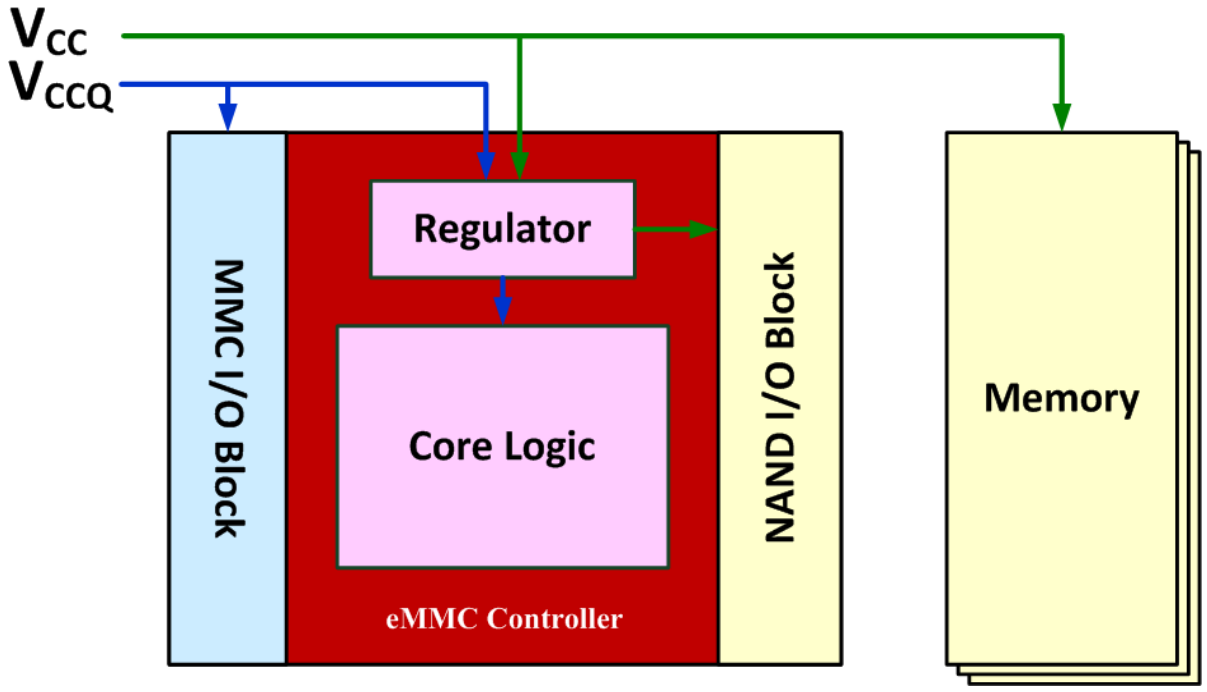


Figure 7-1 Device Power Diagram

7.3. Power supply voltage

Parameter	Symbol	Min.	Max.	Unit	Remark
Supply voltage (NAND)	V_{CC}	2.7	3.6	V	
Supply voltage (I/O)	V_{CCQ}	2.7	3.6	V	
		1.7	1.95		

Table 7-2 Power Supply Voltage

7.4. Bus Signal Line Loading

Parameter	Symbol	Min.	Max.	Unit	Remark
Pull up resistance for CMD	R_{CMD}	4.7	100(1)	KΩ	
Pull up resistance for DAT0-DAT7	R_{DAT}	10	100(1)	KΩ	
Internal pull up resistance for DAT1-DAT7	R_{int}	10	150	KΩ	
Bus signal line capacitance	C_L	-	30	pF	
Signal device capacitance	C_{Device}	-	6	pF	
Maximum signal line inductance	-	-	16	nH	

Table 7-3 Bus Signal Line Loading

(1) Recommended maximum value is 50 KΩ for 1.8V interface supply voltages. A 3V part, may use the whole range up to 100 KΩ.

Parameter	Symbol	Min.	Max.	Unit	Remark
Pull up resistance for CMD	R_{CMD}	4.7	100(1)	KΩ	
Pull up resistance for DAT0-DAT7	R_{DAT}	10	100(1)	KΩ	
Pull down resistance for Data Strobe	R_{DS}	10	100(1)	KΩ	
Internal pull up resistance for DAT1-DAT7	R_{int}	10	150	KΩ	
Signal device capacitance	C_{Device}	-	6	pF	

Table 7-4 Bus Signal Line Loading for HS400

(1) Recommended maximum value is 50 KΩ for 1.8V interface supply voltages.

7.5. Bus Signal Level

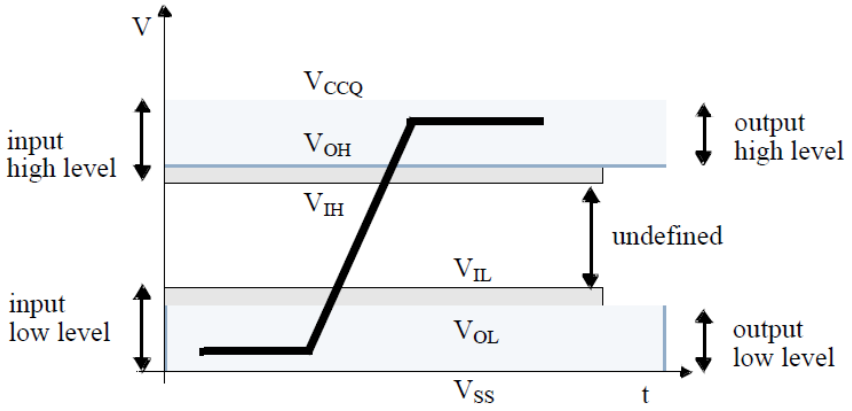


Figure 7-2 Bus Signal Level

Parameter	Symbol	Min.	Max.	Unit	Remark
Output HIGH voltage	V_{OH}	$0.75*V_{CCQ}$	-	V	V_{CCQ} = 3.3V
Output LOW voltage	V_{OL}	-	$0.125*V_{CCQ}$	V	V_{CCQ} = 3.3V
Input HIGH voltage	V_{IH}	$0.625*V_{CCQ}$	V_{CCQ} + 0.3	V	V_{CCQ} = 3.3V
Input LOW voltage	V_{IL}	V_{SS} - 0.3	$0.25*V_{CCQ}$	V	V_{CCQ} = 3.3V
utput HIGH voltage	V_{OH}	V_{CCQ} - 0.45	-	V	V_{CCQ} = 1.8V
Output LOW voltage	V_{OL}	-	0.45	V	V_{CCQ} = 1.8V
Input HIGH voltage	V_{IH}	$0.65*V_{CCQ}$	V_{CCQ} + 0.3	V	V_{CCQ} = 1.8V
Input LOW voltage	V_{IL}	V_{SS} - 0.3	$0.35*V_{CCQ}$	V	V_{CCQ} = 1.8V

Table 7-5 Bus Signal Level

7.6. Bus Timing for eMMC in backward-compatible device and high speed mode

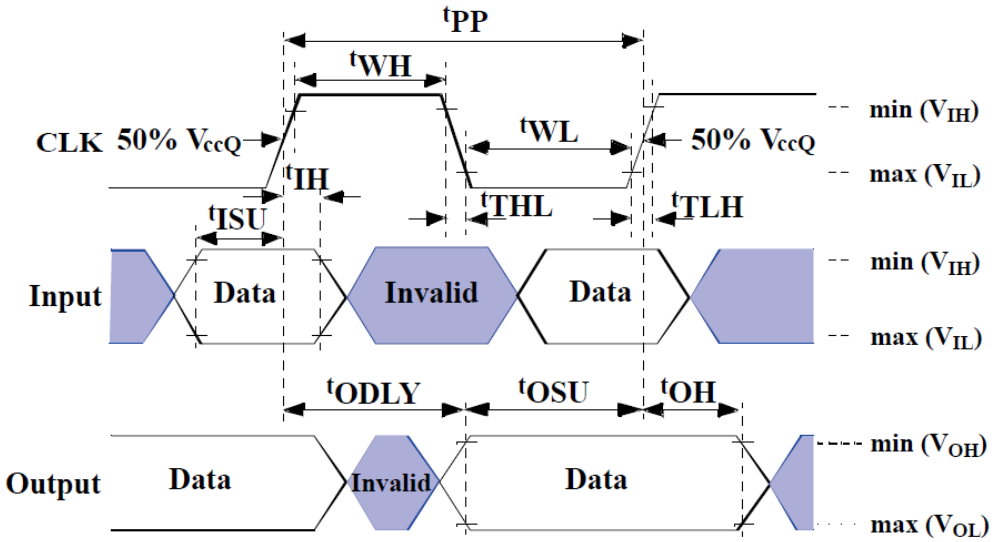


Figure 7-3 Timing diagram data input/output referenced to clock (eMMC in backward-compatible device and high speed)

Parameter	Symbol	Min.	Max.	Unit	Remark
Input MMC_CLK					
Clock frequency data transfer mode	f_{PP}	0	26	MHz	$C_L \leq 30pF$
Clock frequency identification mode	f_{OD}	0	400	KHz	
Clock low time / Clock high time	t_{WL}/t_{WH}	10	-	ns	$C_L \leq 30pF$
Clock rise time / Clock fall time	t_{TLH}/t_{THL}	-	10	ns	$C_L \leq 30pF$
Input MMC_CMD, MMC_DAT (referenced to MMC_CLK)					
Input set-up time	t_{ISU}	3	-	ns	$C_L \leq 30pF$
Input hold time	t_{IH}	3	-	ns	$C_L \leq 30pF$
Output MMC_CMD, MMC_DAT (referenced to MMC_CLK)					
Output set-up time	t_{OSU}	11.7	-	ns	$C_L \leq 30pF$
Output hold time	t_{OH}	8.3	-	ns	$C_L \leq 30pF$

Table 7-6 backward-compatible device mode timing for eMMC

(1) Clock timing is measured at 50% of V_{CCQ}.

(2) Clock rise and fall times are measured by min (V_{IH}) and max (V_{IL}).

Parameter	Symbol	Min.	Max.	Unit	Remark
Input MMC_CLK					
Clock frequency data transfer mode	f_{PP}	0	52	MHz	$C_L \leq 30pF$
Clock frequency identification mode	f_{OD}	0	400	KHz	
Clock low time / Clock high time	t_{WL}/t_{WH}	6.5	-	ns	$C_L \leq 30pF$
Clock rise time / Clock fall time	t_{TLH}/t_{THL}	-	3	ns	$C_L \leq 30pF$
Input MMC_CMD, MMC_DAT (referenced to MMC_CLK)					
Input set-up time	t_{ISU}	3	-	ns	$C_L \leq 30pF$
Input hold time	t_{IH}	3	-	ns	$C_L \leq 30pF$
Output MMC_CMD, MMC_DAT (referenced to MMC_CLK)					
Output delay time during data transfer	t_{ODLY}	-	13.7	ns	$C_L \leq 30pF$
Output hold time	t_{OH}	2.5	-	ns	$C_L \leq 30pF$
Signal rise time	t_{RISE}	-	3	ns	$C_L \leq 30pF$
Signal fall time	t_{FALL}	-	3	ns	$C_L \leq 30pF$

Table 7-7 High speed mode timing for eMMC

(1) Clock timing is measured at 50% of V_{CCQ}.

(2) Clock rise and fall times are measured by min (V_{IH}) and max (V_{IL}).

(3) Inputs CMD, DAT rise and fall times are measured by min (V_{IH}) and max (V_{IL}), and outputs CMD, DAT rise and fall times are measured by min (V_{OH}) and max (V_{OL}).

7.7. Bus Timing for eMMC in DDR Mode

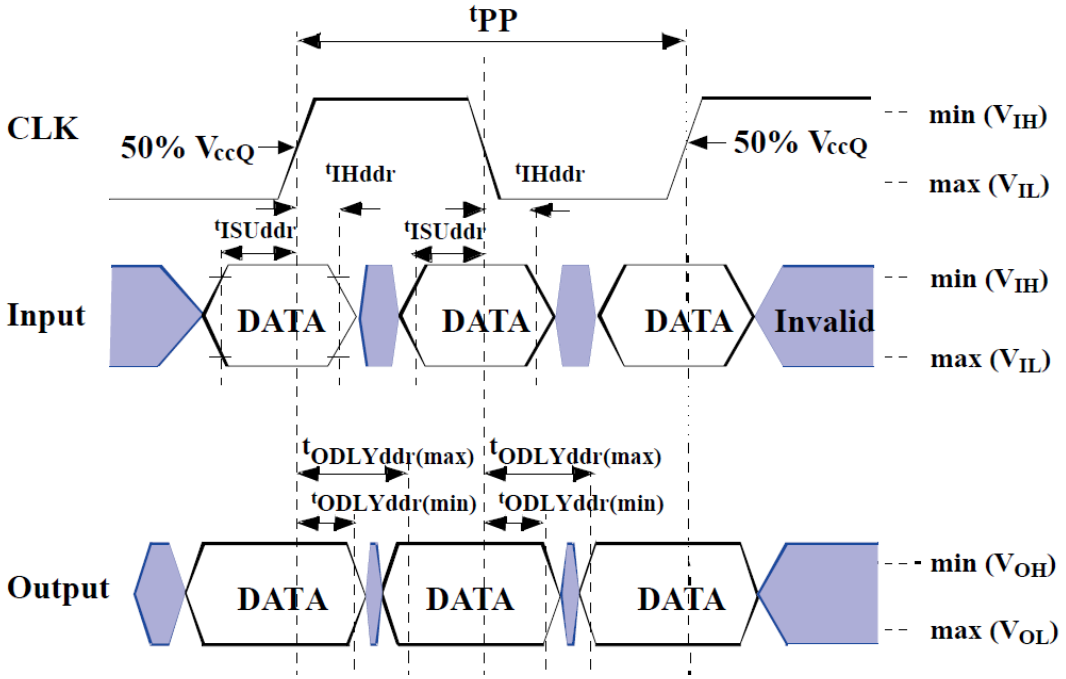


Figure 7-4 Timing diagram data input/output referenced to clock (DDR mode)

Parameter	Symbol	Min.	Max.	Unit	Remark
Input MMC_CLK					
Clock duty cycle	-	45	55	%	
Clock rise time / Clock fall time	t_{TLH}/t_{THL}	-	3	ns	$C_L \leq 30pF$
Input MMC_CMD (referenced to MMC_CLK)					
Input set-up time	t_{ISUddr}	3	-	ns	$C_L \leq 20pF$
Input hold time	t_{IHddr}	3	-	ns	$C_L \leq 20pF$
Output MMC_CMD (referenced to MMC_CLK)					
Output delay time during data transfer	t_{ODLY}	-	13.7	ns	$C_L \leq 20pF$
Output hold time	t_{OH}	2.5	-	ns	$C_L \leq 20pF$
Signal rise time	t_{RISE}	-	3	ns	$C_L \leq 20pF$
Signal fall time	t_{FALL}	-	3	ns	$C_L \leq 20pF$
Input MMC_DAT (referenced to MMC_CLK)					
Input set-up time	t_{ISUddr}	2.5	-	ns	$C_L \leq 20pF$
Input hold time	t_{IHddr}	2.5	-	ns	$C_L \leq 20pF$
Output MMC_DAT (referenced to MMC_CLK)					
Output delay time during data transfer	$t_{ODLYddr}$	1.5	7	ns	$C_L \leq 20pF$

Parameter	Symbol	Min.	Max.	Unit	Remark
Signal rise time	t_{RISE}	-	2	ns	$C_L \leq 20pF$
Signal fall time	t_{FALL}	-	2	ns	$C_L \leq 20pF$

Table 7-8 DDR mode timing for eMMC

(1) Clock timing is measured at 50% of V_{CCQ}.

(2) Inputs DAT rise and fall times are measured by min (V_{IH}) and max (V_{IL}), and outputs DAT rise and fall times are measured by min (V_{OH}) and max (V_{OL}).

7.8. Bus Timing for eMMC in HS200 Mode

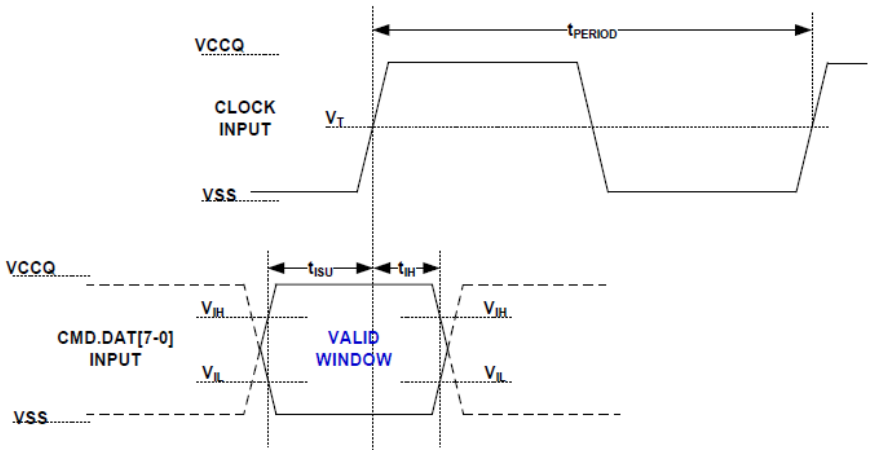


Figure 7-5 Timing diagram data input referenced to clock (HS200 mode)

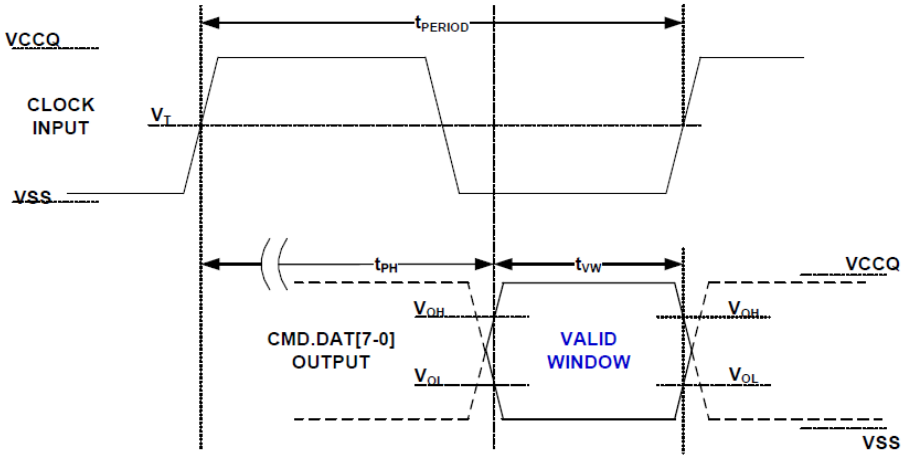


Figure 7-6 Timing diagram data output referenced to clock (HS200 mode)

Parameter	Symbol	Min.	Max.	Unit	Remark
Input MMC_CLK					
Clock cycle time	t_{PERIOD}	5	-	ns	

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock rise time / Clock fall time	t_{TLH}/t_{THL}	-	1	ns	C_{Device} = 6 pF
Clock duty cycle	-	30	70	%	
Input MMC_CMD, MMC_DAT (referenced to MMC_CLK)					
Input set-up time	t_{ISU}	1.4	-	ns	$C_{Device} \leq 6pF$
Input hold time	t_{IH}	0.8	-	ns	$C_{Device} \leq 6pF$
Output MMC_CMD, MMC_DAT (referenced to MMC_CLK)					
Output delay time during data transfer	t_{PH}	0	2	UI	
Delay variation due to temperature change after tuning	Δ_{TPH}	-350 (ΔT=-20°C)	+1550 (ΔT=90°C)	ps	
Output valid data window	t_{VW}	0.575	-	UI	

Table 7-9 HS200 mode timing for eMMC

(1) Unit Interval (UI) is one bit nominal time. For example, UI = 5ns at 200MHz.

7.9. Bus Timing for eMMC in HS400 Mode

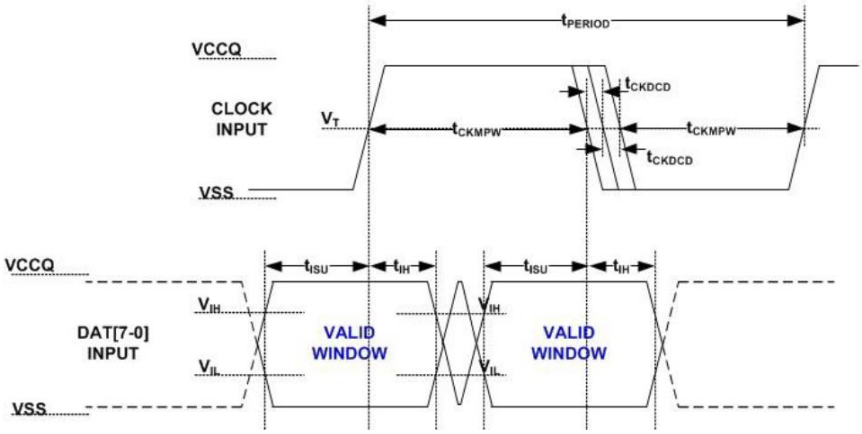


Figure 7-7 Timing diagram data input referenced to clock (HS400 mode)

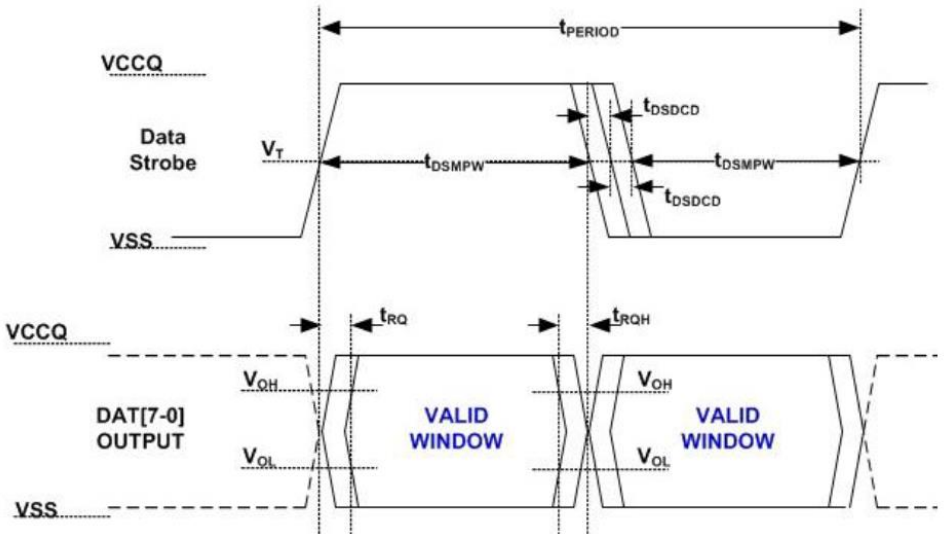


Figure 7-8 Timing diagram data output referenced to clock (HS400 mode)

Parameter	Symbol	Min.	Max.	Unit	Remark
Input MMC_CLK					
Clock cycle time	t_{PERIOD}	5	-	ns	
Slew rate	SR	1.125	-	V/ns	
Duty cycle distortion	t_{CKDCD}	0	0.3	ns	
Minimum pulse width	t_{CKMPW}	2.2	-	ns	
Input MMC_DAT (referenced to MMC_CLK)					
Input set-up time	t_{ISUddr}	0.4	-	ns	$C_{Device} \leq 6pF$
Input hold time	t_{IHddr}	0.4	-	ns	$C_{Device} \leq 6pF$
Slew rate	SR	1.125	-	V/ns	
Output MMC_STRB					
Clock cycle time	t_{PERIOD}	5	-	ns	
Slew rate	SR	1.125	-	V/ns	
Duty cycle distortion	t_{CKDCD}	0	0.2	ns	
Minimum pulse width	t_{CKMPW}	2	-	ns	
Read pre-amble	t_{RPRE}	0.4	-	t_{PERIOD}	
Read post-amble	t_{RPST}	0.4	-	t_{PERIOD}	
Output MMC_ DAT/ MMC_ CMD (referenced to MMC_STRB)					
Output skew	t_{RQ}/t_{RQ_CMD}	-	0.4	ns	
Output hold skew	t_{RQH}/t_{RQH_CMD}	-	0.4	ns	

Parameter	Symbol	Min.	Max.	Unit	Remark
Slew rate	SR	1.125	-	V/ns	

Table 7-10 HS400 mode timing for eMMC

8. eMMC Register Description

The design parameters are parameters that control the implementation of RTL design by Verilog parameter or VHDL generic. The purpose of parameters is to make the hardware design reusable on different conditions.

Software designers should refer to the particular implementation to do the programming. This section introduces the registers in eMMC and the values that are used in eMMC MKEMA008GT1E-C Datasheet. The following table is the register list of current specification. The detail functionality is not described here; please reference to latest eMMC specifications.

Register Name	eMMC 4.5	eMMC 5.01	eMMC 5.1
Operation Condition Register (OCR)	V	V	V
Card Identification Register (CID)	V	V	V
Driver Stage Register (DSR)	V	V	V
Relative Card Address Register (RCA)	V	V	V
Card Specific Data Register (CSD)	V	V	V
Extended Card Specific Data Register (EXT_CSD)	V	V	V

Table 8-1 eMMC Register table

8.1. Operation Conditions Register (OCR) Register

The 32-bit operation conditions register (OCR) stores the voltage profile of the Device and the access mode indication. In addition, this register includes a status information bit. This status bit is set if the Device power up procedure has been finished.

OCR bit	VCCQ voltage window	eMMC
[31]	Card power up status bit (busy)(1)	
[30:29]	Access Mode	00b (byte mode) 10b (sector mode)
[28:24]	Reserved	0 0000b
[23:15]	2.7V – 3.6V	1 1111 1111 b
[14:8]	2.0V – 2.6V	000 0000b
[7]	1.7V~1.95V	1b
[6:0]	Reserved	000 0000b

Table 8-2 OCR Table

(1) This bit is set to LOW if the Device has not finished the power up routine.

8.2. SD Card Identification Register (CID)

The Device IDentification (CID) register is 128 bits wide. It contains the Device identification information used during the Device identification phase. Every type of eMMC Device shall have a unique identification number. The structure of the CID register is defined in the following table.

CID bit	width	Name	Field
[127:120]	8	Manufacture ID	MID
[119:114]	6	Reserved	-
[113:112]	2	Device/BGA	CBX
[111:104]	8	OEM/Application ID	OID
[103:56]	48	Product Name	PNM
[55:48]	8	Product Revision	PRV
[47:16]	32	Product Serial Number	PSN
[15:8]	8	Manufacturing Date	MDT
[7:1]	7	CRC7 check sum	CRC
[0]	1	Not used, always ‘1’	-

Table 8-3 CID Table

8.3. Driver Stage Register (DSR)

The 16-bit driver stage register (DSR) is optionally used to improve the bus performance for extended operating conditions. The CSD register carries the information about the DSR register usage. The default value of the DSR register is 0x404.

8.4. Relative Card Address Register (RCA)

The writable 16-bit relative Device address (RCA) register carries the Device address assigned by the host during the Device identification. This address is used for the addressed host-Device communication after the Device identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all Devices into the Stand-by State with CMD7.

8.5. Card Specific Data Register (CSD)

The Device-Specific Data (CSD) register provides information on how to access the Device contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E below) can be changed by CMD27.

CSD bit	Width	Name	Field	Type	Value	Note
[127:126]	2	CSD structure	CSD_STRUCTURE	R	3h	
[125:122]	4	System specification version	SPEC_VERS	R	4h	
[121:120]	2	Reserved	-	-	-	-
[119:112]	8	Data read access-time 1	TAAC	R	FFh	1 ms
[111:104]	8	Data read access-time 2	NSAC	R	FFh	
[103:96]	8	Max. data transfer rate	TRAN_SPEED	R	32h	25 MHz
[95:84]	12	Device command classes	CCC	R	1F5h	
[83:80]	4	Max. read data block length	READ_BL_LEN	R	9h	512 bytes
[79]	1	Partial block read allowed	READ_BL_PARTIAL	R	0b	Not Support
[78]	1	Write block misalignment	WRITE_BLK_MISALIGN	R	0b	Not Support
[77]	1	Read block misalignment	READ_BLK_MISALIGN	R	0b	Not Support
[76]	1	DSR implemented	DSR_IMP	R	0b	Not support
[75:74]	2	Reserved	-	-	-	-
[73:62]	12	Device size	C_SIZE	R	FFFh	>2GB
[61:59]	3	Max. read current @ VDD min	VDD_R_CURR_MIN	R	3h	
[58:56]	3	Max. read current @ VDD max	VDD_R_CURR_MAX	R	7h	
[55:53]	3	Max. write current @ VDD min	VDD_W_CURR_MIN	R	3h	
[52:50]	3	Max. write current @ VDD max	VDD_W_CURR_MAX	R	7h	
[49:47]	3	Device size multiplier	C_SIZE_MULT	R	7h	
[46:42]	5	Erase group size	ERASE_GRP_SIZE	R	1Fh	
[41:37]	5	Erase group size multiplier	ERASE_GRP_MULT	R	1Ch	
[36:32]	5	Write protect group size	WP_GRP_SIZE	R	0h	
[31]	1	Write protect group enable	WP_GRP_ENABLE	R	1b	

CSD bit	Width	Name	Field	Type	Value	Note
[30:29]	2	Manufacturer default ECC	DEFAULT_ECC	R	0h	
[28:26]	3	Write speed factor	R2W_FACTOR	R	2h	4X
[25:22]	4	Max. write data block length	WRITE_BL_LEN	R	9h	512 bytes
[21]	1	Partial block write allowed	WRITE_BL_PARTIAL	R	0b	Not Support
[20:17]	4	Reserved	-	-	-	-
[16]	1	Content protection application	CONTENT_PROT_APP	R	0b	
[15]	1	File format group	FILE_FORMAT_GRP	R/W	0b	HD like FAT
[14]	1	Copy flag (OTP)	COPY	R/W	0b	Not copied
[13]	1	Permanent write protection	PERM_WRITE_PROTECT	R/W	0b	Not protected
[12]	1	Temporary write protection	TMP_WRITE_PROTECT	R/W/E	0b	Not protected
[11:10]	2	File format	FILE_FORMAT	R/W	0h	HD like FAT
[9:8]	2	ECC code	ECC	R/W/E	0h	None
[7:1]	7	CRC	CRC	R/W/E	-	-
[0]	1	Not used, always ‘1’	-		1b	-

Table 8-4 CSD Table

8.6. Extended CSD register

The Extended CSD register defines the Device properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, that defines the Device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, that defines the configuration the Device is working in. These modes can be changed by the host by means of the SWITCH command.

Extend CSD bit	Width	Name	Field	Type	Value	Note
Properties Segment						
[511:506]	6	Reserved	-	-	-	-
[505]	1	Extend Security Command Error	EXT_SECURITAY	R	0h	

Extend CSD bit	Width	Name	Field	Type	Value	Note
[504]	1	Supported Command Sets	S_CMD_SET	R	1h	
[503]	1	HPI features	HPI_FEATURES	R	1h	
[502]	1	Background operations support	BKOPS_SUPPORT	R	1h	
[501]	1	Max packed read commands	MAX_PACKED_READS	R	3Fh	
[500]	1	Max packed write commands	MAX_PACKED_WRITES	R	3Fh	
[499]	1	Data Tag Support	DATA_TAG_SUPPORT	R	1h	
[498]	1	Tag Unit Size	TAG_UNIT_SIZE	R	3h	
[497]	1	Tag Resources Size	TAG_RES_SIZE	R	0h	
[496]	1	Context management capabilities	CONTEXT_CAPABILITIES	R	5h	
[495]	1	Large Unit size	LARGE_UNIT_SIZE_M1	R	Bh	
[494]	1	Extended partitions attribute support	EXT_SUPPORT	R	3h	
[493]	1	Supported modes	SUPPORTED_MODES	R	1h	
[492]	1	FFU features	FFU_FEATURES	R	0h	
[491]	1	Operation codes timeout	OPERATION_CODE_TIMEOUT	R	0h	
[490:487]	4	FFU Argument	FFU_ARG	R	41536F6Ch	
[486]	1	Barrier support	BARRIER_SUPPORT	R	0h	
[485:309]	177	Reserved	-	-	-	-
[308]	1	CMD Queuing Support	CMDQ_SUPPORT	R	0h	

Extend CSD bit	Width	Name	Field	Type	Value	Note
[307]	1	CMD Queuing Depth	CMDQ_DEPTH	R	0h	
[306]	1	Reserved	-	-	-	-
[305:302]	4	Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	R	0h	
[301:270]	32	Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	R	0h	
[269]	1	Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	R	0h	
[268]	1	Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	R	0h	
[267]	1	Pre EOL information	PRE_EOL_INFO	R	1h	
[266]	1	Optimal read size	OPTIMAL_READ_SIZE	R	8h	
[265]	1	Optimal write size	OPTIMAL_WRITE_SIZE	R	8h	
[264]	1	Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	R	4h	
[263:262]	2	Device version	DEVICE_VERSION	R	0h	
[261:254]	8	Firmware version	FIRMWARE_VERSION	R	1h	
[253]	1	Power class for 200MHz, DDR at VCC= 3.6V	PWR_CL_DDR_200_360	R	0h	
[252:249]	4	Cache size	CACHE_SIZE	R	100h	32KB
[248]	1	Generic CMD6 timeout	GENERIC_CMD6_TIME	R	Ah	
[247]	1	Power off notification(long) timeout	POWER_OFF_LONG_TIME	R	64h	

Extend CSD bit	Width	Name	Field	Type	Value	Note
[246]	1	Background operations status	BKOPS_STATUS	R	0h	
[245:242]	4	Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	R	0h	
[241]	1	Number of correctly programmed sectors	INI_TIMEOUT_AP	R	1Eh	
[240]	1	Cache Flushing Policy	CACHE_FLUSH_POLICY	R	1h	
[239]	1	Power class for 52MHz, DDR at VCC = 3.6V	PWR_CL_DDR_52_360	R	0h	
[238]	1	Power class for 52MHz, DDR at VCC = 1.95V	PWR_CL_DDR_52_195	R	0h	
[237]	1	Power class for 200MHz at VCCQ =1.95V, VCC = 3.6V	PWR_CL_200_195	R	0h	
[236]	1	Power class for 200MHz, at VCCQ =1.3V, VCC = 3.6V	PWR_CL_200_130	R	0h	
[235]	1	Minimum Write Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	R	0h	
[234]	1	Minimum Read Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	R	0h	

Extend CSD bit	Width	Name	Field	Type	Value	Note
[233]	1	Reserved	-	-	-	-
[232]	1	TRIM Multiplier	TRIM_MULT	R	2h	
[231]	1	Secure Feature support	SEC_FEATURE_SUPPORT	R	55h	
[230]	1	Secure Erase Multiplier	SEC_ERASE_MULT	R	F0h	
[229]	1	Secure TRIM Multiplier	SEC_TRIM_MULT	R	F0h	
[228]	1	Boot information	BOOT_INFO	R	7h	
[227]	1	Reserved	-	-	-	-
[226]	1	Boot partition size	BOOT_SIZE_MULT	R	20h	
[225]	1	Access size	ACC_SIZE	R	7h	
[224]	1	High-capacity erase unit size	HC_ERASE_GRP_SIZE	R	1h	
[223]	1	High-capacity erase timeout	ERASE_TIMEOUT_MULT	R	Ah	
[222]	1	Reliable write sector count	REL_WR_SEC_C	R	1h	
[221]	1	High-capacity write protect group size	HC_WP_GRP_SIZE	R	10h	
[220]	1	Sleep current (VCC)	S_C_VCC	R	7h	
[219]	1	Sleep current (VCCQ)	S_C_VCCQ	R	7h	
[218]	1	Production state awareness timeout	PRODUCTION_STATE_AWARENESS_TIMOUT	R	Dh	
[217]	1	Sleep/awake timeout	S_A_TIMEOUT	R	15h	
[216]	1	Sleep Notification Timeout	SLEEP_NOTIFICATION_TIME	R	7h	
[215:212]	4	Sector Count	SEC_COUNT	R	-	Depend on eMMC size

Extend CSD bit	Width	Name	Field	Type	Value	Note
[211]	1	Secure Write Protect Information	SECURE_WP_INFO	R	0h	
[210]	1	Minimum Write Performance for 8bit at 52 MHz	MIN_PERF_W_8_52	R	0h	
[209]	1	Minimum Read Performance for 8bit at 52 MHz	MIN_PERF_R_8_52	R	0h	
[208]	1	Minimum Write Performance for 8bit at 26 MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	R	0h	
[207]	1	Minimum Read Performance for 8bit at 26 MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	R	0h	
[206]	1	Minimum Write Performance for 4bit at 26 MHz	MIN_PERF_W_4_26	R	0h	
[205]	1	Minimum Read Performance for 4bit at 26 MHz	MIN_PERF_R_4_26	R	0h	
[204]	1	Reserved	-	-	-	-
[203]	1	Power class for 26 MHz at 3.6 V 1 R	PWR_CL_26_360	R	0h	
[202]	1	Power class for 52 MHz at 3.6 V 1 R	PWR_CL_52_360	R	0h	
[201]	1	Power class for 26 MHz at 1.95 V 1 R	PWR_CL_26_195	R	0h	

Extend CSD bit	Width	Name	Field	Type	Value	Note
[200]	1	Power class for 52 MHz at 1.95 V 1 R	PWR_CL_52_195	R	0h	
[199]	1	Partition switching timing	PARTITION_SWITCH_TIME	R	6h	
[198]	1	Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	R	19h	
[197]	1	I/O Driver Strength	DRIVER_STRENGTH	R	1Fh	
[196]	1	Device type	DEVICE_TYPE	R	17h	
[195]	1	Reserved	-	-	-	-
[194]	1	CSD STRUCTURE	CSD_STRUCTURE	R	2h	
[193]	1	Reserved	-	-	-	-
[192]	1	Extended CSD revision	EXT_CSD_REV	R	7h	
Modes Segment						
[191]	1	Command set	CMD_SET	R/W/E_P	0h	
[190]	1	Reserved	-	-	-	-
[189]	1	Command set revision	CMD_SET_REV	R	0h	
[188]	1	Reserved	-	-	-	-
[187]	1	Power class	POWER_CLASS	R/W/E_P	0h	
[186]	1	Reserved	-	-	-	-
[185]	1	High-speed interface timing	HS_TIMING	R/W/E_P	0h	
[184]	1	Strobe Support	STROBE_SUPPORT	R	0h	
[183]	1	Bus width mode	BUS_WIDTH	W/E_P	0h	
[182]	1	Reserved	-	-	-	-
[181]	1	Erased memory content	ERASED_MEM_CONT	R	0h	
[180]	1	Reserved	-	-	-	-

Extend CSD bit	Width	Name	Field	Type	Value	Note
[179]	1	Partition configuration	PARTITION_CONFIG	R/W/E & R/W/E_P	0h	
[178]	1	Boot config protection	BOOT_CONFIG_PROT	R/W & R/W/C_P	0h	
[177]	1	Boot bus Conditions	BOOT_BUS_CONDITIONS	R/W/E	0h	
[176]	1	Reserved	-	-	-	-
[175]	1	High-density erase group definition	ERASE_GROUP_DEF	R/W/E_P	0h	
[174]	1	Boot write protection status registers	BOOT_WP_STATUS	R	0h	
[173]	1	Boot area write protection register	BOOT_WP	R/W & R/W/C_P	0h	
[172]	1	Reserved	-	-	-	-
[171]	1	User area write protection register	USER_WP	R/W, R/W/C_P & R/W/E_P	0h	
[170]	1	Reserved	-	-	-	-
[169]	1	FW configuration	FW_CONFIG	R/W	0h	
[168]	1	RPMB Size	RPMB_SIZE_MULT	R	20h	
[167]	1	Write reliability setting register	WR_REL_SET	R/W	1Fh	
[166]	1	Write reliability parameter register	WR_REL_PARAM	R	4h	

Extend CSD bit	Width	Name	Field	Type	Value	Note
[165]	1	Start Sanitize operation	SANITIZE_START	W/E_P	0h	
[164]	1	Manually start background operations	BKOPS_START	W/E_P	0h	
[163]	1	Enable background operations handshake	BKOPS_EN	R/W & R/W/E	0h	
[162]	1	H/W reset function	RST_n_FUNCTION	R/W	0h	
[161]	1	HPI management	HPI_MGMT	R/W/E_P	0h	
[160]	1	Partitioning Support	PARTITIONING_SUPPORT	R	7h	
[159:157]	3	Max Enhanced Area Size	MAX_ENH_SIZE_MULT	R	-	Depend on flash and FW setting
[156]	1	Partitions attribute	PARTITIONS_ATTRIBUTE	R/W	0h	
[155]	1	Partitioning Setting	PARTITION_SETTING_COMPLETED	R/W	0h	
[154:143]	12	General Purpose Partition Size	GP_SIZE_MULT	R/W	0h	
[142:140]	3	Enhanced User Data Area Size	ENH_SIZE_MULT	R/W	0h	
[139:136]	4	Enhanced User Data Start Address	ENH_START_ADDR	R/W	0h	
[135]	1	Reserved	-	-	-	-
[134]	1	Bad Block Management mode	SEC_BAD_BLK_MGMNT	R/W	0h	
[133]	1	Production state awareness	PRODUCTION_STATE_AWARENESS	R/W/E	0h	

Extend CSD bit	Width	Name	Field	Type	Value	Note
[132]	1	Package Case Temperature is controlled	TCASE_SUPPORT	W/E_P	0h	
[131]	1	Periodic Wake-up	PERIODIC_WAKE UP	R/W/E	0h	
[130]	1	Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	R	1h	
[129:128]	2	Reserved	-	-	-	-
[127:64]	64	Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	R	0h	
[63]	1	Native sector size	NATIVE_SECTOR_SIZE	R	0h	
[62]	1	Sector size emulation	USE_NATIVE_SECTOR	R/W	0h	
[61]	1	Sector size	DATA_SECTOR_SIZE	R	0h	
[60]	1	1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	R	0h	
[59]	1	Class 6 commands control	CLASS_6_CTRL	R/W/E_P	0h	
[58]	1	Number of addressed group to be Released	DYNCAP_NEEDED	R	0h	
[57:56]	2	Exception events control	EXCEPTION_EVENTS_CTRL	R/W/E_P	0h	
[55:54]	1	Exception events status	EXCEPTION_EVENTS_STATUS	R	0h	
[53:52]	2	Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE	R/W	0h	

Extend CSD bit	Width	Name	Field	Type	Value	Note
[51:37]	15	Context configuration	CONTEXT_CONF	R/W/E_P	0h	
[36]	1	Packed command status	PACKED_COMMAND_STATUS	R	0h	
[35]	1	Packed command failure index	PACKED_FAILURE_INDEX	R	0h	
[34]	1	Power Off Notification	POWER_OFF_NOTIFICATION	R/W/E_P	0h	
[33]	1	Control to turn the Cache ON/OFF	CACHE_CTRL	R/W/E_P	0h	
[32]	1	Flushing of the cache	FLUSH_CACHE	W/E_P	0h	
[31]	1	Control to turn the Barrier ON/OFF	BARRIER_CTRL	R/W	0h	
[30]	1	Mode config	MODE_CONFIG	R/W/E_P	0h	
[29]	1	Mode operation codes	MODE_OPERATION_CODES	W/E_P	0h	
[28:27]	2	Reserved	-	-	-	-
[26]	1	FFU status	FFU_STATUS	R	0h	
[25:22]	4	Pre loading data size	PRE_LOADING_DATA_SIZE	R/W/E_P	0h	
[21:18]	4	Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	R	6D0E00h	
[17]	1	Product state awareness enablemen	PRODUCT_STATE_AWARENESS_ENABLEMENT	R/W/E & R	0h	
[16]	1	Secure Removal Type	SECURE_REMOVAL_TYPE	R/W & R	9h	
[15]	1	Command Queue Mode Enable	CMDQ_MODE_EN	R/W/E_P	0h	
[14:0]	1	Reserved	-	-	-	-

Table 8-5 Extend CSD Table

9. Production Specifications

9.1. Performance

Part Number	Capacities	Flash Type	Interleave Operation	Frequency / Mode	Flash I/O	Performance (MB/S)	
						Write	Read
MKEMA008GT1E-C	8GB	64Gb MLCx1	N	200MHz / HS200	3.3 v	41	105

Table 9-1 MKEMA008GT1E-C performance

9.2. Power Consumption

Operating Current

Part Number	Capacities	Flash Type	Interleave Operation	Frequency / Mode	Flash I/O	Max Operating Current (mA)	
						Write	Read
MKEMA008GT1E-C	8GB	64Gb MLCx1	N	200MHz / HS200	3.3 v	50	100

Table 9-2 MKEMA008GT1E-C Operating Current

Standby/Sleep Current

Part Number	Capacities	Flash Type	Interleave Operation	Standby Current (μA)	Sleep Current (μA)
MKEMA008GT1E-C	8GB	64Gb MLCx1	N	150	100

Table 9-3 MKEMA008GT1E-C standby/sleep current

9.3. Endurance Test

9.3.1. BIT Test.

Test tool version: BIT 7.1 Pro.

Card Reader: SanDisk ImageMate All-in-One.

Part Number	Capacities	Flash Type	Operation System	Test Time (hr.)	Test Result
MKEMA008GT1E-C	8GB	64Gb MLCx1	Win10 x64	168	Pass

Table 9-4 MKEMA008GT1E-C Bit Test

9.3.2. Junior Test

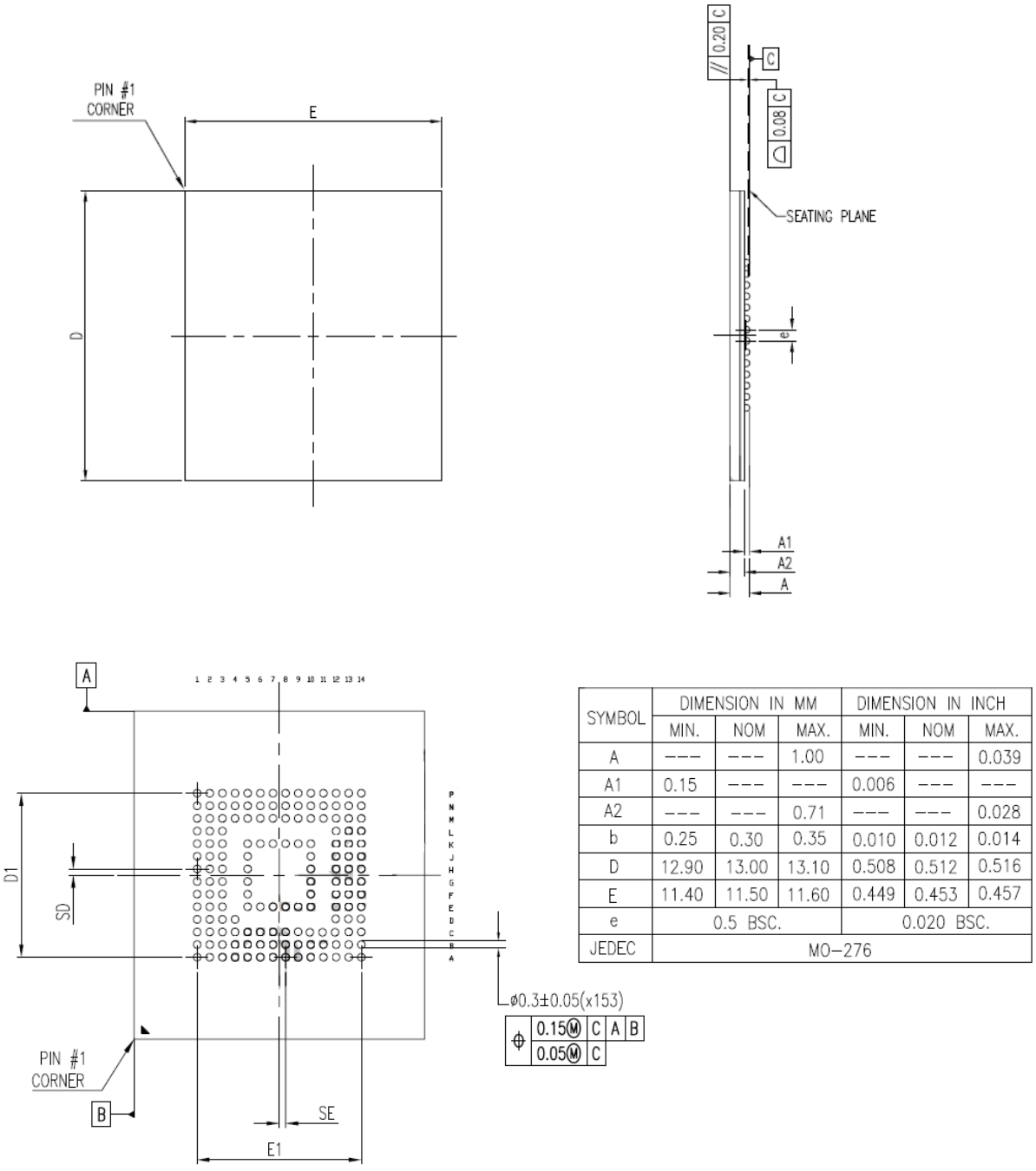
Test tool version: Junior V2.22 DEC 6 2000.

Card Reader: SanDisk ImageMate All-in-One.

Part Number	Capacities	Flash Type	Operation System	Test Time (hr.)	Test Result
MKEMA008GT1E-C	8GB	64Gb MLCx1	Win10 x64	168	Pass

Table 9-5 MKEMA008GT1E-C Junior Test

10. Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	---	---	1.00	---	---	0.039
A1	0.15	---	---	0.006	---	---
A2	---	---	0.71	---	---	0.028
b	0.25	0.30	0.35	0.010	0.012	0.014
D	12.90	13.00	13.10	0.508	0.512	0.516
E	11.40	11.50	11.60	0.449	0.453	0.457
e	0.5 BSC.			0.020 BSC.		
JEDEC	MO-276					

Figure 10-1 Package Outline Dimension Drawing

11. MKEMA008GT1E-C Partition Configuration

TABLE 11-1 MKEMA008GT1E-C Partition Configuration Table

Partition Table	Percentage
Boot1 Partition	4MB/default
Boot2 Partition	4MB/default
RPMB Partition	4MB/default
User Partition	7363MB