Description

JMT N-channel MOSFET

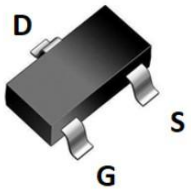
Features

- V_{DS}=60V, I_D=0.25A
  $R_{DS(ON)}$ <2.2Ω @ V_{GS} = 10V
  $R_{DS(ON)}$ <2.87Ω @ V_{GS} = 5V
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired
- ESD Protected: 2KV

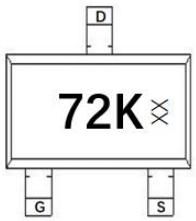
Application

- Battery Operated Systems
- Direct logic-level Interface: TTL/CMOS
- Solid-State Relays

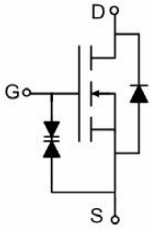
RoHS



SOT-23 top view



Marking and pin Assignment



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
72K	JMTL2N7002KS	TAPING	SOT-23	7inch	3000	180000

Absolute Maximum Ratings (T_A=25℃ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		60	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Continuous Drain Current	T_A= 25℃	0.25	A
		T_A= 100℃	0.16	
I_{DM}	Pulsed Drain Current note1		1	A
P_D	Power Dissipation	T_A= 25℃	0.23	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		543	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃

Electrical Characteristics (T_J=25℃ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D= 250μA	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} =60V, V_{GS} = 0V,	-	-	1	μA
I_{GSS}	Gate to Body Leakage Current	V_{DS} =0V, V_{GS} = ±20V	-	-	±10	uA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D= 250μA	1	1.6	2.5	V
$R_{DS(on)}$	Static Drain-Source on-Resistance note2	V_{GS} =10V, I_D =0.3A	-	1.69	2.2	Ω
		V_{GS} =4.5V, I_D =0.2A	-	2.05	2.87	
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz	-	28	-	pF
C_{oss}	Output Capacitance		-	11	-	pF
C_{rss}	Reverse Transfer Capacitance		-	4	-	pF
Q_g	Total Gate Charge	V_{DS} = 10V, I_D = 0.3A, V_{GS} = 4.5V	-	1.7	-	nC
Q_{gs}	Gate-Source Charge		-	0.3	-	nC
Q_{gd}	Gate-Drain(“Miller”) Charge		-	0.6	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 30V, I_D =0.2A, R_{GEN} = 10Ω,V_{GS}=10V,	-	10	-	ns
t_r	Turn-on Rise Time		-	50	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	17	-	ns
t_f	Turn-off Fall Time		-	10	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	0.25	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	1	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0V, I_S =0.25A	-	-	1.2	V

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%

Typical Performance Characteristics

Figure1: Output Characteristics

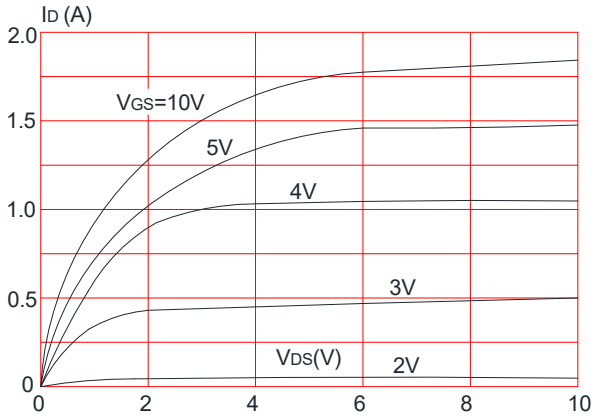


Figure 2: Typical Transfer Characteristics

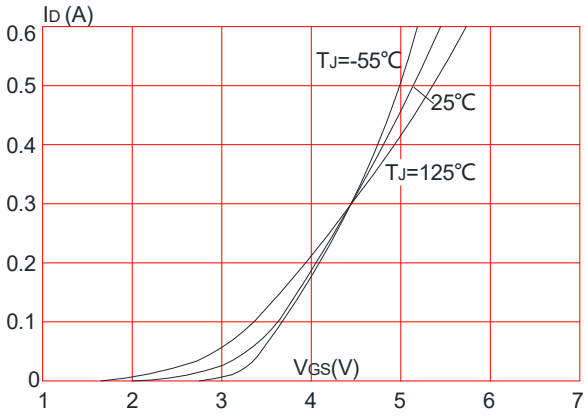


Figure 3: On-resistance vs. Drain Current

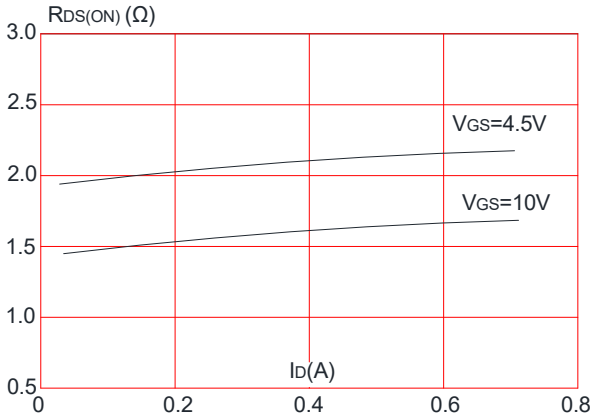


Figure 4: Body Diode Characteristics

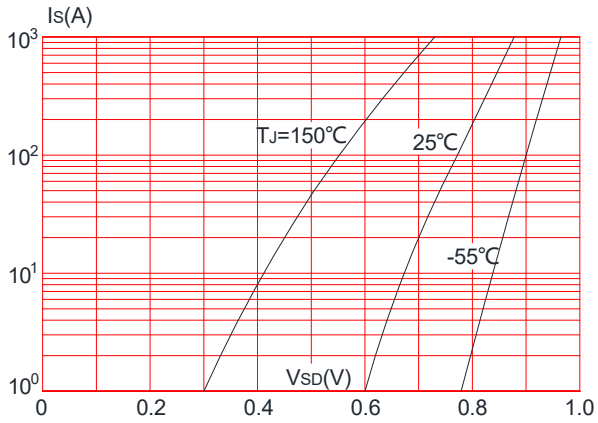


Figure 5: Gate Charge Characteristics

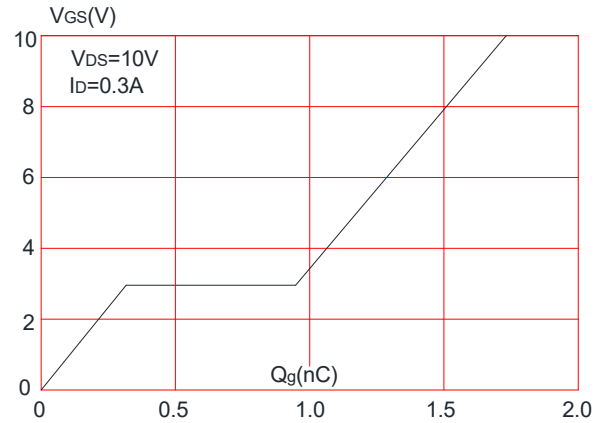


Figure 6: Capacitance Characteristics

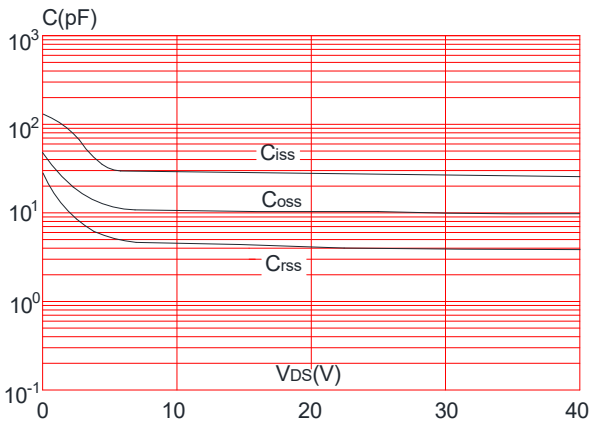


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

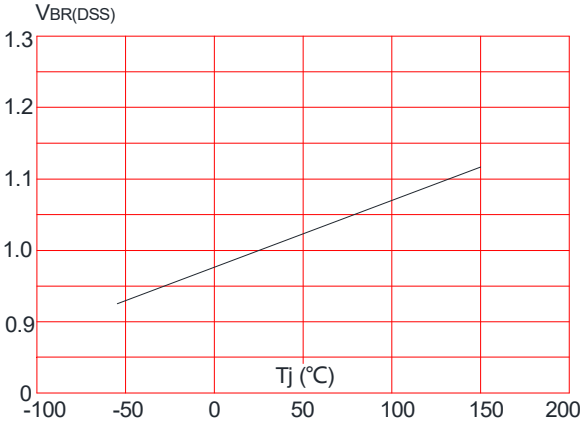


Figure 8: Normalized on Resistance vs. Junction Temperature

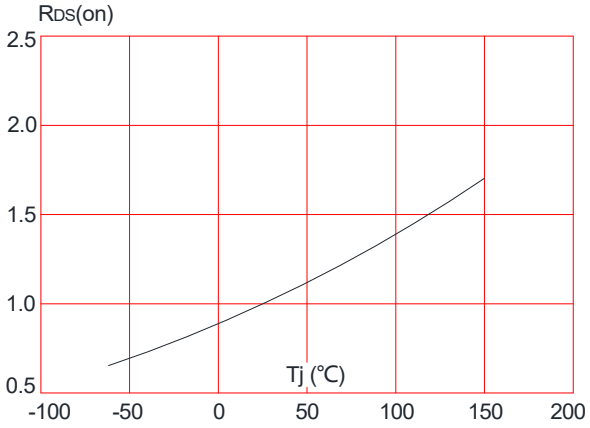


Figure 9: Maximum Safe Operating Area

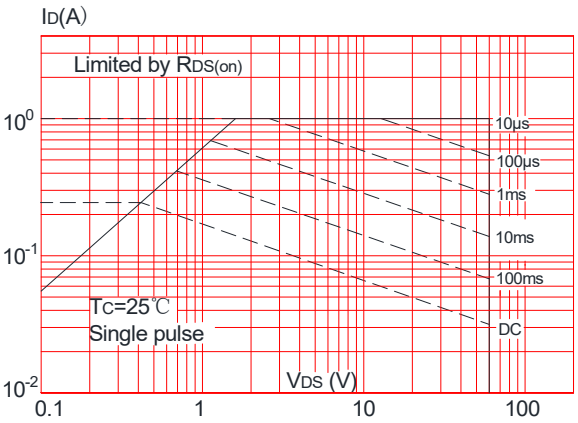


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

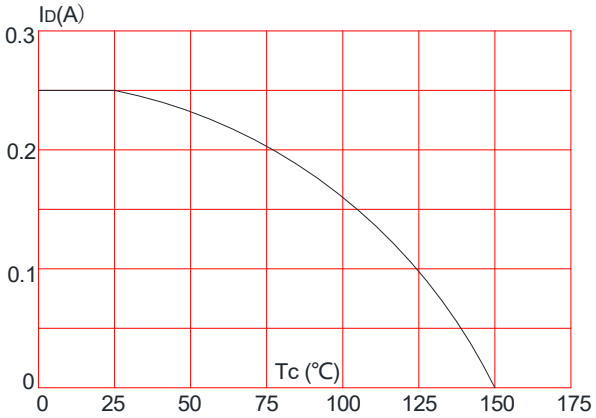
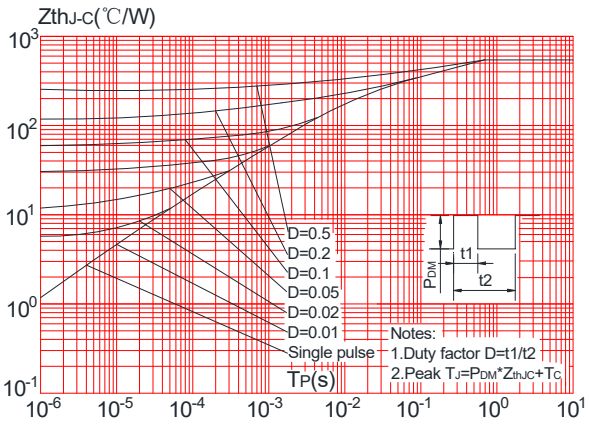


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



Test Circuit

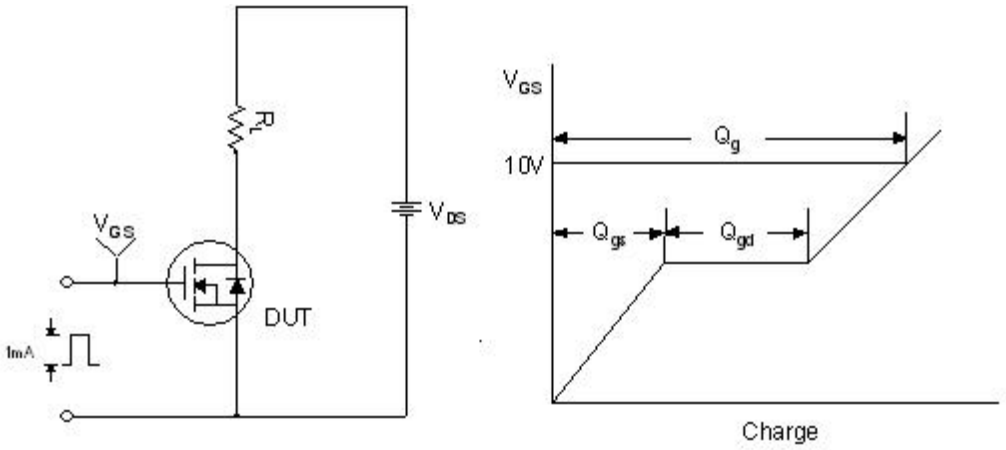


Figure 1. Gate Charge Test Circuit & Waveform

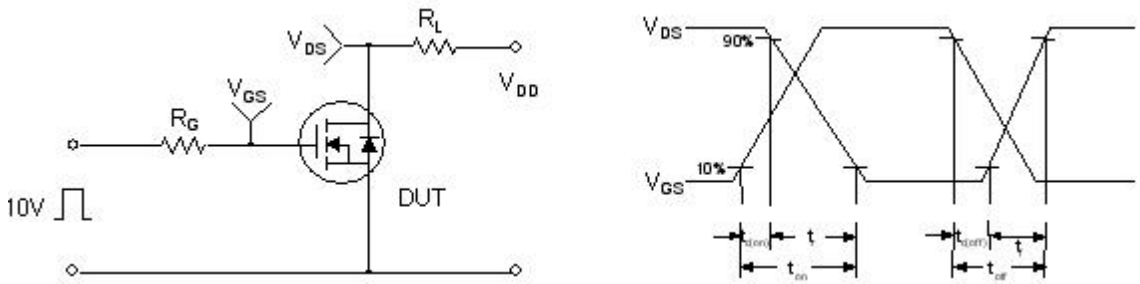


Figure 2. Resistive Switching Test Circuit & Waveforms

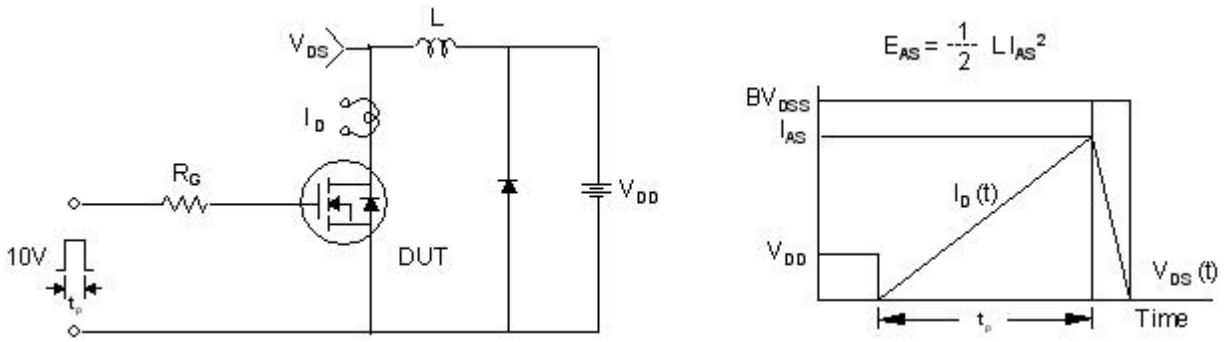
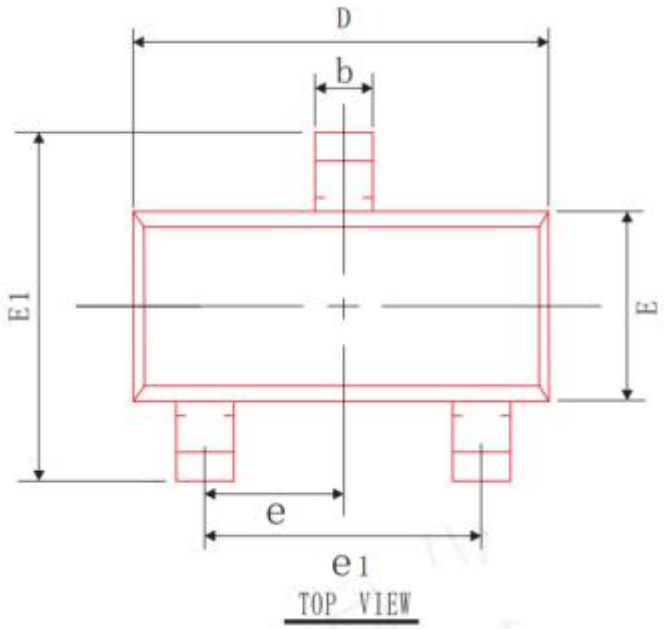
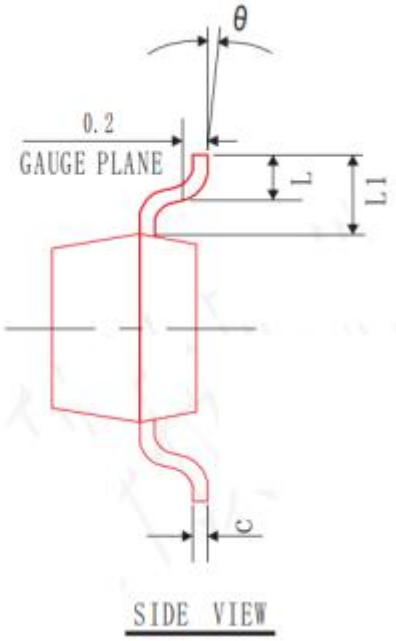
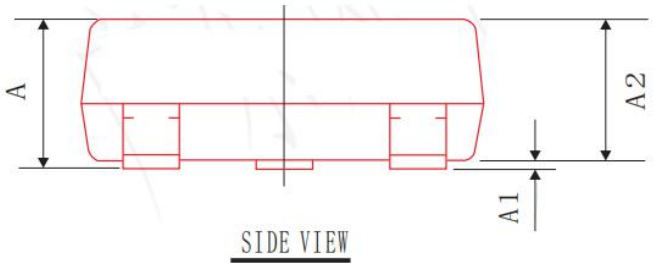


Figure 3. Unclamped Inductive Switching Test Circuit & Waveforms

Package Mechanical Data







SYMBOL	MIN	NOM	MAX
A	0.90	1.05	1.20
A1	0.00	0.05	0.10
A2	0.90	1.00	1.10
b	0.30	0.40	0.50
c	0.08	0.10	0.15
D	2.80	2.90	3.00
E	1.20	1.30	1.40
E1	2.30	2.40	2.50
L	0.30	0.40	0.50
θ	0°	5°	10°
L1	0.55 REF		
e	0.95 BSC		
e_1	1.90 REF		

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