

### Features

- 4.5V to 65V Input Voltage
- Support LED Power up to 60W: 18×3W HBLEDs
- High Contrast Ratio (Minimum Dimming Current Pulse Width <10µS)</li>
- Support Analog Dimming and Thermal Fold-Back
- Constant Switching Frequency Adjustable from 250 kHz to 1000 kHz
- Requires No External Current Sensing Resistor
- Up to 96% Efficiency
- Integrated Low-Side N-Channel MOSFET
- Adjustable Constant LED Current From 350 mA to 1000 mA
- Thermal Shutdown Protection
- Available in ESOP8 package

## Applications

- High Power LED Drivers
- Automotive Lighting

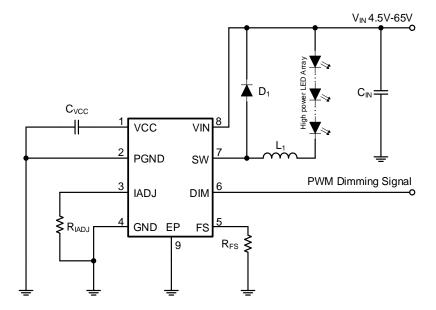
- Architectural Lighting, Office Troffers
- MR-16 LED Lamps

### **General Description**

The RY7614 is 1A 60W common anode-capable constant current buck LED drivers. They are suitable for driving single string of 3W HBLED with up to 96% efficiency. It accepts input voltages from 4.5V to 65V and deliver up to 1A average LED current with  $\pm$ 3% accuracy. The integrated low-side N-channel power MOSFET and current sensing element realize simple and low component count circuitry, as no bootstrapping capacitor and external current-sensing resistor are required. An external small-signal resistor to ground provides very fine LED current adjustment, analog dimming, and thermal fold-back functions.

Constant switching frequency operation eases EMI. No external loop compensation network is needed. The proprietary Pulse-Level-Modulation control method benefits in high conversion efficiency and true average LED current regulation.

## **Typical Application Circuit**

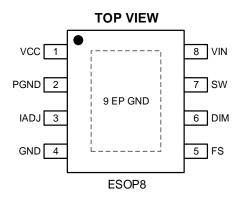


Typical Application Circuit



### Package and Pin Description

### **Pin Configuration**



Top Marking: JH<u>YLL</u> (device code: JH, Y=year code, LL= lot number code)

### **Pin Description**

Pin	Name	Function
1	VCC	Internal Regulator Output Pin. This pin should be by passed to ground by a ceramic capacitor with a minimum value of $1\mu F.$
2	PGND	Power Ground Pin. Ground for power circuitry. Reference point for all stated voltages. Must be externally connected to EP and GND.
3	IADJ	Average Output Current Adjustment Pin. Connect resistor $R_{IADJ}$ from this pin to ground to adjust the average output current.
4	GND	Analog Ground Pin. Analog ground connection for internal circuitry, must be connected to $P_{GND}$ external to the package.
5	FS	Switching Frequency Setting Pin. Connect resistor R <sub>FS</sub> from this pin to ground to set the switching frequency.
6	DIM	PWM Dimming Control Pin. Apply logic level PWM signal to this pin controls the intend brightness of the LED string.
7	SW	Drain of N-MOSFET Switch. Connect this pin to the output inductor and anode of the Schottky diode.
8	VIN	Input Voltage Pin. The input voltage should be in the range of 6V to 65V.
9	EP	Thermal Pad (Power Ground). Used to dissipate heat from the package during operation. Must be electrically connected to PGND external to the package.

### Order Information <sup>(1)</sup>

Marking	Part No.	Model	Description	Package	T/R Qty
JH <u>YLL</u>	70380070	RY7614	RY7614 Async Constant Current HBLED Driver, 4.5-65V, 1A, ESOP8	ESOP8	3000PCS

Note (1): All RYCHIP parts are Pb-Free and adhere to the RoHS directive.



## **Specifications**

### Absolute Maximum Ratings (1) (2)

Item	Min	Max	Unit
V <sub>IN</sub> to GND voltage	-0.3	65	V
V <sub>SW</sub> to GND voltage	-0.3	65	V
DIM to GND	-0.3	6	V
FS, IADJ to GND	-0.3	5	V
Power dissipation <sup>(3)</sup>	Internally Lim	ited	
Operating junction temperature, T <sub>J</sub>	-40	150	°C
Storage temperature, T <sub>stg</sub>	-65	150	°C
Lead Temperature (Soldering, 10sec.)		260	°C

Note (1): Exceeding these ratings may damage the device.

Note (2): The device is not guaranteed to function outside of its operating conditions.

Note (3): The maximum allowable power dissipation is a function of the maximum junction temperature,  $T_{J(MAX)}$ , the junction-to-ambient thermal resistance,  $R_{\theta JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable power dissipation at any ambient temperature is calculated using:  $P_{D(MAX)} = (T_{J(MAX)} - T_A)/R_{\theta JA}$ . Exceeding the maximum allowable power dissipation causes excessive die temperature, and the regulator goes into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at  $T_J=160^{\circ}C$  (typical) and disengages at  $T_J=130^{\circ}C$  (typical).

### **ESD** Ratings

Item	Description	Value	Unit
	Human Body Model (HBM)		
V <sub>(ESD-HBM)</sub>	ANSI/ESDA/JEDEC JS-001-2014	$\pm 2000$	V
	Classification, Class: 2		
	Charged Device Mode (CDM)		
V <sub>(ESD-CDM)</sub>	ANSI/ESDA/JEDEC JS-002-2014	±200	V
	Classification, Class: C0b		
	JEDEC STANDARD NO.78E APRIL 2016		
ILATCH-UP	Temperature Classification,	±150	mA
	Class: I		

### **Recommended Operating Conditions**

Item	Min	Max	Unit
Operating junction temperature <sup>(1)</sup>	-40	125	°C
Operating temperature range	-40	85	°C
Input voltage V <sub>IN</sub>	4.5	65	V
Output Current	0	1	А

Note (1): All limits specified at room temperature ( $T_A = 25^{\circ}C$ ) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).



**RY7614** 

### **Thermal Information**

Item	Description	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)(2)</sup>	48.7	°C/W
R <sub>0JC(top)</sub>	Junction-to-case (top) thermal resistance	52.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.5	°C/W
τιψ	Junction-to-top characterization parameter	8.4	°C/W
Ψјв	Junction-to-board characterization parameter	25.2	°C/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board

## Electrical Characteristics (1) (2)

Parameter	<b>Test Conditions</b>	Min	Тур.	Max	Unit
Input voltage range		4.5		65	V
Supply Current (Quiescent)	Switch Off		6.5		μΑ
Supply Current (Operating)	R <sub>IADJ</sub> =3.125KΩ, V <sub>DIM</sub> =High	2.2	3.3	3.6	mA
Supply Current (Shutdown)	R <sub>IADJ</sub> =3.125KΩ, V <sub>DIM</sub> =Low	0.8	1.2	1.45	mA
Average LED Current	R <sub>IADJ</sub> =3.125KΩ	0.97	1	1.03	А
SW On Resistance			1.8		Ω
Minimum On Time				400	ns
IADJ Pin Voltage		1.23	1.255	1.280	V
Switching Frequency		250	500	1000	KHz
DIM Rising Threshold			1	1.2	V
DIM Falling Threshold		0.7	0.9		V
DIM Threshold Hysteresis			100		mV
	Wake up V <sub>IN</sub> Voltage		3.8	4.2	V
Under-Voltage Lockout Threshold	Shutdown V <sub>IN</sub> Voltage	2.7	3.1		
	Hysteresis V <sub>IN</sub> voltage		700		mV
Thermal Shutdown			160		°C
Thermal Hysteresis			30		°C

T<sub>A</sub>=25°C, unless otherwise specified.

Note (1): MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.

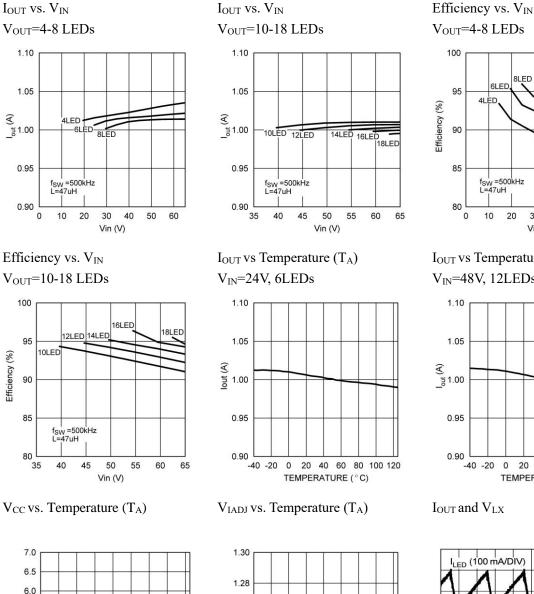
Note (2): Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.





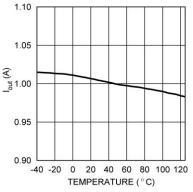
### Typical Performance Characteristics (1) (2)

Note (1): Performance waveforms are tested on the evaluation board. Note (2):  $V_{IN} = 48V$ , ILEDs=1A,  $T_A = +25^{\circ}C$ , unless otherwise noted.

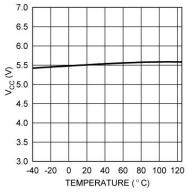


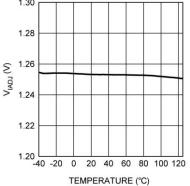
Εſ 6LED 4LED f<sub>SW</sub> =500kHz L=47uH 10 20 60 30 40 50 Vin (V)

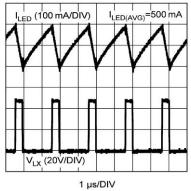
 $I_{OUT}$  vs Temperature (T<sub>A</sub>) V<sub>IN</sub>=48V, 12LEDs



#### Iout and VLX



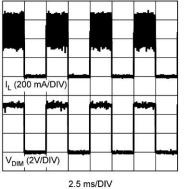






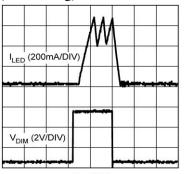
#### $I_{\mathrm{LX}}$ and $V_{\mathrm{DIM}}$

LED Current with PWM Dimming  $(V_{DIM} Rising)$ 

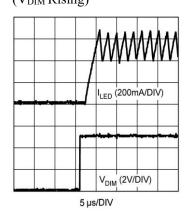


# LED Current with PWM Dimming

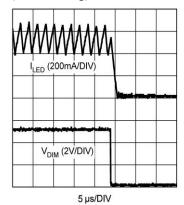
(V<sub>DIM</sub> Rising)



5 µs/DIV

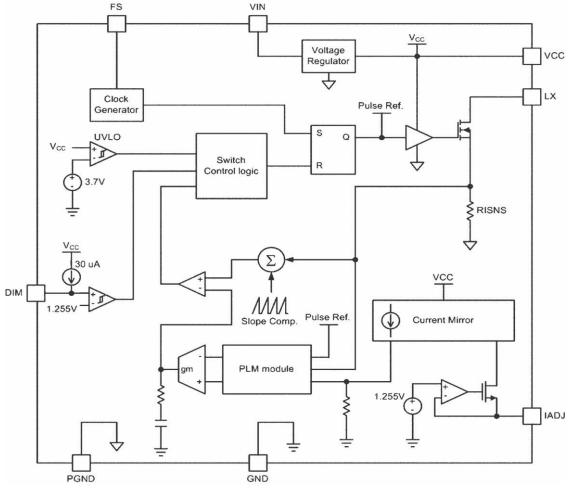


LED Current with PWM Dimming (V<sub>DIM</sub> Falling)





### **Functional Block Diagram**



Block Diagram

### **Functions Description**

### **Under-Voltage Lockout (UVLO)**

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. When the voltage is higher than UVLO threshold voltage, the device is enabled again.

### **Enable and Disable**

The DIM pin of the RY7614 is an input with internal pullup that accepts logic signals for average LED current control. Applying a logic high (greater than 1.2 V) signal to the DIM pin or leaving the DIM pin open will enable the device. Applying a logic low signal (less than 0.9 V) to the DIM pin will disable the switching activity of the device but maintain VCC regulator active. The 7614 allows the inductor current to slew up to the preset regulated level at full speed instead of charging the inductor with multiple restrained switching duty cycles.



### **Minimum Switch On-Time**

As the RY7614 features a 400 ns minimum ON time, it is essential to make sure the ON time of the internal switch is not shorter than 400 ns when setting the LED driving current. If the switching ON time is shorter than 400 ns, the accuracy of the LED current may not maintain and exceed the rated current of the LEDs.

### **Peak Switch Current Limit**

The RY7614 features an integrated switch current limiting mechanism that protects the LEDs from being overdriven. The switch current limiter triggers when the switch current exceeds three times the current level set by  $R_{IADJ}$ . Once the current limiter is triggered, the internal power switch turns OFF to allow the inductor to discharge and cycles repetitively until the overcurrent condition is removed. The current limiting feature is exceptionally important to avoid permanent damage of the application circuit due to short circuit of LED string.

### **Analog Dimming Control**

The IADJ pin can be used as an analog dimming signal input. As the average output current of the RY7614 depends on the current being drawn from the IADJ pin, thus the LED current can be increased or decreased by applying external bias current to the IADJ pin.

### **Thermal Shutdown**

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, it shuts down the whole chip. When the temperature falls below its lower threshold (Typ. 130°C) the chip is enabled again.

### **Applications Information**

### Setting the LED Current

The RY7614 requires no external current sensing resistor for LED current regulation. The average output current of the RY7614 is adjustable by varying the resistance of the resistor,  $R_{IADJ}$  that connects across the IADJ and GND pins. The IADJ pin is internally biased to 1.255 V. The LED current is then governed by following Equation:  $I_{LED} =$ 

```
\frac{3125 \times 10^3}{R_{IADI}} mA, Where 350mA<I<sub>LED</sub><1A.
```

ILED (MA)	R <sub>1</sub> (KΩ)
350	8.93
500	6.25
700	4.46
1000	3.13

The LED current can be set to any level in the range from 350 mA to 1A. When the overcurrent protection is activated, current regulation cannot be maintained until the overcurrent condition is cleared.

### Setting the Switch Frequency

RY7614 is PWM LED drivers that contain a clock generator to generate constant switching frequency for the device. The switching frequency is determined by the resistance of an external resistor  $R_{FS}$  in the range of 250 kHz to 1MHz. Lower resistance of  $R_{FS}$  results in higher switching frequency. The switching frequency of the RY7614 is governed using Equation:



$$f_{SW} = \frac{20 \times 10^6}{R_{FS}} KHz$$

Calculate the value of  $R_{FS}$  for 500-kHz switching frequency using a standard value of  $RFS = 40.2k\Omega$ .

f <sub>SW</sub> (KHz)	R <sub>FS</sub> (KΩ)
250	80
500	40
1000	20

#### **Inductor Selection**

To ensure proper output current regulation, the RY7614 must operate in Continuous Conduction Mode (CCM). With the incorporation of PLM, the peak-to-peak inductor current ripple can be set as high as  $\pm 60\%$  of the defined average output current. The minimum inductance of the inductor is decided by the defined average LED current and allowable inductor current ripple. Calculate the minimum inductor value required for 600 mA or less peak-to-peak LED current ripple using Equation:

$$L_{MIN} = \frac{(V_{IN} - V_{LED}) \times V_{LED}}{f_{SW} \times V_{IN} \times \Delta i_{L-PP}}$$

Choose a higher standard value of  $L = 47 \mu H$ .

#### **Output Capacitor Selection**

The device is designed to operate with a wide selection of ceramic output capacitors. The selection of the output capacitor value is a trade-off between output voltage ripple and capacitor cost and form factor. In general, capacitor values of  $2.2\mu$ F up to  $10\mu$ F can be used. For better voltage filtering, ceramic capacitors with low ESR are recommended. X5R and X7R types are suitable because of their wider voltage and temperature ranges.

#### **Input Capacitor Selection**

For good input voltage filtering, low ESR ceramic capacitors are recommended. A  $4.7\mu$ F ceramic input capacitor is sufficient for most of the applications. For better input voltage filtering and EMI reduction, this value can be increased. The input capacitor should be placed as close as possible to the input pin of the converter.

#### **Diode Selection**

A Schottky diode should be used for the output diode. The forward current rating of the diode should be higher than the load current, and the reverse voltage rating must be higher than the output voltage. Do not use ordinary rectifier diodes, since slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer.



### Layout Guidelines

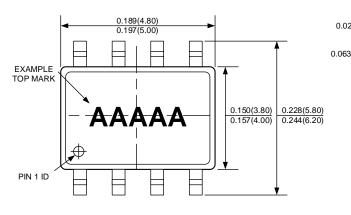
PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

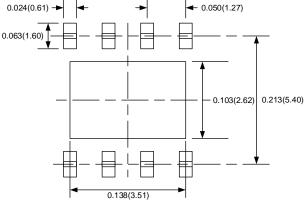
- 1. Minimize area of switched current loops. Input capacitor should be placed as close as possible to the VIN terminal. Grounding for both the input and output capacitors should consist of a small localized topside plane that connects to GND. The inductor should be placed as close as possible to the SW pin and output capacitor.
- 2. Minimize the copper area of the switch node. The SW terminals should be directly connected with a trace that runs on top side directly to the inductor. To minimize IR losses this trace should be as short as possible and with an enough width. However, a trace that is wider than 100 mils will increase the copper area and cause too much capacitive loading on the SW terminal. The inductors should be placed as close as possible to the SW terminals to further minimize the copper area of the switch node.
- 3. Have a single point ground for all device analog grounds. The ground connections for the feedback components should be connected then routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground plane. If not properly handled, poor grounding can result in degraded load regulation or erratic switching behavior.
- 4. Minimize trace length to the FB terminal. The feedback trace should be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise.
- 5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. If voltage accuracy at the load is important make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.



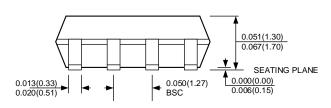
### **Package Description**

### **ESOP8 (EXPOSED PAD)**

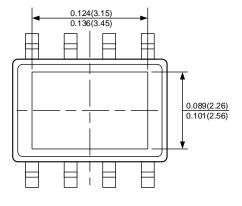




TOP VIEW

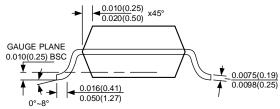


FRONT VIEW



**BOTTOM VIEW** 





SIDE VIEW

NOTE:

1. CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.

2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH,

PROTRUSIONS OR GATE BURRS. 3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.

4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING)

SHALL BE 0.004" INCHES MAX. 5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA. 6. DRAWING IS NOT TO SCALE.