# Over Voltage Protection IC with Surge Protection

## General Description

The LP5280 series is a highly integrated circuit, it used to protect low voltage system from abnormal high input voltage. The IC continuously checks the input voltage. When the protection status is occur, the power MOS will turn off at the same time. The LP5280 series is safety devices to ensure worked against accidents.

In case of the OVLO pin voltage exceeds an Over-Voltage Protection (OVP) threshold voltage level, the internal power MOS will turn off within 1μs. Input voltage OVP threshold could be used to set by external resistors divider. Also, LP5280 has an input 6.8V-OVP, LP5280A was 5.95V-OVP, LP5280B was 10.5V-OVP, and LP5280C was 14V-OVP, which could be select by connecting OVLO pin to ground.

Other features include over temperature protection and under-voltage lockout (UVLO). The LP5280 series is available in a space saving WLCSP 12-ball (0.4mm pitch) package.

## Order Information

LP5280□□□□
- F: Green
- Package Type
  - HV: WLCSP-12
- OVP Level
  - Non :6.8V
  - A :5.95V
  - B :10.5V
  - C :14V

## Features

- Withstand High Input Voltage Up to 29V
- Input Over Voltage Protection
  - Internal Input OVP=6.8V(Typ.) @LP5280
  - Internal Input OVP=5.95V(Typ.) @LP5280A
  - Internal Input OVP=10.5V(Typ.) @LP5280B
  - Internal Input OVP=14V(Typ.) @LP5280C
- OVP Response Time=40ns(Typ.)
- 4.8A Current Capability
- Power MOS $R_{DS(ON)}$=25mΩ(Typ.)
- Fault Signal Output
- Enable Control
- Under Voltage Lockout
- Over-Temperature Protection
- IEC61000-4-5 Surge >100V
- Available in WLCSP12
- RoHS Compliant and Halogen Free

## Applications

- Mobile Handsets and Tablets
- Portable Media Players
- MP3 Players
- Charging Ports

## Marking Information

| Device | Marking | Package | Shipping |
|---|---|---|---|
| LP5280HVF | LPS<br>LP5280<br>YWX | WLCSP-12 | 3K/REEL |
| LP5280AHVF | LPS<br>LP5280A<br>YWX | WLCSP-12 | 3K/REEL |
| LP5280BHVF | LPS<br>LP5280B<br>YWX | WLCSP-12 | 3K/REEL |
| LP5280CHVF | LPS<br>LP5280C<br>YWX | WLCSP-12 | 3K/REEL |
| Y: Y is year code. W: W is week code. X: X is series number. | | | |

## Typical Application Circuit

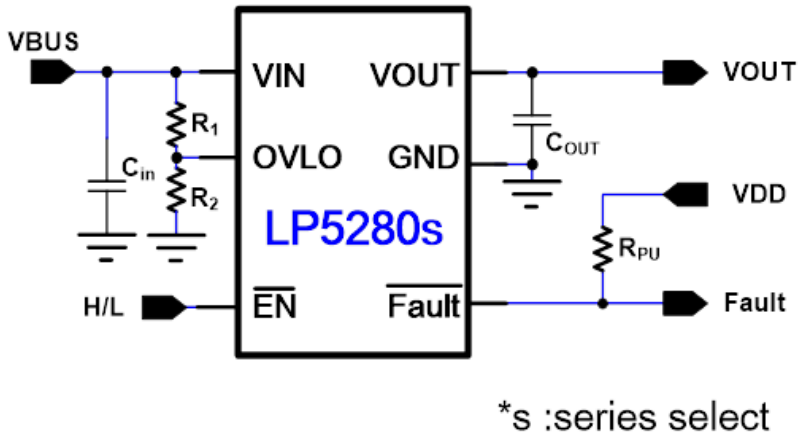



Figure 1. Typical Application Circuit of LP5280 series

## Pin Configuration

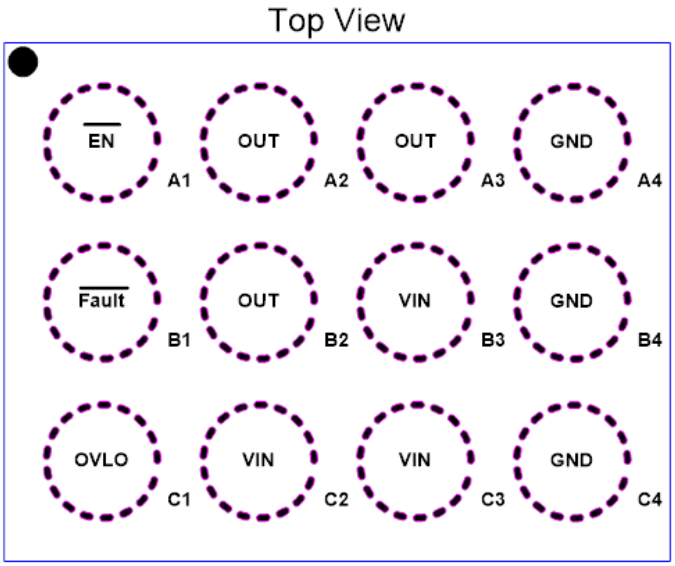



Figure 2. Package Top View

## Function Block Diagram

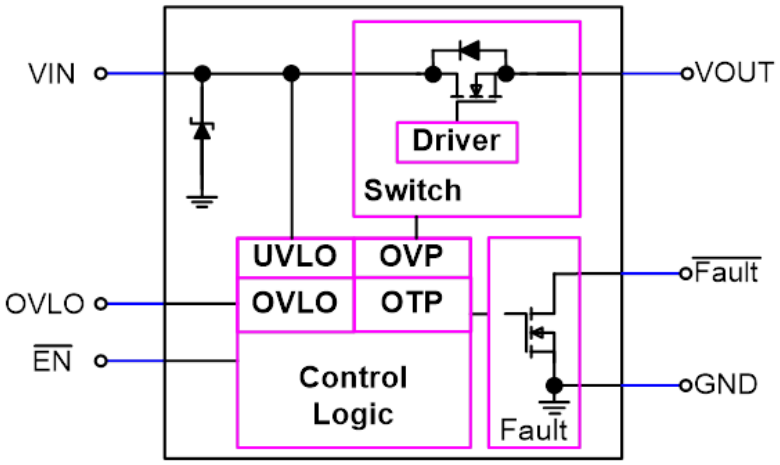



Figure 3. Function Block Diagram

## Functional Pin Description

| Pin NO. | WLCSP | Description |
|---|---|---|
| VIN | B3,C2,C3 | Power Source Input. Connect a ceramic capacitor between VIN and GND. |
| GND | A4,B4,C4 | Ground. |
| $\overline{\text{Fault}}$ | B1 | Fault Function Pin. Open drain connected to a resistor. |
| $\overline{\text{EN}}$ | A1 | Enable Pin. |
| OVLO | C1 | Over Voltage Lockout. Adjustment Pin. |
| VOUT | A2,A3,B2 | Output through the power MOSFET. |

## Absolute Maximum Ratings Note1

- ✧ VIN to GND ---------- -0.3V to +29V
- ✧ VOUT to GND ---------- -0.3V to +29V
- ✧ OVLO to GND ---------- -0.3V to +24V
- ✧ All Other Pin to GND ---------- -0.3V to +6V
- ✧ Maximum External Over Voltage Lockout Setting ---------- 14V
- ✧ Operating Junction Temperature Range ($T_J$) ---------- -40℃ to 150℃
- ✧ Operation Ambient Temperature Range ---------- -40°C to +105°C
- ✧ Storage Temperature Range ---------- -55°C to +150°C
- ✧ Maximum Soldering Temperature (at leads, 10sec) ---------- +260°C

**Note1.** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Electrical Characteristics

($T_A$ = 25°C, $V_{IN}$ = 5V, VEN=0V, OVLO=0V, CIN=0.1uF, and COUT=1uF. Unless Otherwise Specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **General Function** | | | | | | |
| Input Clamp Voltage | $V_{IN\_Clamp}$ | | | 31 | | V |
| Power Source Voltage | $V_{IN}$ | $T_J$= +25 °C | 2.5 | 5 | 28 | V |
| Input UVLO Threshold | $V_{UVLO}$ | $V_{IN}$ Rising | | 2.25 | | V |
| UVLO Threshold Hysteresis | $\Delta V_{UVLO}$ | Falling Hysteresis | | 150 | | mV |
| Power On Deglitch Time | $T_{Deglitch}$ | From VIN>UVLO to 10%VOUT, $\overline{EN}$ Low | | 20 | | ms |
| Soft Start Time | $T_{SS}$ | From VIN>UVLO to $\overline{Fault}$ low, $\overline{EN}$ Low | | 30 | | ms |
| Power Source Current at Operation | $I_{IN}$ | $V_{IN}$=5V, $\overline{EN}$=L | | 67 | | μA |
| Power Source Current at OV Condition | $I_{IN\_OVLO}$ | $V_{IN}$=5V, $\overline{EN}$=L, OVLO=3V | | 70 | | μA |
| Thermal Shutdown Threshold | $T_{SD}$ | | | 130 | | °C |
| Thermal Shutdown Threshold Hysteresis | $\Delta T_{SD}$ | | | 20 | | °C |
| **Logic Function** | | | | | | |
| $\overline{EN}$ Threshold Voltage | $V_{ENH}$ | | 1 | | | V |
| | $V_{ENL}$ | | | | 0.5 | V |
| $\overline{EN}$ Input Resistance to GND | $I_{EN}$ | $\overline{EN}$=5V | | | 5 | uA |
| $\overline{Fault}$ Output Logic Low | | Sink 1mA | | | 0.4 | V |
| $\overline{Fault}$ Logic High Leakage Current | | $\overline{Fault}$=5V | -0.5 | | 0.5 | uA |
| **Power MOS** | | | | | | |
| Switch On Resistance | $R_{DS(ON)}$ | $I_{OUT}$=1A | | 25 | | mΩ |
| Switch Turn on Time | $T_{ON}$ | $R_{OUT}$=100 Ω, $C_{OUT}$=22uF, $V_{OUT}$ from 0.1$V_{IN}$ to 0.9$V_{IN}$ | | 1 | | ms |
| Switch Turn off Time | $T_{OFF}$ | $R_{OUT}$=100 Ω, $C_{OUT}$=Non, Trigger OVLO to stop $V_{OUT}$ | | 40 | | ns |
| **External OVLO Function** | | | | | | |
| OVLO Leakage Current | $I_{OVLO}$ | | -0.1 | | +0.1 | uA |
| External OVLO Set Threshold | $V_{EOVLO}$ | | | 1.2 | | V |
| External OVLO select Threshold | $V_{EOV\_H}$ | | | 0.4 | | V |
| External OVLO select Threshold Hysteresis | $V_{EOV\_L}$ | | | 0.3 | | V |

## Electrical Characteristics

($V_{IN}$ = 5V, $T_A$ = 25°C, Unless Otherwise Specified)

| Parameter | Symbol | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **Internal OVLO Functions** | | | | | | | |
| Input Over Voltage Protect threshold | $V_{IOVLO}$ | LP5280 | $V_{IN}$ Rising | 6.6 | 6.8 | 7 | V |
| | | | $V_{IN}$ Falling | 6.51 | 6.65 | | V |
| | | LP5280A | $V_{IN}$ Rising | 5.83 | 5.95 | 6.07 | V |
| | | | $V_{IN}$ Falling | 5.73 | 5.85 | | V |
| | | LP5280B | $V_{IN}$ Rising | 10.3 | 10.5 | 10.7 | V |
| | | | $V_{IN}$ Falling | 10.1 | 10.3 | | V |
| | | LP5280C | $V_{IN}$ Rising | 13.7 | 14 | 14.3 | V |
| | | | $V_{IN}$ Falling | 13.4 | 13.7 | | V |

## Timing Diagram

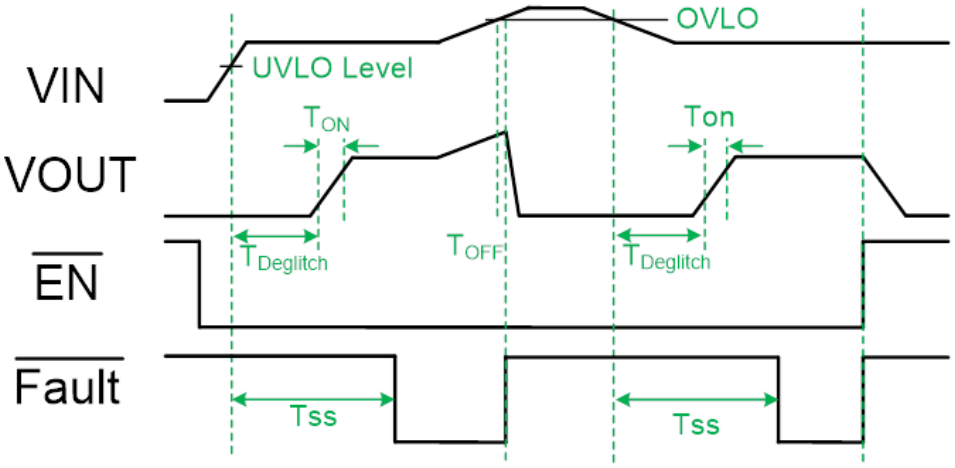



Figure 4. Power Sequence

# Application Information

The LP5280 series devices monitor the input voltage to protect the OTG system of a Li-Ion battery. When enabled, the system is protected against input overvoltage by turning off an internal switch, immediately removing power from the charging circuit. Additionally, the device also monitors its own temperature and switches off if device too hot.

## Under Voltage Lockout (UVLO)

The LP5280 series had an UVLO internal circuit that enables the device once the voltage on the $V_{IN}$ voltage exceeds the UVLO threshold voltage.

## Surge Protection

The LP5280 series integrates a clamp circuit to suppress input surge voltage. For surge voltages large than $V_{OVLO}$ and small than $V_{IN\_Clamp}$, the switch will be turned off and the clamp circuit is not work. For surge voltages greater than $V_{IN\_Clamp}$, the internal clamp circuit will detect surge voltage level and discharge the surge energy to ground. The device can suppress surge voltages up to 100V.

## Over Temperature Protection

The LP5280 series device enters over temperature protection (OTP) if its junction temperature exceeds 130°C (Typ.). During over temperature protection none of the device's functions are available. To resume normal operation the junction temperature need cool down, and the outputs will restart.

## Enable Control

The LP5280 series has an enable pin which can be used to enable or disable the device. When the EN pin is driven high, the switch is turned off. The EN pin has an internal pull-down resistor can be floating.

## Fault Output

The FAULT pin is open-drain output.

- Input Over Voltage
- OVLO Voltage Threshold
- Over Temperature

## External Over Voltage Lockout

The power MOS will be turned off whenever input voltage higher than $V_{IOVLO}$. The value of $V_{OVLO}$ can be set by external resistor divide or just be internal set value $V_{IOVLO}$.

When $V_{OVLO}$ is smaller than $V_{EOV\_L}$, $V_{OVLO}$ will be decided by $V_{IOVLO}$. When $V_{OVLO}$ is larger than $V_{EOV\_H}$, the power switch will be turned off once $V_{OVLO}>V_{EOVLO}$. The external resistor divide can be decided according to the following equation:

$$V_{OVLO}=(R1/R2+1) \times V_{EOVLO}$$

The setting value of $V_{EOVLO}$ should not be higher than 14V.

## Layout Consideration

The proper PCB layout and component placement are critical for all circuit. LP5280 series is meant to protect downstream circuit. Here are some suggestions to the layout design.

1. Route power line on PCB as straight, wide and short as possible.
2. Connected all ground together with one uninterrupted ground plane.
3. The input and output capacitor should be located as closed as possible to the chip and ground plane.
4. Other components should be located close to the chip.
5. The power trace from connector to device may suffer from ESD event; keep other traces away from it to minimize possible EMI and ESD coupling.

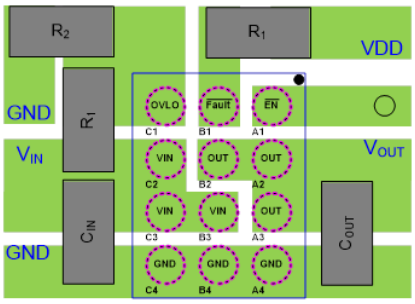
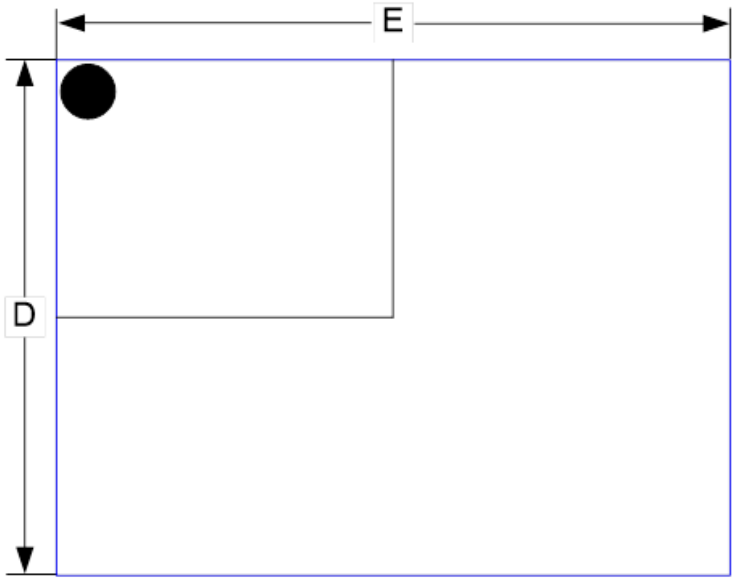



Figure 5. Recommended PCB Layout Diagram

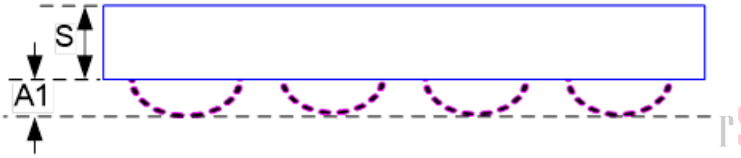
# Packaging Information

**WLCSP-12-ball Package(1.3×1.78) pitch 0.4 (Unit: mm)**

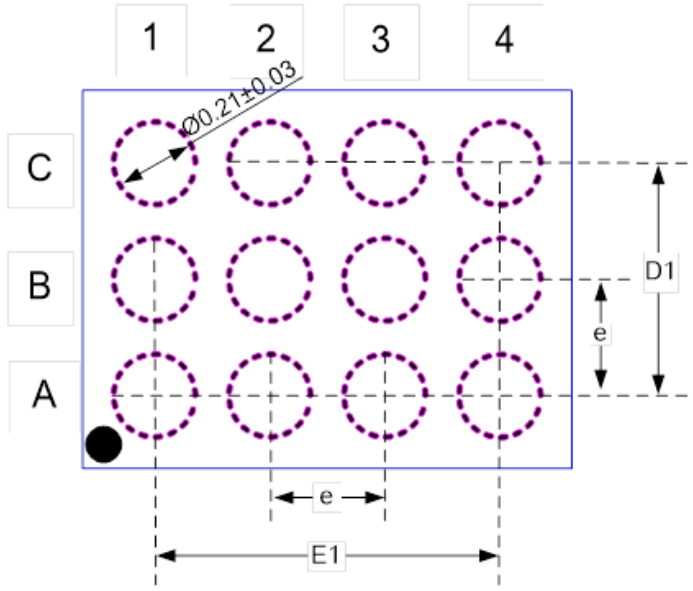



TOP VIEW

| SYMBOLSUNIT | DIMENSION IN MILLIMETER | | |
|---|---|---|---|
| | MIN | TYP | MAX |
| D | 1.30 | 1.33 | 1.36 |
| E | 1.77 | 1.79 | 1.82 |
| S | 0.37 | 0.38 | 0.39 |
| D1 | | 0.8 | |
| E1 | | 1.2 | |
| A1 | 0.14 | 0.165 | 0.18 |
| e | | 0.4 | |




SIDE VIEW




BOTTOM VIEW