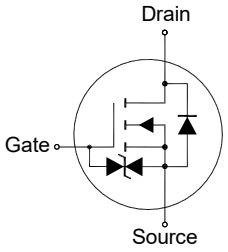
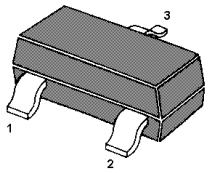
MMBT7002K

N-Channel Enhancement Mode MOSFET

Features

- Low on resistance $R_{DS(ON)}$
- Low gate threshold voltage
- Low input capacitance
- ESD protected up to 2KV





1.Gate 2.Source 3.Drain
TO-236 Plastic Package

Absolute Maximum Ratings (at T_a = 25℃ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	V
Gate-Source Voltage	V_{GSS}	± 20	V
Drain Current (Continuous)	I_D	300	mA
Drain Current (Pulse Width ≤ 10 μs)	I_{DM}	800	mA
Total Power Dissipation	P_{tot}	350	mW
Operating and Storage Temperature Range	T_j, T_{stg}	- 55 to + 150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance-Junction to Ambient [1)]	$R_{\theta JA}$	357	℃/W

[1)] Device mounted on FR-4 substrate PC board, with minimum recommended pad layout.

Dated: 08/09/2020 Rev: 07

Characteristics at T_a = 25℃ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain Source Breakdown Voltage at I_D = 10 µA	BV_{DSS}	60	-	-	V
Zero Gate Voltage Drain Current at V_{DS} = 60 V	I_{DSS}	-	-	1	µA
Gate Source Leakage Current at V_{GS} = ± 20 V	I_{GSS}	-	-	± 10	µA
Gate Threshold Voltage at V_{DS} = V_{GS}, I_D = 250 µA	$V_{GS(th)}$	1	-	2.5	V
Static Drain Source On-Resistance at V_{GS} = 10 V, I_D = 500 mA at V_{GS} = 4.5 V, I_D = 200 mA	$R_{DS(ON)}$	- -	- -	3 4	Ω
DYNAMIC PARAMETERS					
Forward Transconductance at V_{DS} = 10 V, I_D = 200 mA	g_{FS}	80	-	-	mS
Gate Resistance at V_{GS} = 0 V, V_{DS} = 0 V, f = 1MHz	R_g	-	200	-	Ω
Input Capacitance at V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	22.5	50	pF
Output Capacitance at V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	-	9	25	pF
Reverse Transfer Capacitance at V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	-	7.5	10	pF
Gate charge total at V_{DS} =10 V, I_D = 0.5 A, V_{GS} = 4.5 V	Q_g	-	0.44	-	nC
Gate to Source Gate Charge at V_{DS} =10 V, I_D = 0.5 A, V_{GS} = 4.5 V	Q_{gs}	-	0.2	-	nC
Gate to Drain Charge at V_{DS} =10 V, I_D = 0.5 A, V_{GS} = 4.5 V	Q_{gd}	-	0.1	-	nC
Turn-On Delay Time at V_{DS} = 30 V, V_{GS} = 10 V, I_D = 0.5 A, R_G = 25 Ω	$t_{d(on)}$	-	2.7	-	ns
Turn-On Rise Time at V_{DS} = 30 V, V_{GS} = 10 V, I_D = 0.5 A, R_G = 25 Ω	t_r	-	2.5	-	ns
Turn-Off Delay Time at V_{DS} = 30 V, V_{GS} = 10 V, I_D = 0.5 A, R_G = 25 Ω	$t_{d(off)}$	-	13	-	ns
Turn-Off Fall Time at V_{DS} = 30 V, V_{GS} = 10 V, I_D = 0.5 A, R_G = 25 Ω	t_f	-	8	-	ns
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at V_{GS} = 0 V, I_S = 0.5 A	V_{SD}	-	0.85	-	V
Body Diode Reverse Recovery Time at I_S = 0.5 A, di/dt = 100 A / µs	t_{rr}	-	30	-	ns
Body Diode Reverse Recovery Charge at I_S = 0.5 A, di/dt = 100 A / µs	Q_{rr}	-	29	-	nC

Electrical Characteristics Curves

Fig. 1 Typical Output Characteristic

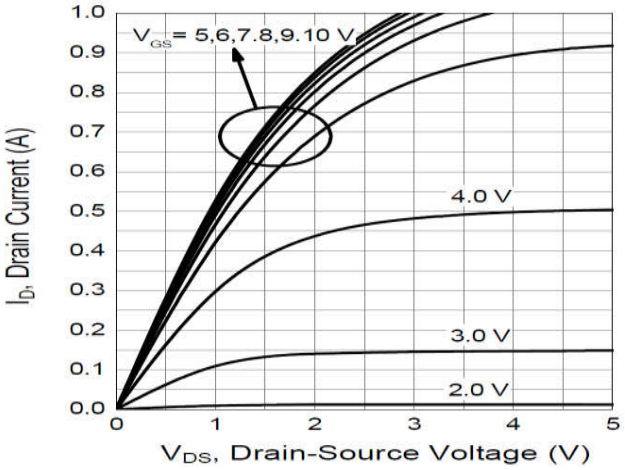


Fig. 2 Typical Transfer Characteristics

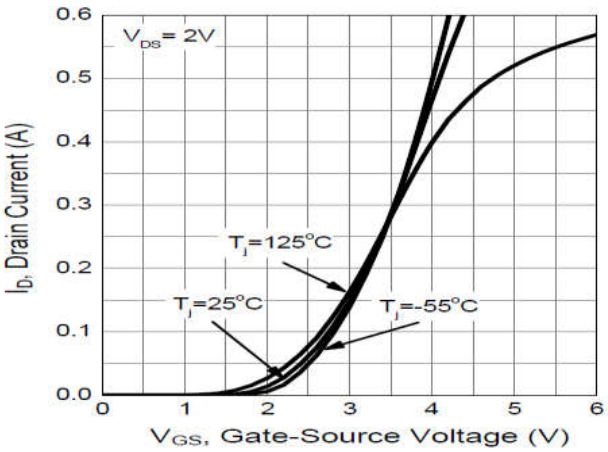


Fig. 3 Gate-Source Voltage vs.$R_{DS(on)}$

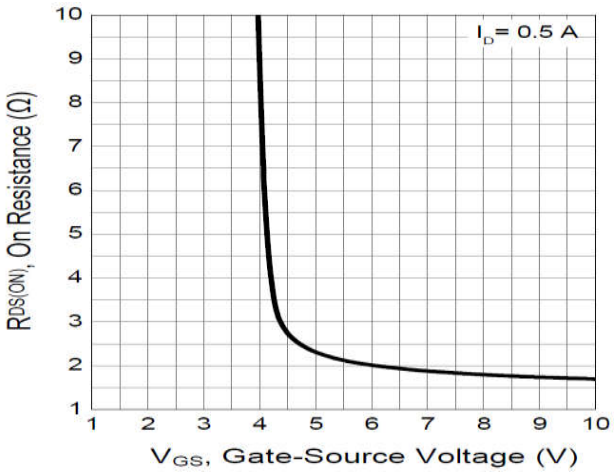


Fig. 4 on-Resistance vs.T_j

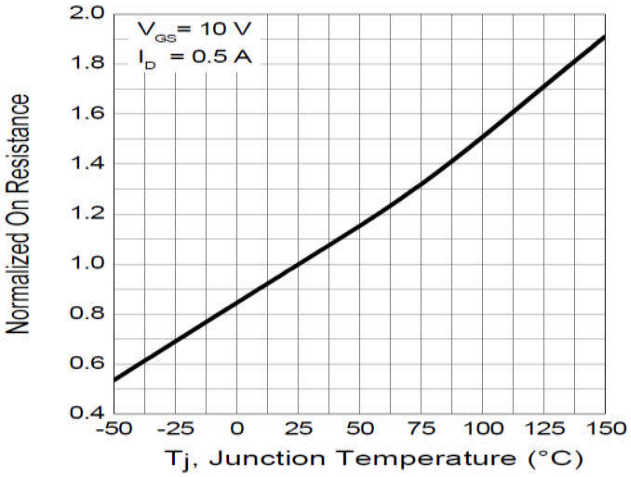


Fig. 5 Drain Current vs. on-Resistance

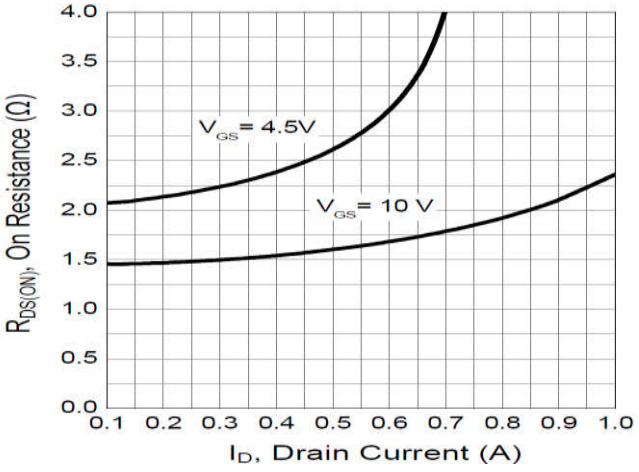
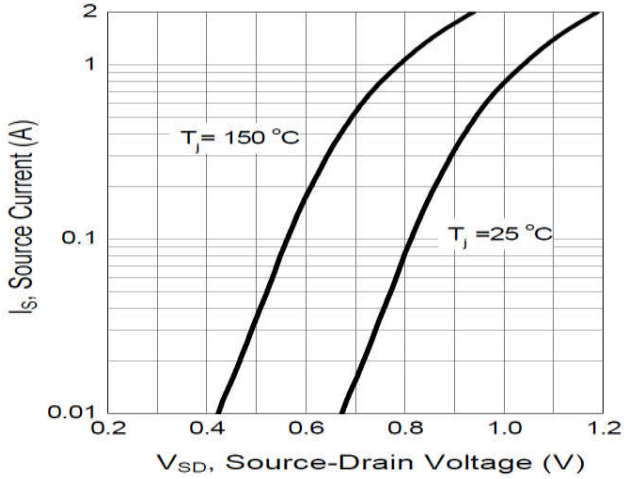


Fig. 6 Typical Forward Characteristic



Electrical Characteristics Curves

Fig. 7 Typical Junction Capacitance

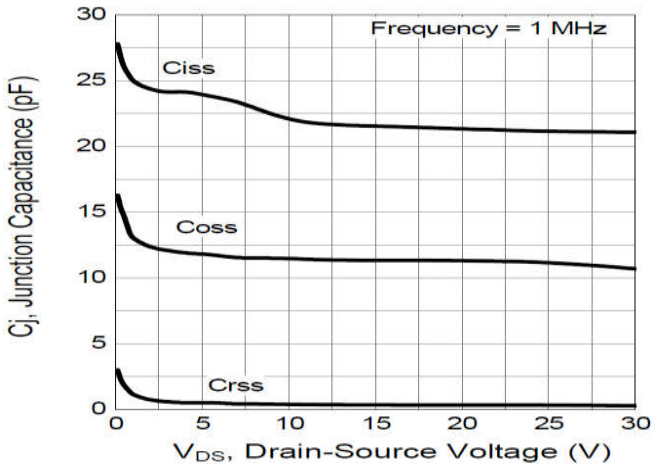


Fig. 8 Gate Charge

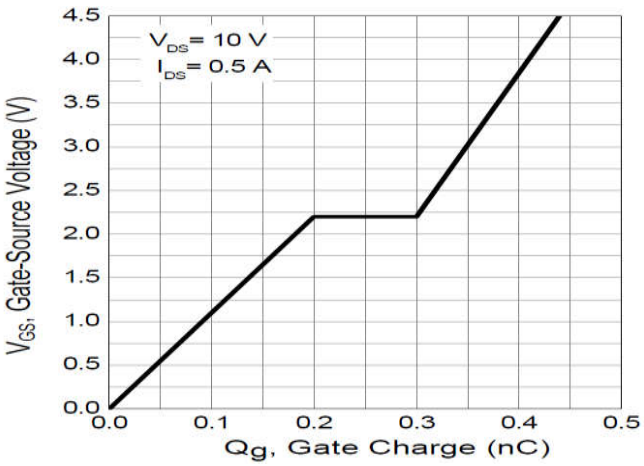
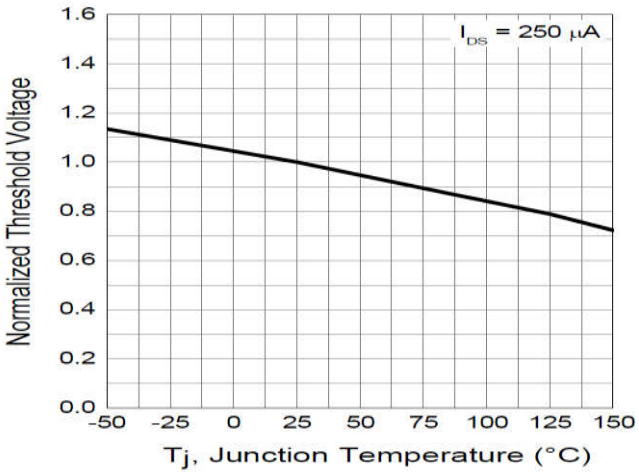


Fig. 9 Gate Threshold Variation vs. T_j



Test Circuits

Fig.1-1 Switching times test circuit

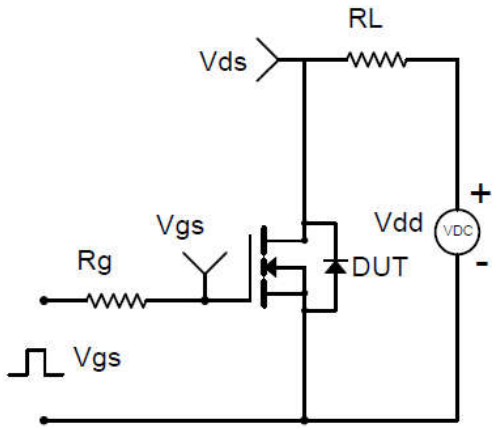


Fig.1-2 Switching Waveform

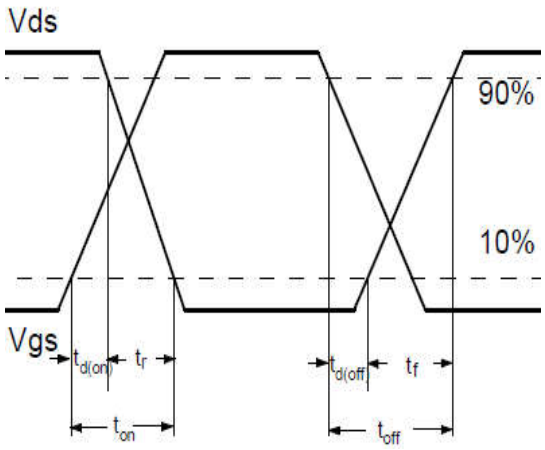


Fig.2-1 Gate charge test circuit

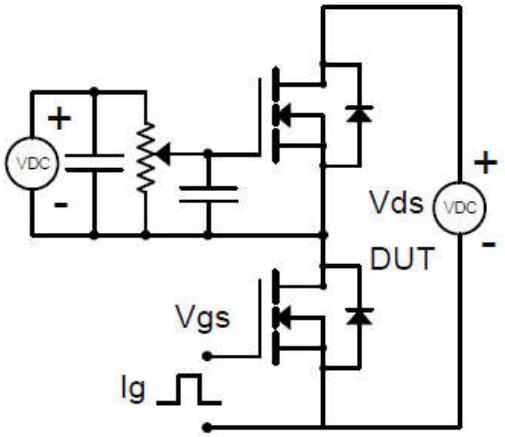
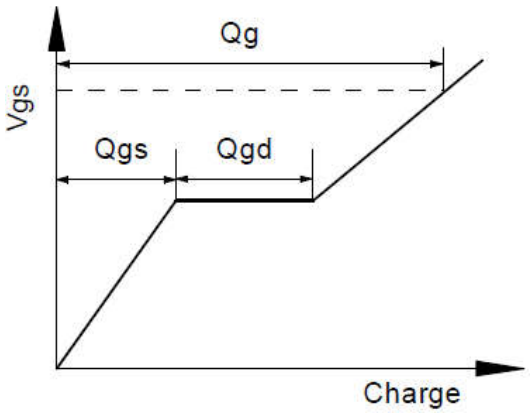
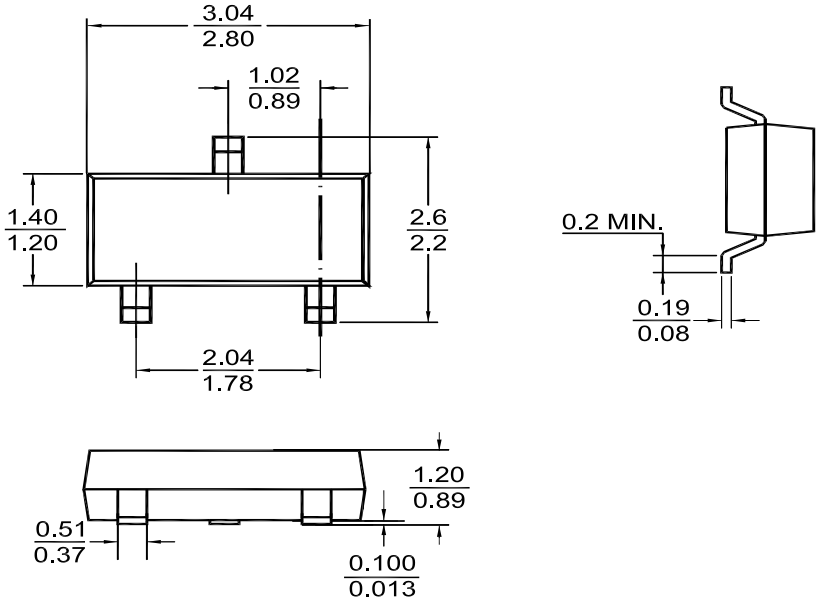


Fig.2-2 Gate charge waveform

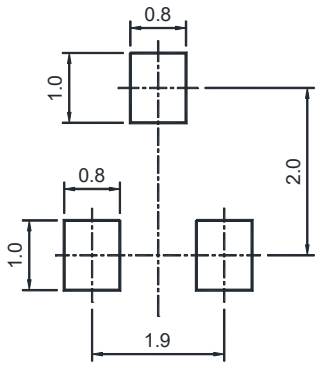


PACKAGE OUTLINE

Plastic surface mounted package (Dimensions in mm) **TO-236**



Recommended Soldering Footprint



Packing information

Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
TO-236	8	4 ± 0.1	0.157 ± 0.004	178	7	3,000

Marking information

" K72 " = Part No.

"YM" = Date Code Marking

"Y" = Year

"M" = Month

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