Data Sheet

BCM5325E

Integrated 10/100BASE-T/TX Six-Port Switch

GENERAL DESCRIPTION

The BCM5325E is a six-port 10/100BASE-T/TX integrated switch targeted at cost-sensitive Fast Ethernet managed switch systems. The device contains five full-duplex 10BASE-T/100BASE-TX Fast Ethernet transceivers, each of which performs all of the physical layer interface functions for 10BASE-T Ethernet on CAT 3, 4, or 5 unshielded twisted-pair (UTP) cable and 100BASE-TX Fast Ethernet on CAT 5 UTP cable. 100BASE-EFX is supported through the use of external fiber optic transceivers.

The BCM5325E device provides a very highly integrated solution. It combines all of the functions of a high-speed switch system, including packet buffer, transceivers, media access controllers (MACs), address management and a non-blocking switch controller, into a single monolithic 0.18-µm CMOS device. It complies with the IEEE 802.3, 802.3u, and 802.3x specifications, including the MAC control Pause frame and auto-negotiation subsections, providing compatibility with all industry-standard Ethernet and Fast Ethernet devices. This function requires only a small low-cost microcontroller to initialize and configure the device.

FEATURES

- Six-port, 10/100 Mbps integrated switch controller—fully non-blocking configuration
- Five integrated 10/100BASE-T/TX/EFX IEEE 802.3u compliant transceivers.
- Integrated full-duplex capable IEEE 802.3x-compliant MACs
- 64 KB on-chip packet buffer
- Media Independent Interface (MII) provided for an additional TX/FX uplink to PHY or MAC.
- Integrated address management—supports up to 1K unicast addresses
- Port mirroring and Layer-3 IGMP snooping
- IEEE 802.1p QoS packet classification with four priority queues and DiffServ DSCP priorities in IPv4 and IPv6
- 16 entries IEEE 802.1q-based and Port-based VLAN
- Supports IEEE 802.1x EAPOL higher layer protocol
- EEPROM (93C46) allows further un-managed capabilities
- 25-MHz crystal or oscillator
- Low-power 3.3/1.8V, 0.18 µm CMOS technology
- HP auto-MDIX function hardware selectable
- 128-pin MQFP package.
- Ingress/egress rate control
- Pin compatible with BCM5325
- Protected port capability
- DTE/DPM power over Ethernet detection

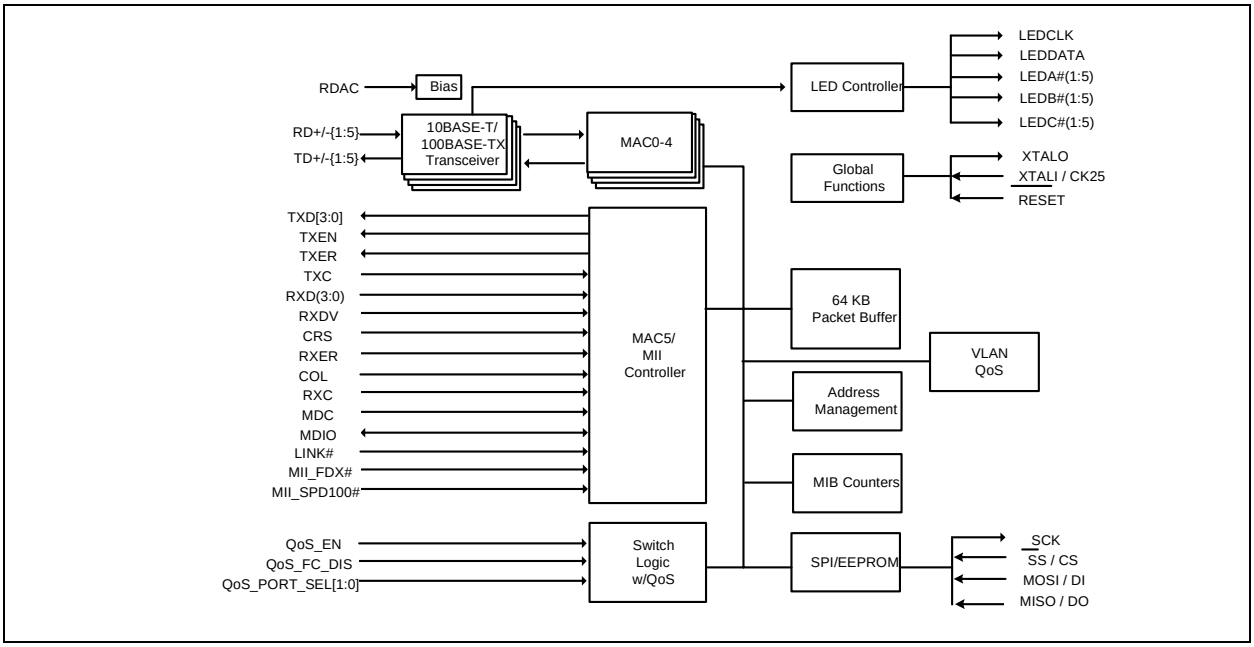

Figure 1: Functional Block Diagram

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REVISION HISTORY

Revision	*Date*	*Description*
5325E-DS14-R	09/16/08	**Updated:** • "FEATURES" • "Rate Control Register" on page 147.
5325E-DS13-R	04/22/08	**Removed** • Figure 33, "VDDBIAS Circuitry," on page 82.
5325E-DS12-R	06/01/07	**Added:** • "100BASE-Enhanced FX" on page 23 • Vidiff (for full threshold and half threshold) and Vicm to Table 171, "Recommended Operating Conditions," on page 177. • TDV cm and VO symbols to Table 172, "Electrical Characteristics," on page 178.
5325E-DS11-R	03/06/07	**Updated:** • Figure 9, "Normal MII Configuration," on page 48. • Figure 10, "Reversed MII Configuration," on page 49. • Table 172, "Electrical Characteristics," on page 177. • Table 173, "128-MQFP Thermal Characteristics—Without Heat Sink (2-Layer PCB)," on page 178 **Added:** • Table 174, "128-MQFP Thermal Characteristics—Without Heat Sink (4-Layer PCB)," on page 178. • Table 175, "128-MQFP Thermal Characteristics—With Heat Sink," on page 178.
5325E-DS10-R	12/22/06	**Updated:** • Table 29, "Pseudo PHY MII Register Definitions," on page 63.
5325E-DS09-R	11/02/06	**Updated:** • Table 41 on page 88. **Added:** • "LED Flash Control Register" on page 95. • "LEDa Control Register" on page 95. • "LEDb Control Register" on page 96. • "LEDc Control Register" on page 96.
5325E-DS08-R	07/18/06	**Updated:** • TXD[0] should be pulled down during power-up ("MII1_TXD[0]" on page 81). • TXD[1] should be pulled down during power-up ("MII1_TXD[1]" on page 81). • DNC list of signal description includes pin 43 ("DNC" on page 83). • "Ingress Mirror Divider Register" on page 106. • "Egress Mirror Divider Register" on page 108.
5325E-DS07-R	04/19/06	**Updated:** • "MIB Engine" on page 45. • Table 142, "IEEE 802.1Q VLAN Registers (Page 0x34)," on page 154. • Table 143, "IEEE 802.1Q VLAN Control 0 Register (Page: 0x34, Address 0x00)," on page 155. • Table 152, "Default IEEE 802.1Q Tag Register Address Summary," on page 162. • Table 166, "Reverse MII Mode Output Timings," on page 173. • Table 172, "Electrical Characteristics," on page 178.

Revision	*Date*	*Description*
5325E-DS06-R	10/04/05	**Updated:** • DNC in Table 35, “Signal Description,” on page 67. • Pin Assignment by Pin Number,” on page 73. • Table 37, “Pin Assignment by Signal Name,” on page 76. • Ingress_VID_check in Table 140, “802.1Q VLAN Control 4 Register (Page: 0x34, Address 0x04),” on page 143 and drop_Vtable_miss in Table 141, “802.1Q VLAN Control 5 Register (Page: 0x34, Address 0x05),” on page 144. • Note below Section 11 Ordering Information. **Added:** • TXD[0] and TXD[1] to Table 35, “Signal Description,” on page 67.
5325E-DS05-R	08/02/05	**Updated:** • “MIB Counters Per Port” on page 43.Figure 9,”Normal MII Configuration,” on page 46. Figure 10, “Reversed MII Configuration,” on page 47. • “Ordering Information” on page 164.
5325E-DS04-R	04/01/05	Minor edits

Revision	*Date*	*Description*
5325E-DS02-R	09/17/04	**Updated:** • "Features" • "Overview" • "802.1Q VLAN" • "Bridge Management" • "Spanning Tree Port State" • "Disable" • "Blocking" • "Listening" • "Management Frames" • "Independent Management Port" • "OPCODE Field in BRCM Tag for Management Port Frame" table • "MII Port" • "Programming Interfaces" • Moved "Register Access through Pseudo PHY Interface" after "EEPROM Interface" • "Switch Mode Register" • "Mirror Capture Control Register (Page 0x02: Address 0x10–0x11)" table • "Multiport Vector 1 Register (Page 0x04: Address 0x16–0x17)" table • "Multiport Vector 2 Register (Page 0x04: Address 0x26–0x27)" table • "Secure Source Port Mask (Page 0x04: Addresses 0x30–0x31)" table • "Behavior for Reserved Multicast Addresses" table. • "MII Management (MDC/MDIO)" • "Signal Description" table • "Control Registers (Page 0x00)" table • "Secure Destination Port Mask (Page 0x04: Addresses 0x32–0x33) "table • "PHY Port Status Register (Pages 0x10–0x14, 0x19, Address 0x02–0x03)" table • "PHY Identifier Registers (Pages 0x10–0x14, 0x19, Address 0x04–0x07)" table **Added:** - "Cable Analyzer" - "Revision ID Register (Page 0x02: Address 0x02)" - "Queue 0 TXDSC Control 3 Register" - "Queue 1 TXDSC Control 3 Register" - "Queue 2 TXDSC Control 3 Register" - "Queue 3 TXDSC Control 3 Register" **Removed:** • "Serial Management" • "SMP Control Register"
5325E-DS01-R	04/13/04	**Updated:** • "Switch Mode Register (Page 0x00: Address 0x0B)" table • "MII1 Port State Override Register (Page 0x00: Address 0x0E)" table • "Secure Destination Port Mask" • "Page 0x31 VLAN Registers" table • "Port VLAN Control Register Serial, MII, Ports[0:4] (Page 31h, Address 00d–09d, 16d–19d, 00h–09h, 10h–13h)" table
5325E-DS00-R	03/22/04	Initial release

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Section 1: Introduction

OVERVIEW

The BCM5325E is a single-chip, six-port 10BASE-T/100BASE-TX switch device. This device integrates:

- Five 10BASE-T/100BASE-TX transceivers.
- One general use 10/100 MII interface.
- Six full-duplex capable media access controllers (MACs).
- High-performance integrated packet buffer memory.
- An address resolution engine.
- A non-blocking switch controller.
- A set of management information base (MIB) statistics registers.

The integrated 10BASE-T/100BASE-TX transceivers perform all the physical layer interface functions for 100BASE-TX full-duplex or half-duplex Ethernet on CAT-5 twisted pair cable and 10BASE-T full-duplex or half-duplex Ethernet on CAT-3, -4, or -5 cable.

The transceiver performs 4B5B, MLT3, NRZI, and Manchester encoding and decoding, clock and data recovery, stream cipher scrambling/descrambling, digital adaptive equalization, line transmission, carrier sense and link integrity monitor, auto-negotiation and MII management functions. Each of the five integrated transceiver ports of the BCM5325E connects directly to the network media through isolation transformers. The integrated transceiver is fully compliant with the IEEE 802.3 and IEEE 802.3u standards.

The device provides six internal media access controllers. Each MAC is dual-speed and both half- and full-duplex capable. Flow control is provided in the half-duplex mode with backpressure. In full-duplex mode, IEEE 802.3x frame-based flow control is provided. The MAC is IEEE 802.3-compliant and supports a maximum frame size of 1536 bytes.

An integrated address management engine provides address learning and recognition functions at maximum frame rates. The address table provides capacity for up to 1K unicast addresses. Addresses are added to the table after receiving an error-free packet. Broadcast and multicast frames are forwarded to all ports except the port where it was received.

AUDIENCE

This document is for designers interested in integrating the BCM5325E RoboSwitch™ into their hardware designs, and others who need specific data about the physical characteristics and operation of the BCM5325E RoboSwitch.

DATA SHEET INFORMATION

The following notational conventions are used in this document:

- Signal names are shown in UPPERCASE letters.
  Example: DATA
- A bar over a signal name indicates that it is active low.
  Example: CE
- In register and signal descriptions, [n:m] indicates a range from bit n to bit m.
  Example: [7:0] indicates bits 7 through 0, inclusive.
- The use of R or RESERVED indicates that a bit or field is reserved by Broadcom for future use. Typically, R is used for individual bits and RESERVED is used for fields.
- Numerical modifiers such as K or M follow traditional usage.
  Example: 1 KB means 1,024 bytes, 100 Mbps (referring to Fast Ethernet speed) means 100,000,000 bits per second, and 133 MHz means 133,000,000 Hertz.
- The lowercase letter b denotes bit and uppercase letter B denotes bytes (8-bits).
- The hexidecimal number is represented by 0x(hex number) or yyh.

Where it seems helpful, cross-reference links have been incorporated in the data sheet. The cross-reference is denoted in blue text. When using a PDF version of data sheet, users can jump to another related section of the data sheet by clicking on this blue text using the PDF hand tool.

As always, every effort is made to improve the data sheet and other documentation. To submit suggestions, send e-mail to RoboDocs@broadcom.com. For technical questions, contact your local sales representative.

Section 2: Features and Operation

OVERVIEW

The BCM5325E includes the following features:

QOS

The QoS (Quality of Service) feature provides up to four internal queues per port to support four different traffic priorities. These priorities can be programmed such that high-priority traffic experiences less delay in the switch under congested conditions than that of lower priority traffic. This can be important in minimizing latency for delay sensitive traffic. The BCM5325E can assign the packet to one of the four egress transmit queues according to Port-Based QoS (Ingress Port ID), "IEEE 802.1P QoS" on page 4, "MAC-Based QoS" on page 4, or "Diff-Serv QoS" on page 4 information. The "Frame Priority Decision Tree" on page 5 decides which priority system is used based on four programmable register bits. This priority is then assigned to one of the four priority queues on a port-by-port basis.

The QoS mechanism operates at full wirespeed. Flow control measures can be enabled when QoS is active by programming the Table 133 on page 133.

SOFTWARE CONTROL

Writing to the QOS_Enable bit in the "QoS Control Register" on page 131 enables software control of the QoS mechanisms as described in the following sections.

EGRESS TRANSMIT QUEUES

Each Egress port supports up to four queues as programmed by the TXQ_MODE bits in the "QoS Control Register" on page 131. Each incoming frame is assigned to an egress transmit queue depending on its assigned priority. Each egress transmit queue is a list specifying an order for packet transmission. The corresponding egress port transmits packets from each of the queues according to a programmable algorithm, with the higher priority queues being given greater access than the lower priority queues, with Queue 0 being the lowest priority queue.

PORT-BASED QOS

Port-based QoS can be activate activated by programming the Port-Based QOS bits in the Table 129 on page 131. If Port-Based QoS is enabled, the traffic coming in on that ingress port is always allocated to the highest transmit queue. The Port-based priority is assigned to a frame based on the results of "Frame Priority Decision Tree" on page 5. If Port-Based QoS is disabled, the traffic coming in on that ingress port is always allocated to the lowest transmit queue.

DIFF-SERV QOS

Diff-Serv QoS is enabled on a port by port basis by setting the DIFF-SERV_EN bit in Table 132 on page 132. When using Diff-Serv priority mechanism, the packet is classified based on the DSCP field in the IP header (in both IPv4, and IPv6 format). If the tag is present, the packet is assigned a remapped Diff-Serv priority based on the Diff-Serv Mapping registers on "QoS Diff-Serv Enable Register" on page 132. The Diff-Serv priority is assigned to the frame depending on the result of the "Frame Priority Decision Tree" on page 5. Each Diff-Serv priority is mapped to one of the egress transmit queues based on the "DiffServ DSCP Priority Register" on page 134.

IEEE 802.1P QOS

IEEE 802.1P QoS is enabled on a port by port basis via the QOS_1P_EN bit in the "QoS IEEE 802.1P Enable Register" on page 132. When using the IEEE 802.1P priority mechanism, the packet is examined for the presence of a valid IEEE 802.1P Priority Tag. If the tag is present, the priority is assigned to a valid transmit queue via the "IEEE 802.1P Priority Threshold Register" on page 133. The IEEE 802.1 QoS is assigned to the frame based on the results of "Frame Priority Decision Tree" on page 5.

MAC-BASED QOS

When using MAC-Based QoS, the destination address and VLAN ID is used to index the ARL table as described in "Address Management" on page 23. The matching ARL entry contains a two bit PRI field as shown in Table 17 on page 25. These bits set the MAC-Based Priority for the frame to the corresponding transmit queue. The MAC-Based priority is assigned to the frame depending on the result of the "Frame Priority Decision Tree" on page 5. The PRI bits for a learned ARL entry default to priority 0. To change the default, an ARL entry is written to the ARL table as described in the "Writing an ARL Entry" on page 28.

FRAME PRIORITY DECISION TREE

The Frame Priority Decisions Tree determines which of the priority systems is used to the frame priority. As summarized above, the frame priority can be determined according to the Ingress Port-Based Priority, IEEE 802.1P Priority, MAC-Based Priority, or Diff-Serv Priority information. The Diff-Serv and IEEE 802.1P QoS priorities are available only if the respective QoS is enabled, and the received packet has the appropriate tagging. The QoS order is: Port-based --> Diffserv --> IEEE 802.1p --> MAC-based.

The frame priority decision tree is:

```
If (Port-Based QOS bits in the Table 129 on page 131 is set)
   Transmit Queue follow port based priority rule.
else if (DIFF-SERV_EN is enabled per port and received tagged L3 packet)
   Transmit Queue assigned priority based on the DiffServ rule.
else if (QOS_1P_EN is enabled per port and received tagged packet)
   Transmit Queue assigned the priority by IEEE 802.1p rule.
else Transmit Queue corresponding to MAC-based priority rule.
```

Writing the QOS_Layer_Sel bits in the "QoS Priority Queue Control Register" on page 131 to 0 alters the Frame Decision Tree above by reversing the Diff-Serv and IEEE 802.1P.

PORT-BASED VLAN

The Port-Based VLAN (Virtual LAN) feature partitions the switching ports into virtual private domains designated on a per port basis. Data switching outside of the port's private domain is not allowed. The BCM5325E provides flexible VLAN configuration for each ingress (receiving) port.

The Port-Based VLAN feature works as a filter, filtering out traffic destined to non-private domain ports. The private domain ports are selected for each ingress port via the "Port-Based VLAN Control Register" on page 135. For each received packet, the ARL resolves the DA and obtains a forwarding vector, a list of ports to which the frame shall be forwarded. The ARL then applies the VLAN filter to the forwarding vector, effectively masking out the non-private domain ports. The frame is forwarded only to those that meet the ARL table criteria, as well as the Port-Based VLAN criteria.

IEEE 802.1Q VLAN

The BCM5325E supports IEEE 802.1Q VLAN and up to 16 VLAN Table entries that reside in the internal embedded memory. Once the VLAN table is programmed and maintained by the microcontroller or CPU, the BCM5325E autonomously handles all operations of the protocol. These actions include the stripping or adding of the IEEE 802.1Q tags depending on the requirements of the individual transmitting port. It also performs all the necessary VLAN lookups in addition to MAC L2 lookups. If the MII port is designated as the management port, the CPU is responsible for tagging and untagging all packets received and transmitted from/to the switch.

IEEE 802.1Q VLAN Table Organization

Each VLAN Table Entry, also referred to as a VID or VLAN ID, consists of a Valid Bit, High Order VLAN bits, Untag Map, and Forward Map.

- Valid Bit designates whether the VID is valid.
- High Order VLAN bits consist of bits[11:4] of the 2-byte Tag Control Information field of the IEEE 802.1Q frame. See High Order 8-Bit VLAN ID below for more information.
- Untag Map controls whether the egress packet is tagged or if the tag should be removed for egress to provide backward support for non-IEEE 802.1Q networks.
- Forward Map defines the membership within a VLAN domain.

The Untag Map and Forward Map include bit-wise representation of all the ports.

Each entry of the VLAN table is indexed by the lower order 4-bits of the VLAN ID. For this reason, the VLAN table is not able to simultaneously accommodate entries for two VLAN IDs with the same lower order 4-bits. The second VLAN entry would overwrite the first.

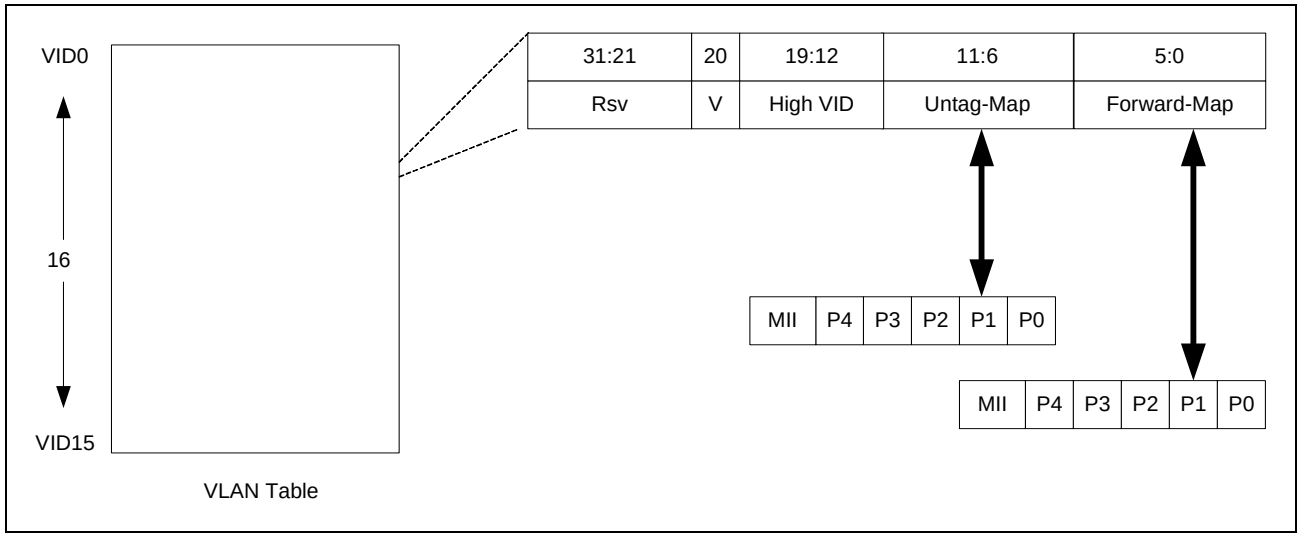


Figure 2: IEEE 802.1Q VLAN Untag Table

PROGRAMMING THE VLAN TABLE

The IEEE 802.1Q VLAN feature can be enabled by writing to the EN_1QVLAN bit in the "IEEE 802.1Q VLAN Control 0 Register" on page 137. The default priority and VID can be assigned to each port in the "IEEE 802.1Q Default Port TAG Register" on page 144. These are necessary when tagging a previously untagged frame.

The VLAN Table can be written using the following steps:

- Use the "IEEE 802.1Q VLAN Write Register" on page 142 to define which ports are part of the VLAN group and which ports should be untagged. The Valid bit should be set to 1.
- Use the "IEEE 802.1Q VLAN Table Access Register" on page 142 to define the High Order VLAN ID bits of the VLAN group.
- Use the "IEEE 802.1Q VLAN Table Access Register" on page 142 to define the Low Order VLAN ID bits of the VLAN group. These bits access the VLAN table entry.
- Set bit 12 of the "IEEE 802.1Q VLAN Table Access Register" on page 142 to 1, indicating a write operation.
- Set bit 13 of the "IEEE 802.1Q VLAN Table Access Register" on page 142 to 1, starting the write operation. This bit returns to 0 when the write is complete.

The VLAN Table can be read using the following steps:

- Use the "IEEE 802.1Q VLAN Table Access Register" on page 142 to define from which VLAN group (Low Order bits) to read the data.
- Set bit 12 of the "IEEE 802.1Q VLAN Table Access Register" on page 142 to 0, indicating a read operation.
- Set bit 13 of the "IEEE 802.1Q VLAN Table Access Register" on page 142 to 1, starting the read operation. This bit returns to 0 when the read is complete.
- Read the "IEEE 802.1Q VLAN Read Register" on page 143 to obtain the VLAN table entry information.

HIGH ORDER 8-BIT VLAN ID

When a packet is received with an IEEE 802.1Q tag, the lower order bits are used to search the VLAN table. If there is a valid entry in the corresponding location, the high order 8-bits are then checked. If 8BIT_CHECK bit of the "IEEE 802.1Q VLAN Control 3 Register" on page 139 is set, the high order 8-bits are checked against the high order 8-bits contained in the VLAN table entry. If this bit is not set, the bits are checked against the high 8-bits contained in the HIGH8_VID bits of the "IEEE 802.1Q VLAN Write Register" on page 142. In this case, the high 8-bits contained in the write register would need to be unchanged after initialization to ensure that the incoming packet's VID is compared to the correct high order bits. To program the VLAN table with entries that do not share common high order 8-bits, the 8BIT_CHECK bit should be set.

RATE CONTROL

Forwarding excessive broadcast traffic, consumes switch resources, which can negatively impact the forwarding of other traffic. The rate control mechanism is used to protect regular traffic from an overabundance of broadcast, multicast, or destination lookup failure (DLF) traffic. This feature monitors the rate of ingressed traffic of programmable packet types. If the rates of these packet types exceed the programmable maximum rate, the packets are dropped. To enable rate control for each of the three packet types, set bits[6:4] of the "Rate Control Register" on page 147.

The broadcast storm mechanism works on a credit-based rate system that figuratively uses a bucket to track the bandwidth of each port (see Figure 3). Credit is continually added to the bucket based on the Rate Percentage values programmed in bits[1:0] of the "Rate Control Register" on page 147. Credit is decremented from the bucket whenever one of the programmable packet types is ingressed at the port. If no packets are ingressed for a considerable length of time, the bucket credit continues to increase up to a programmable maximum bucket size as programmed in the bits[3:2] of the "Rate Control Register" on page 147. If a heavy burst of traffic is suddenly ingressed at the port, the bucket credit becomes drained. When the bucket is emptied, incoming traffic is constrained to the Rate Percentage, the rate at which credit is added to the bucket. At this point, excess broadcast, multicast, and/or DLF packets are dropped.

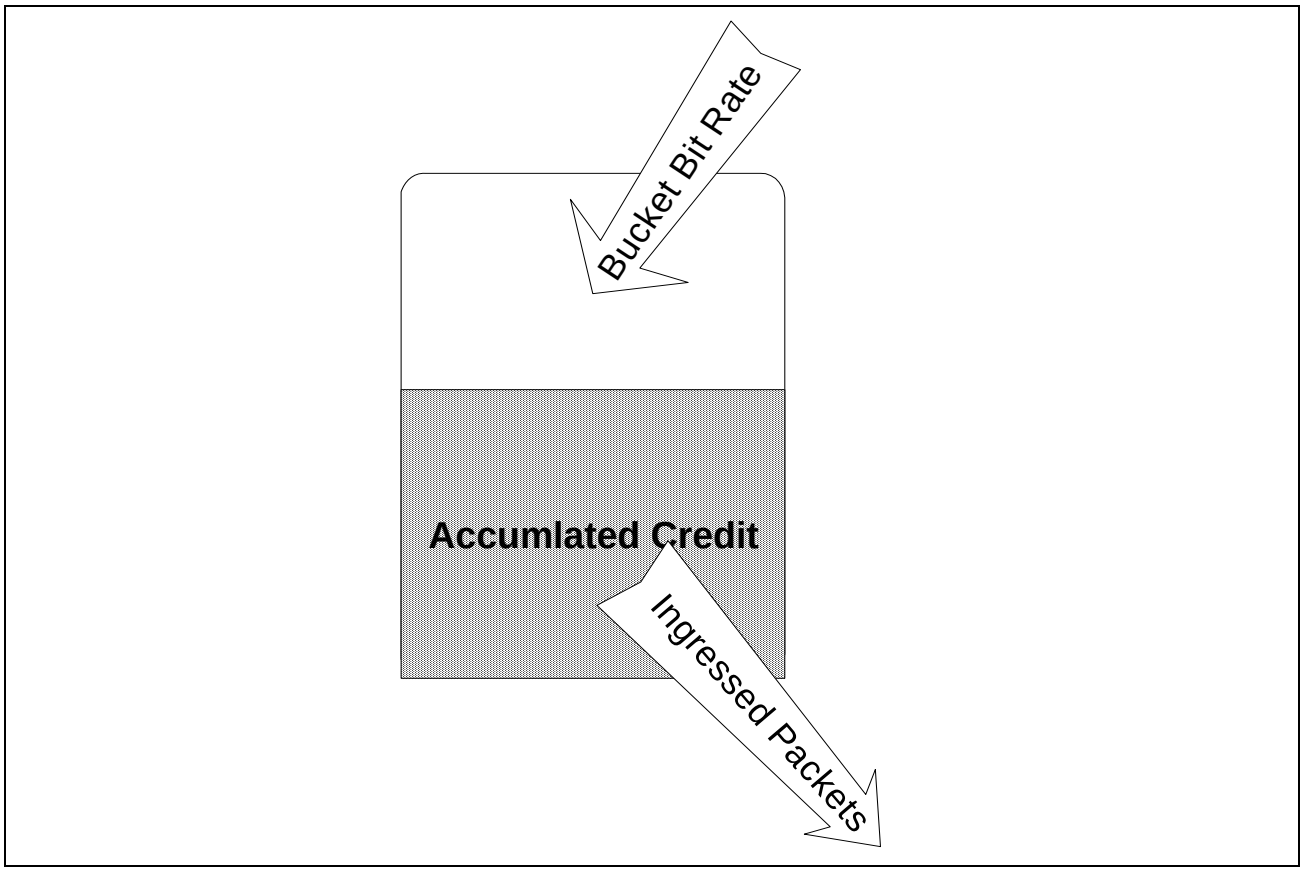


Figure 3: Bucket Flow

PROTECTED PORTS

The Protected Ports feature allows certain ports to be designated as protected. The protected ports are selected via the "Protected Mode Control Register" on page 83. All other ports are non-protected. Traffic between protected port group members is blocked. However, protected ports are able to send traffic to unprotected ports. Unprotected ports can send traffic to any port. There are several applications that can benefit from protected ports.

- Aggregator. All of the available ports are designated as protected ports except a single aggregator port. All traffic incoming to the protected ports are not sent within the protected ports group. Any flooded traffic is forwarded only to the aggregator port.
- To prevent non-secured ports from monitoring important information on a server port, the server port and non-secured ports are designated as protected. The non-secured ports are not able to receive traffic from the server port.

PORT MIRRORING

The BCM5325E supports port mirroring, allowing ingress and/or egress traffic to be monitored by a single port defined as the mirror capture port. The BCM5325E can be configured to mirror the ingress traffic and/or egress traffic of any other port(s). Mirroring multiple ports is possible but can create congestion at the mirror capture port. Several filters are used to decrease congestion.

ENABLING PORT MIRRORING

Port mirroring is configured using a set of registers located in "Page 0x02: Management/Mirroring Registers" on page 88. Port Mirroring is enabled by setting the MIRROR_ENABLE bit in the "Mirror Capture Control Register" on page 90.

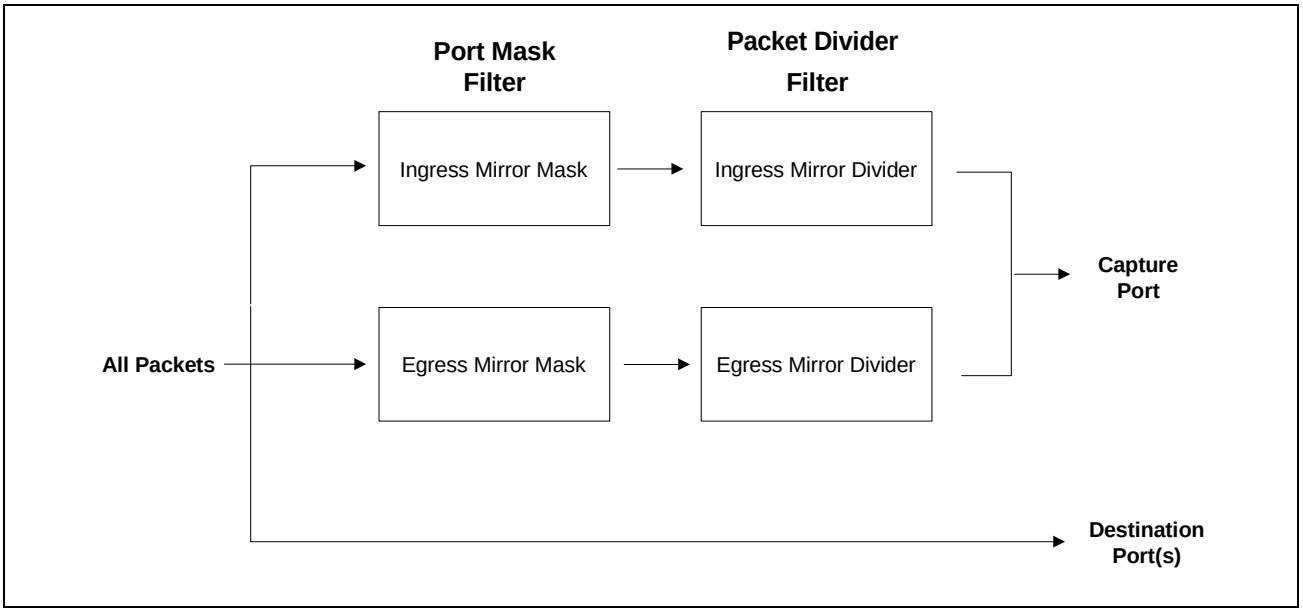


Figure 4: Mirror Filter Flow

CAPTURE PORT

The Capture Port is capable of monitoring other specified ports. Frames transmitted and received at the other ports are forwarded to the Capture Port according to the Mirror Rules below. The capture port is specified by the CAPTURE_PORT bits of the "Mirror Capture Control Register" on page 90.

MIRROR FILTERING RULES

Mirror Filtering Rules consist of a set of two filter operations, "Port Mask Filter" on page 10 and "Packet Divider Filter" on page 10, that are applied to traffic ingressed and/or egressed at a switch port. They are programmed via the following registers:

- Ingress Mirror Rules are programed using two registers: the "Ingress Mirror Control Register" on page 91 and "Ingress Mirror Divider Register" on page 91.
- Egress Mirror Rules are programed using two similar registers: the "Egress Mirror Control Register" on page 92, and the "Egress Mirror Divider Register" on page 92.

These registers work similarly, but one sets controls for the mirroring of frames based on which port the frame was received (ingressed), and the other sets controls for the mirroring of frames based on which port the frame was transmitted (egressed).

Port Mask Filter

The IN_MIRROR_MASK bits in the "Ingress Mirror Control Register" on page 91 define the receive ports that are monitored. The OUT_MIRROR_MASK bits in the "Egress Mirror Control Register" on page 92 define the transmit ports that are monitored.

Any number of ingress/egress ports can be programmed to be mirrored, but bandwidth restrictions on the one mirror capture port should be taken under advisement, so as not to cause congestion or packet loss.

Packet Divider Filter

The IN_DIV_EN bit in the Table 65 on page 91 allows further statistical sampling to be performed. When IN_DIV_EN = 1, the receive frames passing the initial filter are divided by the value IN_MIRROR_DIV, which is a 10-bit value stored in the "Ingress Mirror Divider Register" on page 91. Only one out of every n frames is forwarded to the mirror capture port, where n is the number specified in the IN_MIRROR_DIV bits. Similarly, the Egress Mirror Divide function is controlled by the "Egress Mirror Control Register" on page 92 and the "Egress Mirror Divider Register" on page 92.

IGMP SNOOPING

IGMP is a commonly used protocol to transmit video and multimedia streams over IP. When the Enable IGMP IP layer Snooping bit is set in the "Global Management Configuration Register" on page 89 the BCM5325E looks in the protocol field of the IP header of each frame and forwards IGMP control packets to the Management Port as defined in the "Global Management Configuration Register" on page 89. The Management CPU can then determine from the information contained within the IGMP control packets which port should participate in the multiport group session. In turn, the CPU affects this by programming either the ARL table or the applicable ports in the Multiport Addresses as described in "Using the Multiport Addresses" on page 29.

WAN PORT

If a port is designated as a WAN port, all received traffic is forwarded only to the CPU port. Additionally, all local traffic won't flood the WAN port. The WAN port is selected by setting bits[4:0] of the "WAN Port Select Register" on page 83.

To avoid Multicast, Broadcast, and/or Destination Lookup Failure (DLF) packets received at the Management Port from flooding to the WAN port, set Bit 5 of the "WAN Port Select Register" on page 83. When set, only egress-directed frames from the Management port can be forwarded to the WAN port.

IEEE 802.1X PORT-BASED SECURITY

IEEE 802.1X is a port-based authentication protocol. By receiving and extracting special frames, the CPU can control whether the ingress and egress ports should forward packets. If a user port (supplicant) wants to get service from another port (authenticator), it must get approved by the authenticator. EAPOL is the protocol used by the authentication process.

After reset, if IEEE 802.1x is enabled on a port-based basis via the "IEEE 802.1X Control 2 Register" on page 110. Initially, all traffic at the designated ports are blocked. Setting the bit in the "IEEE 802.1X Control 1 Register" on page 110 allows BPDU and EAPOL frames to be forwarded. The BCM5325E detects BPDU and EAPOL frames and pass them to the CPU port. After the authentication process is finished, the CPU is responsible to set the "IEEE 802.1X Control 2 Register" on page 110 of any authenticated ports to 0 to permit normal traffic.

DTE/DPM POWER OVER ETHERNET DETECTION

The BCM5325E provides support for identifying DTE capable of accepting power via MDI. Such a DTE is typically connected to a switch capable of detecting its presence and able to establish signaling with it. The process of identifying DTE Power via MDI capable is termed DPM.

When the BCM5325E starts auto-negotiation and DPM detection is enabled, it sends a unique Fast Link Pulse (FLP) word that is different from a normal FLP word. If the Link partner is DPM capable, it returns this unique FLP word. Otherwise, the BCM5325E may receive the Link partner's word instead of the unique FLP word sent. The BCM5325E updates a register containing relevant status bits that the MAC can read. The BCM5325E continues to send the unique FLP word if no response is received from the Link partner. At any time, the MAC can disable DPM detection and restart auto-negotiation to establish normal link with the Link partner.

DPM DETECTION DESCRIPTION

A shadow register containing required enable and status bits for DPM support is present in the BCM5325E. The BCM5325E defaults to Normal mode and Non-DPM Detection mode upon power-up, as per the IEEE 802.3u standard. The shadow register is accessed after setting bit 7 of the DPM register (pages 0x10–0x14, address 0x3E–0x3F) (see Table 2 on page 13) to 1.

Figure 5 on page 12 shows the sequence for DPM detection procedure combined with auto-negotiation. Table 2 on page 13, and Table 3 on page 15 show DPM register and interrupt register bits and their description. The MAC can enable DPM detection by setting the DPMDETEN bit to 1, and restart auto-negotiation by setting ANRSTRT bit to 1. When enabled, the BCM5325E loads an internally generated unique word into the Auto-negotiation Advertisement register and sends it out. While this word is transmitted, the link pulse width can be increased from 150 ns to 950 ns, in 50-ns increments per FLPWIDTH register if LPXTND bit is set to 1. If LPXTND bit is a 0, then a default link pulse width of 100 ns is used.

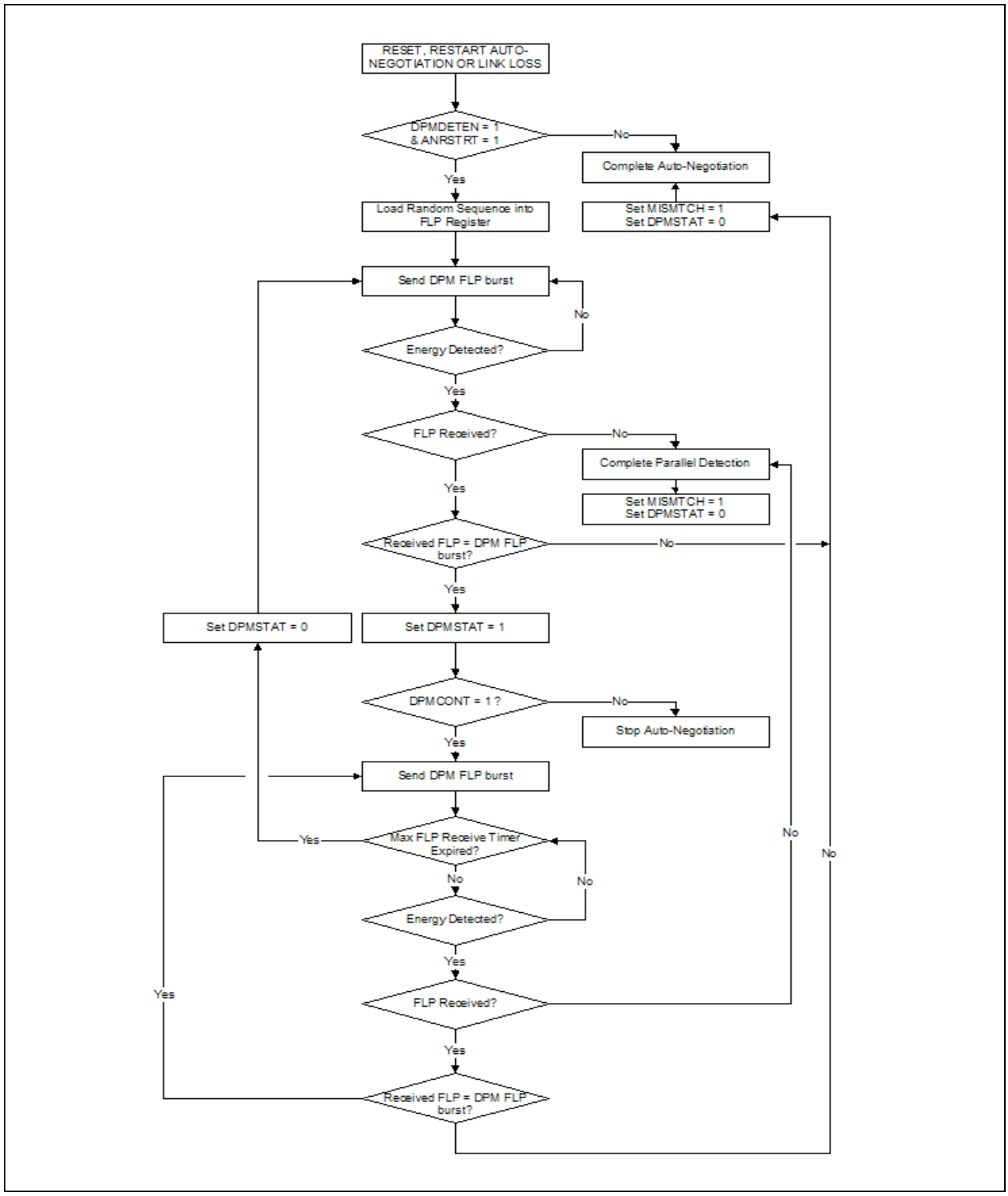


Figure 5: DPM Detection and Auto-Negotiation Flow Diagram

DPM DETECTION

In DPMDETEN mode, the BCM5325E continues to send out an internally generated unique FLP word of DPM FLP burst, until it detects energy from the Link partner. When it detects energy, the BCM5325E takes the following actions:

- If no FLP is received, then the BCM5325E starts and completes parallel detection, sets MISMTCH bit to 1, and enters link phase as per the parallel detection.
- If the received FLP word does not match the DPM FLP burst, then the BCM5325E sets the MISMTCH bit to 1, completes auto-negotiation, and enters the link phase.
- If the received FLP word matches the DPM FLP burst, then the BCM5325E sets the DPMSTAT bit to 1 and takes the following action depending on if the DPMCONT bit is a:
  - 0, then the BCM5325E stops auto-negotiation and waits for MAC before taking further action.
  - 1, then the BCM5325E sends a DPM FLP burst and monitors the state of receive FLP timer and energy from the Link partner. If:
    - Receive FLP timer has expired, then it sets the DPMSTAT bit to 0 and starts over the DPM detection.
    - Energy is detected from the Link partner but no FLP is received, then the BCM5325E starts and completes parallel detection, sets the MISMTCH bit to 1, and enters the link phase as per the parallel detection.
    - Energy detected from the Link partner is an FLP word and it matches the DPM FLP burst, then the BCM5325E goes to the previous bullet and continues as stated.
    - Energy detected from the Link partner is an FLP word but it does not match the DPM FLP burst, then the BCM5325E sets the MISMTCH bit to 1, completes auto-negotiation, and enters the link phase.

DPM REGISTER DESCRIPTION

The following table shows the DPM register and its bit definitions, page 0x10–0x14, address 0x1E–0x1F (bit 7 [pages 0x10–0x14, address 0x3E–0x3F] must be set).

Table 1: DPM Register Summary (Pages 0x10–0x14, Address 0x1E–0x1F)

Address	*Name*	*15–11*	*10–7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*	*Default*
0x1E-0x1F	DPM	FLPWIDTH	Reserved	DPMCONT	Reserved	LPXTND	MISMTCH	DPMSTAT	ANRSTR	DPMDETEN	0x0000

Table 2: DPM Register (Page 0x10–0x14, Address 0x1E–0x1F)

Bit	*Name*	*R/W*	*Description*	*Default*
15–11	FLPWIDTH[4:0]	R/W	FLP width increment register.	0
10–7	Reserved	RO	Write as 0, ignore when read.	0
6	DPMCONT: Continuous DPM Detect Enable	R/W	• 0 = Stop after detecting a DPM capable link partner. • 1 = Continue detecting a DPM capable link partner.	0
5	Reserved	RO	Write as 0, ignore when read.	0
4	LPXTND: Extend Link Pulse Width	R/W	• 0 = Normal link pulse width (100 ns). • 1 = Set link pulse width to 150 ns.	0
3	MISMTCH: Word Mismatch	RO	1 = FLP Word mismatch occurred during DPM detection, indicating that the link partner is not a DPM link partner.	0
2	DPMSTAT: Status	RO	1 = Link partner is DPM capable.	0
1	ANRSTRT: Restart	R/W	1 = Restart auto-negotiation (identical to register 0 bit 9) bit used for DPM detection.	0
0	DPMDETEN: DPM Enable	R/W	1 = Enable DPM detection mode.	0

FLPWIDTH[4:0]: FLP Width in DPMDETEN Mode

When the BCM5325E is in DPMDETEN mode and LPXTND is set to 1, then the FLP pulse width can be changed from a default 100 ns to 150 ns. The width can be further increased to a maximum of 950 ns in 50-ns increments as specified by the FLPWIDTH[4:0]. Although the FLP width can be theoretically increased to 150 + 31*50 = 1700 ns, Broadcom does not recommend to increase the FLP width to more than 950 ns due to TX magnetic characteristic.

DPMCONT: Continuous DPM Detect Enable

While in DPMDETEN mode and if this bit is set to 1 after initially detecting a DPM capable Link partner, the BCM5325E continues to monitor the presence of a DPM capable Link partner. If it detects a non-DPM Link partner while in this continuous DPM detection mode, the BCM5325E establishes a link with the Link partner if possible. For details, see Figure 5 on page 12.

LPXTND: Extend Link Pulse Width

When this bit is set to 1, the BCM5325E increases the link pulse width from a normal 100 ns to 150 ns. Additionally, the link pulse width can be increased to a maximum of 950 ns in 50 ns increments per register FLPWIDTH.

MISMTCH: Word Mismatch

When DPM detection is enabled, the Link partner's FLP word is compared to the unique FLP word sent. The MISMTCH bit is set to 1 if the comparison fails indicating that the Link Partner is not DPM capable.

DPMSTAT: DPM Status

When DPM detection is enabled, the Link partner's FLP word is compared to the unique FLP word sent. If it matches, the Link Partner is DPM capable and DPMSTAT bit is set to 1.

ANRSTRT: Restart

This bit, when set to 1, restarts the auto-negotiation. The BCM5325E, after power up, is in a non-DPM detection mode. If DPM detection is needed DPMDETEN bit should be set to 1 and auto-negotiation restarted. Auto-negotiation can also be restarted by setting bit 9 of reg. 0 (Control register) to 1.

DPMDETEN: DPM Detection Enable

When this bit is set to 1, the BCM5325E enables DPM detection when auto-negotiation is restarted. Otherwise, the BCM5325E auto-negotiates in a non-DPM detection mode as per the IEEE 802.3u standard.

DPM INTERRUPTS REGISTER DESCRIPTION

In addition to DPM detection, the BCM5325E is capable of generating interrupts to indicate DPMSTAT bit change if interrupt mode is enabled. The BCM5325E has a maskable interrupt bit in the pages 0x10–0x14, address 0x34–0x35 Bit 12, DPMMASK of pages 0x10–0x14, address 0x34–0x35, which, when set to 1, disables the generation of DPMSTAT change interrupt. Bit 5, DPMINT, of pages 0x10–0x14, address 0x34–0x35 indicates that there has been a change in DPMSTAT bit.

Table 3: Interrupt Register (Pages 0x10–0x14, Address 0x34–0x35)

Address	*Name*	*15–13*	*12*	*11–6*	*5*	*4–0*	*Default*
0x34–0x35	Interrupt	Reserved	DPMMASK	Reserved	DPMINT	Reserved	0x9F0X

DPMINT: DPM Interrupt

Bit 5 of pages 0x10-0x14, address 0x34-0x35, a read only bit, if read as a 1, indicates that there has been a DPMSTAT bit change in the DPM detection process. The change indicated could be from 0 to 1 or from a 1 to 0. Additionally, if the interrupt has been enabled and DPMMASK is a 0, then the BCM5325E generates an interrupt. Reading of register 1Ah clears the DPMINT bit and the interrupt that was caused by DPMSTAT bit change.

DPMMASK: DPM Mask

When the BCM5325E is in DPMDETEN mode, bit 12 of pages 0x14-0x14, address 0x34-0x35, when set to 1, disables any interrupt generated by the DPMSTAT change if interrupt is enabled. However, bit 5, DPMINT, provides DPMSTAT change regardless of DPMMASK bit.

CABLE ANALYZER

The BCM5325E incorporates a robust state machine to analyze the cable plant and diagnose cable problems. When enabled, the BCM5325E can analyze the cable connected to its transceivers through the magnetic modules RJ-45, then reports whether the cable is open or short and also the distance at which it is detecting the open or short.

CABLE ANALYZER REGISTERS AND PROGRAMMING

Cable diagnostics can be initiated at any time by entering certain parameters in the required register bits and then setting the *start* bit. Once the start bit is set, the PHY starts the cable diagnostics and looks for opens, shorts, cable lengths on pair-A and pair-B. When this analysis is completed, it records the results and resets the start bit.

Shadow Register Description

All of the required bits for the cable analyzer are located in the shadow registers, in particular shadow registers (Pages 10-14h, addresses 26h and 28h). Within address 26h, there are eight sub-registers 0x26-0, 0x26-1, 0x26-2, 0x26-3, 0x26-4, 0x26-5, 0x26-6, and 0x26-7.

Shadow register 0x26-n is accessed by writing an index value (n = 000b to 111b) to the shadow register at address 28h. To access shadow register 0x26-1, the index value in shadow register 28h must be set to 1. Also note that whenever an access is made (either a read or a write) to shadow register 26h, the index value in the shadow register 28h is automatically incremented.

When changing a bit within any register, preserve the existing values of reserved bits by performing a ‘read modify’ write.

The following tables show the cable analyzer registers and their contents.

Table 4: Shadow Register 28h (Pages 10h-14h, address 28h)

Address	*15-11*	*10-8*	*7-0*	*Default*
0x28	Reserved	0x26 index	Reserved	0x0000

0x26 index [10:8]. To access shadow register 26h, first an index value from 0(000b) to 7(111b) must be written to these bits. When an access (either read or write) is made to shadow register 26h, this value automatically increments by one (111b after increment becomes 000b).

Table 5: Shadow Register 0x26-0 (Pages 10h-14h, address 26h)

Address	*15-14*	*13-12*	*11-10*	*9-8*	*7-6*	*9-3*	*2*	*1*	*0*	*Default*
0x26-0	Reserved	Pair-B State	Pair-A State	Pass	Error	Reserved	Start	MP	Reserved	0x0000

Pair-B State[13:12]. After the completion of cable analyzer, these bits indicate the status of pair-B of the cable (see Table 6 for details). Pair-B of the cable is the pair that is connected to RD+/- of the device.

Table 6: Pair-B State

Value	*Result for Pair-B*
00b	No fault detected
01b	Pair is open
10b	Pair is short
11b	Reserved

Note: When the cable analyzer function returns a value of 00 (No fault detected), then the attached cable is good. If the device is unable to establish a valid link, the problem is not related to the cable.

Pair-A State[11:10]. After the completion of cable analyzer, these bits indicate the status of pair-A of the cable (see Table 7 for details). Pair-A of the cable is the pair that is connected to TD+/- of the device.

Table 7: Pair-A State

Value	*Result for Pair-A*
00b	No fault detected
01b	Pair is open
10b	Pair is short
11b	Reserved

Note: When the cable analyzer function returns a value of 00 (No fault detected), then the attached cable is good. If the device is unable to establish a valid link, the problem is not related to the cable.

Start [2]. Setting this bit to a 1 starts the cable diagnostics function in the BCM5325. This should be the last bit that is set after programming the required values in shadow registers 0x26-0, 0x26-1, 0x26-2, 0x26-3, 0x26-4, 0x26-5, 0x26-6 and 0x26-7. This bit is cleared when the cable analyzer function is complete. Once this bit is set, it is reset in approximately 5 microseconds.

MP [1] = 1. This is an internal variable required to be set before starting the cable analyzer. Set this bit to a 1.

Pass [9:8]. These bits are 11b when reading the results of the cable analyzer.

Error [7:6]. These bits must be 00b when reading the results of the cable analyzer.

Table 8: Shadow Register 0x26-1 (Pages 10h-14h, address 26h)

Address	*15-8*	*7-0*	*Default*
0x26-1	Pair-B length	Pair-A length	0x0000

Pair-B length [15:8]. These bits indicate the length of pair-B once the cable analyzer is completed. To convert this value to meters, multiply the value by 0.8. This value should be used in combination with the result posted on the condition of pair-B in bits [13:12] of shadow register 0x26-0.

Table 9: Pair-B Cable Diagnostics Result

Pair-B state [13:12] (shadow register 0x26-0)	*Pair-B length [15:8] (shadow register 0x26-1)*
01b	Distance at which an open is detected in pair-B
10b	Distance at which a short is detected in pair-B

Pair-A length [7:0]. These bits indicate the length of pair-A once the cable analyzer is completed. To obtain the value in meters, multiply this value by 0.8. This value should be used in combination with the result posted on the condition of pair-A in bits [11:10] of shadow register 0x26-0.

Table 10: Pair-A Cable Diagnostics Result

Pair-A state [11:10] (shadow register 0x26-0)	*Pair-A length [7:0] (shadow register 0x26-1)*
01b	Distance at which an open is detected in pair-A
10b	Distance at which a short is detected in pair-A

Table 11: Shadow Register 0x26-2 (Pages 10h-14h, address 26h)

Address	*15-14*	*13-12*	*11-10*	*9-6*	*5*	*4-0*	*Default*
0x26-2	GainA	Reserved	TypeA	Reserved	HP	ThresholdA	0x0000

GainA [15:14] = 01b. This is an internal variable required to be set before starting the cable analyzer. Set these bits to 01b.

TypeA [11:10] = 10b. This is an internal variable required to be set before starting the cable analyzer. Set these bits to 10b.

HP [5] = 1. This is an internal variable required to be set before starting the cable analyzer. Set these bits to a 1.

ThresholdA [4:0] = 00100b. This is an internal variable required to be set before setting the start bit in shadow register 0x26-0 to start the cable analyzer. Set these bits to 00100b.

Table 12: Shadow Register 0x26-3 (Pages 10h-14h, address 26h)

Address	*15-8*	*7-0*	*Default*
0x26-3	SourceA	Reserved	0x0000

SourceA [13:8] = 00100000b. This is an internal variable required to be set before setting the start bit in shadow register 0x26-0 to start the cable analyzer. Set these bits to 00100000b.

Table 13: Shadow Register 0x26-4 S (Pages 10h-14h, address 26h)

Address	*15-11*	*10*	*9*	*8-6*	*5-0*	*Default*
0x26-4	Reserved	TypeB	Reserved	TPG	Reserved	0x0000

TypeB [10]. This is an internal variable required to be set before starting the cable analyzer. Set this bit to a 1.

TPG [8:6]. This is an internal variable required to be set before starting the cable analyzer. Set this bit to 100b.

Table 14: Shadow Register 0x26-5 (Pages 10h-14h, address 26h)

Address	*15-14*	*13-5*	*4-2*	*1-0*	*Default*
0x26-5	GainB	Reserved	ThresholdB	Reserved	0x0400

GainB [15:14 = 11b]. This is an internal variable required to be set before starting the cable analyzer. Set these bits to 11b.

ThresholdB [4:2] = 001b. This is an internal variable required to be set before setting the start bit in shadow register 0x26-0 to start the cable analyzer. Set these bits to 001b.

Table 15: Shadow Register 0x26-6 (Pages 10h-14h, address 26h)

Address	*15-14*	*13-8*	*7-0*	*Default*
0x26-6	Reserved	SourceB	Reserved	0x0000

SourceB [13:8] = 000001b. This is an internal variable required to be set before setting the start bit in shadow register 0x26-0 to start the cable analyzer. Set these bits to 000001b.

Table 16: Shadow Register 0x26-7 (Pages 10h-14h, address 26h)

Address	*15-9*	*8-6*	*5*	*4-0*	*Default*
0x26-7	Reserved	PGWB	Reserved	AmpB	0x0000

PGWB [8:6] = 001b. This is an internal variable required to be set before setting the start bit in shadow register 0x26-0 to start the cable analyzer. Set this bit to a 001b

AmpB [4:0] = 01100b. This is an internal variable required to be set before setting the start bit in shadow register 0x26-0 to start the cable analyzer. Set this bit to a 01100b.

PROGRAMMING EXAMPLE

The following example shows a general flow of completing the cable analyzer in the PHY:

Cable Analyzer Programming

Start

Write register ***(Pages 10h-14h, address 3Eh)*** = 0x008B Enable shadow register

Wait

Read ***(Pages 10h-14h, address 28h)***; Wait here for at least 2 seconds of bit 6 for address 28h to be at 0. This ensures that there is no energy from the link partner.
Write ***(Pages 10h-14h, address 28h)*** -0x0000

End Wait

Write register ***(Pages 10h-14h, address 26h)*** = 0x0000
Write register ***(Pages 10h-14h, address 28h)*** = 0x0200 Set access shadow register 26h to 0x26-2
Write ***(Pages 10h-14h, address 26h)*** = 0x4824; 0x26-2
Write ***(Pages 10h-14h, address 26h)*** = 0x4000; 0x26-3
Write ***(Pages 10h-14h, address 26h)*** = 0x0500; 0x26-4
Write ***(Pages 10h-14h, address 26h)*** = 0xC404; 0x26-5
Write ***(Pages 10h-14h, address 26h)*** = 0x0100; 0x26-6
Write ***(Pages 10h-14h, address 26h)*** = 0x004C; 0x26-7
Write ***(Pages 10h-14h, address 26h)*** = 0x8006; 0x26-0 (Start cable diagnostics)

Wait

Write ***(Pages 10h-14h, address 28h)*** = 0x0000; Set access to 0x26-0
Read ***(Pages 10h-14h, 1 address 26h)*** ; Read 0x26-0
If register 0x26-0 bit [2] = 1 then go to **Wait**

Result

Pair-A status = 0x26-0 bit [11:10]
Pair-B status = 0x26-0 bit [13:12]

Read ***(Pages 10h-14h, 19h, address 26h)*** ; Read 0x26-1
Pair-A length = bit [7:0] X 0.8 meters
Pair-B length = bit [15:8] X 0.8 meters

Write register ***(Pages 10h-14h, 1address 3Eh)*** = 0x000B Enable default MII register access

End

Note

1. If a port is connected to a link partner with a good cable (no short or no open on either pair) and the link partner is not powered up, then the cable status bits are valid, but the length bits are invalid.
2. If a port is connected to a link partner, and if either the link is up or the port is detecting energy from the link partner, then the cable diagnostics result is unpredictable.

Cable Analyzer Flow Chart

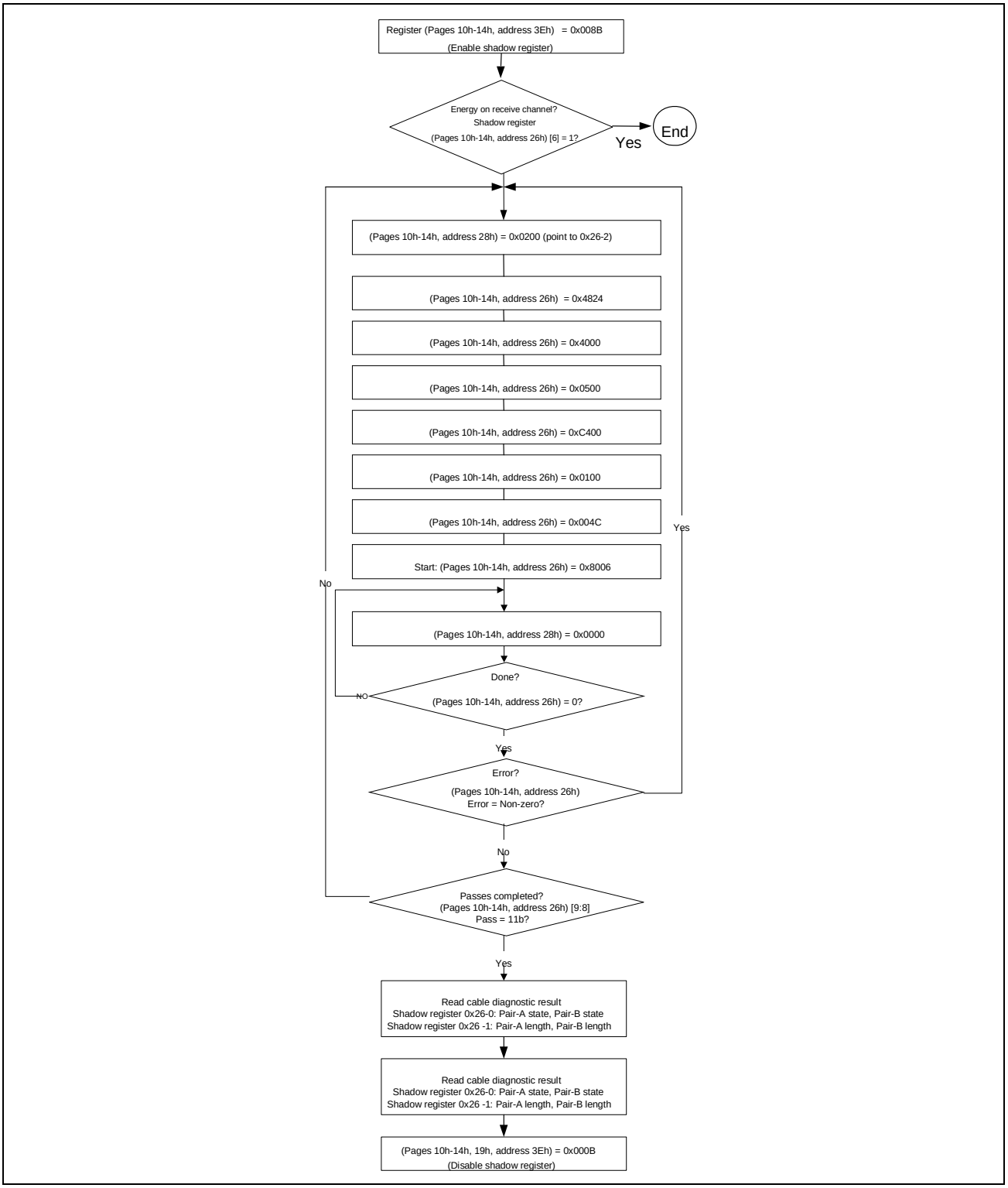


Figure 6: Cable Analyzer Flow Chart

100BASE-ENHANCED FX

BCM5325E offers Enhanced FX (EFX) mode for a cost-reduced version of the 100BASE-FX feature. The EFX feature establishes a link by detecting the input signal amplitude directly rather than relying on the signal detect (SD) signal from an optical module in 100BASE-FX mode. This approach allows designers to disregard signal detect (SD) or loss of signal (LOS) from the 100BASE-FX transceiver module. The signal requirements for the input signals as well as the register settings required for configuring the EFX feature are described below. Notice that the BCM5325E switch offers two threshold modes: Full Threshold mode and Half Threshold mode. In Half Threshold mode, lower amplitude input signals can trigger the link state, however, the noise requirement is tighter. Figure 7 shows an example.

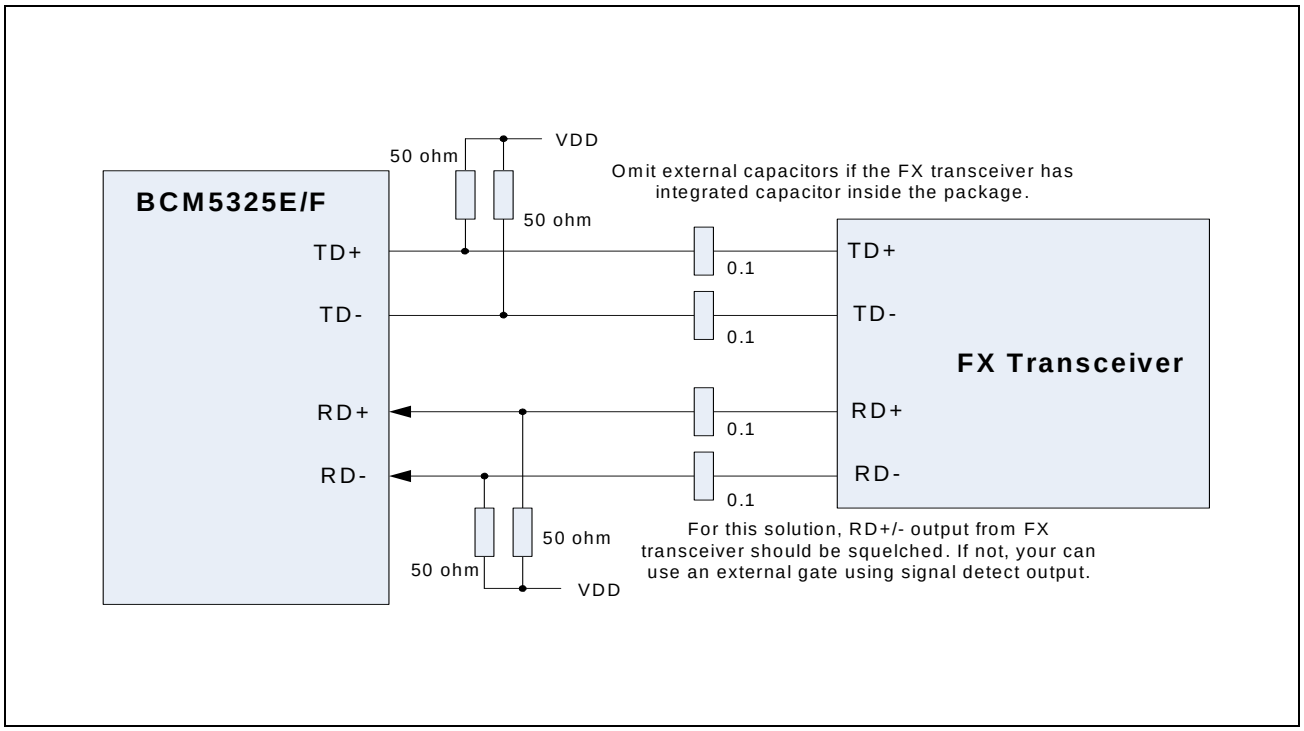


Figure 7: Typical EFX Connection Diagram

The EFX feature can be enabled by setting the following registers in sequence after power-up.

To set the EFX feature in Full Threshold mode:

- PHY register 0x00, write 0x2100 configures the PHY in 100M, full-duplex mode with auto-negotiation disabled (same as SPI register 0x00).
- PHY register 0x10, write 0x0220 bypasses the scrambler/descrambler block. Bit 9 bypasses the scrambler and descrambler blocks. Bit 5 enables the 100 BASE-FX Far-End-Fault function (same as SPI register 0x20).
- PHY register 0x17, write 0x0020 changes the coding from MLT-3 code to two-level binary (same as SPI register 0x2E).
- PHY register 0x1F, write 0x008B enables the shadow register when bit 7 is set (same as SPI register 0x3E).
- PHY register 0x19, write 0x0200 enables the special signal detection block (same as SPI register 0x32).
- PHY register 0x1D, write 0x0084 configures the transmit amplitude to 1v pk-pk (same as SPI register 0x3A).
- PHY register 0x1F, write 0x000B exits the shadow register mode (same as SPI register 0x3E).

To set the EFX feature in Half Threshold mode,

- PHY register 0x1F, write 0x008B enable the shadow register when bit 7 is set (same as SPI register 0x3E).
- PHY register 0x11, write 0x0A01 sets the threshold to the Half Threshold mode (same as SPI register 0x22).
- PHY register 0x1F, write 0x000B exits the shadow register mode (same as SPI register 0x3E).

ADDRESS MANAGEMENT

The BCM5325E Address Resolution Logic contains the following features:

- The two-bin per bucket address table configuration.
- Hashing of the MAC/VID address to generate the address table pointer.

The address management unit of the BCM5325E provides packet rate learning and recognition functions. The address table supports 1K unicast or multicast addresses in the 64 KB on-chip memory. Although the address table shares the packet buffer memory, adequate memory bandwidth is provided for both functions to operate at maximum packet rate.

ADDRESS TABLE ORGANIZATION

The address table is in the bottom of the internal SRAM, occupying the address range from 0x3800 to 0x3FFF. Each bucket contains two entries (or bins). The address table is organized into 512 buckets with two entries in each bucket. This allows up to two MAC addresses with the same index bits to be mapped into the address table.

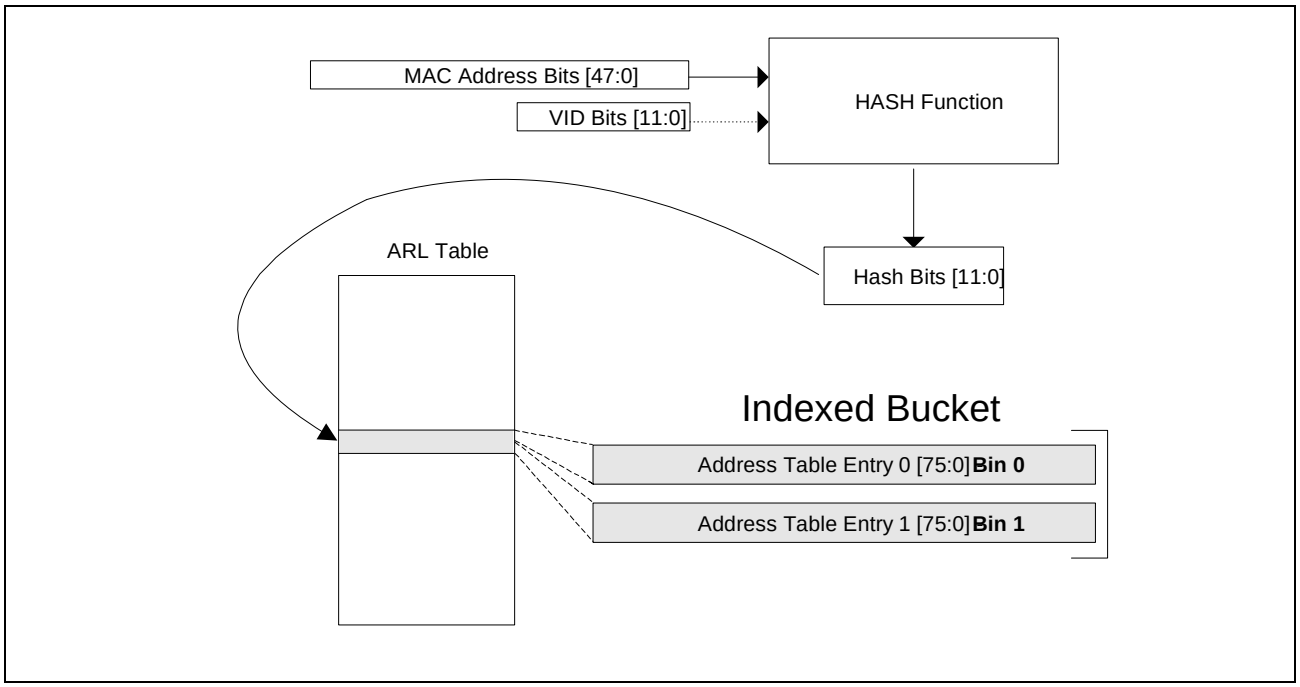


Figure 8: Mode Address Table Organization

The index into the address table is computed from the MAC address using a hash algorithm. If EN_1QVLAN and VLAN Learning Mode bits are set to 1 in the "IEEE 802.1Q VLAN Control 0 Register" on page 137, both the MAC address and the VLAN ID (VID) are used to compute the hashed index. The hash algorithm uses the CRC-CCITT polynomial. The input to the hash is reduced to a 16 bit CRC hash value. Bits 10:0 of the CRC are used index the 1K address table.

The CRC-CCITT polynomial is:

$$x^{16} + x^{12} + x^5 + 1$$

Hashing can be disabled by setting HASH_DISABLE = 1 in the "Global ARL Configuration Register" on page 94, in which case the BCM5325E device reverts to the direct addressing method.

Address Learning

Information is gathered from received unicast packets, and learned or stored for the future purpose of forwarding frames addressed to the receiving port. During the receive process the frame information, such as the source address (SA) and VID, is saved until completion of the packet. An entry is created in the ARL table memory if the following conditions are met:

- The packet is not from the Management port.
- The packet has been received without error.
- The packet is of legal length.
- The packet has a unicast SA.
- If using IEEE 802.1Q VLAN, the packet is from a SA that belongs to the indicated VLAN domain.
- There is free space available in memory to which the hashed index points.

When source addresses are dynamically learned, the VALID bit is set, the AGE bit is set, and the STATIC bit is cleared in the entry. See Table 17 on page 25 for a description of a unicast ARL entry.

Multicast addresses are not learned into the ARL table, but must be written via one of the "Programming Interfaces" on page 47. See "Writing an ARL Entry" on page 28 and Table 18 on page 26 for more information.

Address Resolution and Frame Forwarding

Received packets are forwarded based on the information learned or written into the ARL table. Address resolution is the process of locating this information and assigning a forwarding destination to the packet. The destination address (DA) and VID of the received packet is used to calculate a hashed index to the ARL table. The hashed index key is used by the address resolution function to locate a matching ARL entry. The frame is assigned a destination based on the forward field (PORTID or IPMC0) of the ARL entry. If the address resolution function fails to return a matching ARL entry, the packet is flooded to all appropriate ports. The following two sections describe the specifics of address resolution and frame forwarding for "Unicast Addresses" on page 24 and "Multicast Addresses" on page 25.

Unicast Addresses

Frames containing a unicast destination address are assigned a forwarding field corresponding to a single port. Listed below is the unicast address resolution algorithm:

- If the MPORT_ADDR_EN bit is set and the DA matches one of the addresses programmed in the "Multiport Address 1 Register" on page 95 or the "Multiport Address 2 Register" on page 96, the packet is forwarded to the corresponding port map contained in the "Multiport Vector 1 Register" on page 95 or the "Multiport Vector 2 Register" on page 96. See "Using the Multiport Addresses" on page 29 for more information.
- The lower 12 bits of the hashed index key are used as a pointer into the address table memory and both entries in the

bucket are retrieved. The address resolution logic processes the two entries in parallel.

- If the valid indicator is set and the address stored at one of the locations matches the index key of the packet received, the forwarding field port ID is assigned to the destination port of the packet. The packet is then forwarded.
- If the destination port matches the source port, the packet is not forwarded.
- Else, the packet is flooded to all appropriate ports.

If EN_1QVLAN and VLAN Learning Mode bits are set to 1 in the "IEEE 802.1Q VLAN Control 0 Register" on page 137, both the MAC address and the VID are used to compute the hashed index. The following table describes a unicast ARL entry.

Table 17: Address Table Entry for Unicast Address

Field	*Description*
VID	VLAN ID associated with the MAC address
VALID	• 1 = Entry is valid. • 0 = Entry is empty.
STATIC	• 1 = Entry is static, will not be aged out, and is written and updated by software. • 0 = Entry is dynamically learned and aged.
AGE	• 1 = Entry has been accessed or learned since last aging process. • 0 = Entry has not been accessed since last aging process.
Reserved	–
PORTID	Port Identifier. The port associated with the MAC address.
MAC ADDRESS	48-bit MAC address.

Note: The fields described in Table 17 can be written via the "ARL Entry 0 Register" on page 101 and "ARL Entry 1 Register" on page 102.

Multicast ARL table entries are described in Table 18 on page 26.

Multicast Addresses

Frames containing a multicast destination address are assigned a forwarding field corresponding to multiple ports specified in a port map. If the IP_MULTICAST bit is set in the "Multicast IP Address Control Register" on page 83, multicast frames are assigned a forwarding field corresponding to a multicast port map from the matching ARL entry. If no matching ARL entry is found, the packet is flooded to all appropriate ports.

Listed below is the multicast address resolution algorithm:

- If the DA matches one of the globally assigned reserved addresses between 01-80-C2-00-00-00 and 01-80-C2-00-00-2F, the packet is handled as described in Table 19 on page 26.
- If theMPORT_ADDR_EN bit is set and the DA matches one of the addresses programmed in the "Multiport Address 1 Register" on page 95 or the "Multiport Address 2 Register" on page 96, the packet is forwarded to the corresponding port map contained in the "Multiport Vector 1 Register" on page 95 or the "Multiport Vector 2 Register" on page 96. See "Using the Multiport Addresses" on page 29 for more information.
- Otherwise, the lower 12 bits of the hashed index key are used as a pointer into the ARL table memory and both entries in the bucket are retrieved. The address resolution logic processes the two entries in parallel.
- If the valid indicator is set and the address stored at one of the entry locations matches the index key of the packet received, the forwarding field port map is assigned to the destination port of the packet.
- Else, all other multicast and broadcast packets are flooded to all appropriate ports.

If EN_1QVLAN and VLAN Learning Mode bits are set to 1 in the "IEEE 802.1Q VLAN Control 0 Register" on page 137, both the MAC address and the VID are used to compute the hashed index. See Table 18 for a description of a multicast ARL entry. See "Accessing the ARL Table Entries" on page 28 for more information.

Table 18: Address Table Entry for Multicast Address

Field	*Description*
VID	VLAN ID associated with the MAC address
VALID	• 1 = Entry is valid. • 0 = Entry is empty.
STATIC	• 1 = Entry is static, will not be aged out, and is written and updated by software. • 0 = Not defined
AGE	The age bit is ignored for static ARL table entries.
Reserved	–
IPMC0[7:0]	Multicast forwarding mask. The field is a per port vector. Bits[7:0] correspond to CPU port, MII port, and ports[4:0], respectively. • 1 = Forwarding enable • 0 = Forwarding disable
MAC ADDRESS	48-bit MAC address

Note: The fields described in Table 18 can be written via the "ARL Entry 0 Register" on page 101 and "ARL Entry 1 Register" on page 102.

Unicast ARL table entries are described in Table 17 on page 25. The following table summarizes the actions taken for specific reserved multicast addresses. Packets identified with these destination addresses are handled uniquely since they are designed for special functions.

Table 19: Behavior for Reserved Multicast Addresses

MAC Address	*Function*	*IEEE 802.1 Specified Action*	*Default Mode Action (Note 1)*	*Frame-Managed Mode Action*
01-80-C2-00-00-00	Bridge Group Address	Drop Frame	Forward Frame to All Appropriate Ports.	Forward Frame to Frame Management Port Only (Note 2).

Note: Default Mode disables the frame management port option. The IMP (when the MII is used as the interface to the external management subsystem, the port is referred to as the In-band Management Port) does not receive frame data when in this mode. The MII port is treated as a normal network port and have frames forwarded to it in accordance with the entries in the address table.

Note: Frames with the reserved multicast address corresponding to the Bridge Group Address (01-80-C2-00-00-00) are forwarded to the programmed Frame Management Port based on the contents of the BPDU Multicast Address Register (in the ARL Control Register Page). Changing this register from the default value causes frames with the new address to be forwarded to the Frame Management Port, and BPDUs are flooded to all ports except the Frame Management Port.

Note: Frames with the reserved multicast address corresponding to the GMRP or GVRP Addresses (01-80-C2-00-00-20 or 01-80-C2-00-00-21) are forwarded to all ports except the Source and Frame Management Ports. If the switch product implements either of these protocols, then theBCM5325E should be programmed to use the Frame-Managed Mode, and the multicast address should be instantiated in the address table, with a Port ID that forwards the frame to the chip and port with the defined Frame Management Port.

Table 19: Behavior for Reserved Multicast Addresses

MAC Address	*Function*	*IEEE 802.1 Specified Action*	*Default Mode Action (Note 1)*	*Frame-Managed Mode Action*
01-80-C2-00-00-01	IEEE 802.3x MAC Control Frame	Drop Frame	Receive MAC Determines if Valid PAUSE Frame and Acts Accordingly	Receive MAC Determines if Valid PAUSE Frame and Acts Accordingly.
01-80-C2-00-00-02	Reserved	Drop Frame	Drop Frame	Forward Frame to Frame Management Port Only.
01-80-C2-00-00-03	IEEE 802.1x Port-Based Network Access Control	Drop Frame	Drop Frame	Forward Frame to Frame Management Port Only.
01-80-C2-00-00-04~ 01-80-C2-00-00-0F	Reserved	Drop Frame	Drop Frame	Forward Frame to Frame Management Port Only.
01-80-C2-00-00-10	All LANs Bridge Management Group Address	Forward Frame	Forward Frame to All Appropriate Ports.	Forward Frame to All Appropriate Ports.
01-80-C2-00-00-11~ 01-80-C2-00-00-1F	Reserved	Forward Frame	Forward Frame to All Appropriate Ports.	Forward Frame to Frame Management Port Only.
01-80-C2-00-00-20	GMRP address	Forward Frame	Forward Frame to All Appropriate Ports.	Forward Frame to All Appropriate Ports Except Frame Management Port (Note 3).
01-80-C2-00-00-21	GVRP address	Forward Frame	Forward Frame to All Appropriate Ports.	Forward Frame to All Appropriate Ports Except Frame Management Port. (Note 3).
01-80-C2-00-00-22~ 01-80-C2-00-00-2F	Reserved	Forward Frame	Forward Frame to All Appropriate Ports.	Forward Frame

Note: Default Mode disables the frame management port option. The IMP (when the MII is used as the interface to the external management subsystem, the port is referred to as the In-band Management Port) does not receive frame data when in this mode. The MII port is treated as a normal network port and have frames forwarded to it in accordance with the entries in the address table.

Note: Frames with the reserved multicast address corresponding to the Bridge Group Address (01-80-C2-00-00-00) are forwarded to the programmed Frame Management Port based on the contents of the BPDU Multicast Address Register (in the ARL Control Register Page). Changing this register from the default value causes frames with the new address to be forwarded to the Frame Management Port, and BPDUs are flooded to all ports except the Frame Management Port.

Note: Frames with the reserved multicast address corresponding to the GMRP or GVRP Addresses (01-80-C2-00-00-20 or 01-80-C2-00-00-21) are forwarded to all ports except the Source and Frame Management Ports. If the switch product implements either of these protocols, then theBCM5325E should be programmed to use the Frame-Managed Mode, and the multicast address should be instantiated in the address table, with a Port ID that forwards the frame to the chip and port with the defined Frame Management Port.

STATIC ADDRESS ENTRIES

The BCM5325E supports static ARL table entries that are created and updated via one of the "Programming Interfaces" on page 47. These entries can contain either unicast or multicast destinations. The entries are created by writing the entry location via the "Page 0x05: ARL Access Registers" on page 99, and setting the STATIC bit. The AGE bit is ignored. Static

entries do not learn MAC addresses or port associations automatically, and are not aged out by the automatic internal aging process. See “Writing an ARL Entry” on page 28 for details.

ACCESSING THE ARL TABLE ENTRIES

ARL table entries are accessed by one of two mechanisms. The first mechanism uses the ARL Read/Write Control, which allows an address entry location to be read, modified, or written based on the value of a known MAC address. The second mechanism searches the ARL table sequentially, returning all valid entries.

Reading an ARL Entry

The steps for reading an ARL entry:

- Set the MAC address in the “MAC Address Index Register” on page 100.
- Set the VLAN ID in the “VID Table Index Register” on page 101. This is necessary only if the VID is used in the index key.
- Set the ARL_R/W bit to 1 in the “ARL Read/Write Control Register” on page 100.
- Set the START/DONE bit to 1 in the “ARL Read/Write Control Register” on page 100. This initiates the read operation.

The MAC address and VID are used to calculate the hashed index to the ARL table. The matching ARL bucket is read. The contents of entry 0 are stored in the “ARL Entry 0 Register” on page 101. The contents of entry 1 are stored in the “ARL Entry 1 Register” on page 102.

Entries that do not have the VALID bit set should be ignored. The contents of the MAC/VID registers must be compared against the known MAC address and VID. Entries that do not match may be a valid entry, but are not a valid match for the index key. All other read entries are considered valid ARL entries.

Writing an ARL Entry

The steps for writing an ARL entry:

- Follow the steps above to read the ARL entry matching the MAC address and VID that is written to the table.
- Keep the values of the “MAC Address Index Register” on page 100, the “VID Table Index Register” on page 101, the “ARL Entry 0 Register” on page 101, the “ARL Entry 1 Register” on page 102 that are left from the previous read operation.
- Determine which ARL entry (0 or 1) is to be written based on the existing values of the VALID bit, and MAC/VID bits.
- Modify the “ARL Entry 0 Register” on page 101 or the “ARL Entry 1 Register” on page 102 as necessary. Set the STATIC bit so that the entry is not aged out.
- Set the ARL_R/W bit to 0 in the “ARL Read/Write Control Register” on page 100.
- Set the START/DONE bit to 1 in the “ARL Read/Write Control Register” on page 100. This initiates the write operation.

The MAC address and VID are used to calculate the hashed index to the ARL table. Both entry 0 and entry 1 are written to the matching ARL bucket.

Searching the ARL Table

The second way to access the ARL table is through the ARL Search Control. The entire ARL table is searched sequentially, revealing each valid ARL entry. Setting the START/DONE bit in the “ARL Search Control Register” on page 104 begins the search from the top of the ARL table. This bit is cleared when the search is complete. During the ARL search, the ARL_SR_VALID bit indicates when a found valid 76-bit entry is available in the “ARL Search Result Register” on page 105 and the “ARL Search Result Extension Register” on page 106. When the host reads the contents of the “ARL Search Result

Register" on page 105, the search process automatically continues to seek the next valid entry in the address table. Invalid address entries are skipped, providing the host with an efficient way of searching the entire address table.

The ARL Search and ARL Read/Write operations execute in parallel with other register accesses. This allows the host processor to start a read, write or search process, and then read/write other registers, returning periodically to see if the operation has completed.

ADDRESS AGING

The aging process periodically removes dynamically learned addresses from the ARL table. When an ARL entry is learned or referenced, the AGE bit is set to 1. The aging process scans the ARL table at regular intervals, aging out entries not accessed during the previous 1 to 2 aging intervals. The aging interval is programmable via the AGE_TIME bits in the "Aging Time Control Register" on page 90. Aging is disabled by setting the AGE_TIME bits to 0.

Entries that are written and updated via one of the "Programming Interfaces" on page 47, should have the STATIC bit set. Thus, they are not affected by the Aging Process.

For each entry in the ARL table, the Aging Process performs the following if the VALID bit is:

- Not set, then do nothing.
- Set and the STATIC is set, then do nothing.
- Set, the STATIC bit is not set, and the AGE bit is set, then clear the AGE bit. This keeps the entry in the table, but marks it such that it is removed if it is not accessed before the subsequent Aging scan.
- Set, the STATIC bit is not set, and the AGE bit is reset, then reset the VALID bit. This effectively deletes the entry from the ARL table. The entry has been aged out.

USING THE MULTIPORT ADDRESSES

In addition to the ARL table, the "Multiport Address 1 Register" on page 95 and "Multiport Address 2 Register" on page 96 can be used. Packets with a corresponding DA are forwarded to the port map contained in the "Multiport Vector 1 Register" on page 95 or the "Multiport Vector 2 Register" on page 96. These registers must be enabled via the MPORT_ADDR_EN bit in the "Global ARL Configuration Register" on page 94. While the name suggests that these registers are used only for multiport forwarding, they can be used for multicast or unicast addresses, and the forwarding map can include one or more ports.

BRIDGE MANAGEMENT

To support Bridge Management the BCM5325E provides the following services:

- Bridge Management state register access through the CPU interface
- Bridge Protocol Data Unit (BPDU) frame forwarding through the CPU interface or the MII interface

SPANNING TREE PORT STATE

The BCM5325E device supports the Spanning Tree Protocol (STP) by providing the spanning tree state in the Port Control Register for each of the six network ports. Each Port Control Register (PCR) contains 3 bits dedicated to STP state (STP_STATE[2:0]) as well as additional bits to control the operation of the MAC port.

In the Frame Management mode of operation (FRAME_MANAGE_MODE = Frame Management), the default state of the STP_STATE[2:0] bits are all 0s, and no spanning tree state is maintained. Write operations to the spanning tree state bits are ignored. Frames are forwarded based only on their DA. Known unicast address frames are forwarded to their single defined destination port, and unknown unicast, as well as all multicast/broadcast addressed frames, are flooded to all ports, with the exception of the management port, providing SW_FWDG_EN = 1. BPDU frames, are one of the IEEE 802.1 reserved multicast addresses that the unmanaged mode floods. For a complete list of the forwarding behavior of the unmanaged address resolution logic, see Table 19 on page 26.

In the Frame Management mode of operation (FRAME_MANAGE_MODE = Frame Management), six ports are considered network ports, and can have STP port state associated with them, these being the 5 integral 10BASE-T/100BASE-TX ports, and the MII port. The MII port, when configured as the In-band Management Port (IMP), also has no STP state associated with it.

The following section describes how the BCM5325E reacts to the STP state bits as written by the management CPU (providing SW_FWDG_EN = 1).

Disable

In this state, all frames received by the port are discarded. The port also does not forward any transmit frames, queued by either BCM5325E receive network ports, or frames cast by the management entity via the IMP. Addresses are not learned by ports in the Disabled state. This is the default state that the BCM5325E powers up in when FRAME_MANAGE_MODE = Enabled.

Blocking

In this state, the MAC port forwards received BPDUs to the designated Frame Management port. All other frames received by the port are discarded and the addresses are not learned. The port won't forward any transmit frames, queued by other BCM5325E receive network ports. Note that the Blocking and Listening states of all BCM5325E ports are identical. The external management processor running the STP algorithm must distinguish these two states using the STP algorithm, but is able to store the Blocking and Listening state information into the BCM5325E for consistency. However, the BCM5325E forwards frames cast by the Frame Management entity. It is the responsibility of the processor not to issue BPDUs or other frames to a port in the Blocking state.

Listening

In this state, the MAC port forwards received BPDUs to the designated Frame Management port. All other frames received by the port are discarded and the addresses are not learned. The port won't forward any transmit frames, queued by other BCM5325E receive network ports, but transmits frames cast by the management entity as expected (such as BPDUs). Note that the Blocking and Listening states of all BCM5325E ports are identical. The external management processor running the STP algorithm must distinguish these two states using the STP algorithm, but is able to store the Blocking and Listening state information into the BCM5325E for consistency.

Learning

In this state the MAC port forwards received BPDUs to the Frame Management port, transmits BPDUs sent into the Frame Management port, and learns incoming frames' MAC addresses. All other frames received by the port are discarded.

Forwarding

In this state the MAC port forwards received BPDUs to the Frame Management port, transmits BPDUs sent into the Frame Management port, forwards all other frames and learns all in coming frames' MAC addresses.

Table 20: Spanning Tree State

Spanning Tree State	*Receive BPDU*	*Transmit BPDU*	*Normal Frames*	*Address Learning*	*STP_STATE [3:0]*
No Spanning Tree	Treated as Broadcast	Flood to all ports except Management Port and source port	Forward	Learn	000
Disabled	Disabled	Disabled	Don't Forward	Don't Learn	001
Blocking	Forward to Management	Disabled	Don't Forward	Don't Learn	010
Listening	Forward to Management	Enabled	Don't Forward	Don't Learn	011
Learning	Forward to Management	Enabled	Don't Forward	Learn	100
Forwarding	Forward to Management	Enabled	Forward	Learn	101

MANAGEMENT FRAMES

Management frames received by the BCM5325E are forwarded to the Bridge Management entity (an external CPU or microcontroller). When the MII is used as the interface to the external management subsystem the port is referred to as the In-band Management Port (IMP). Note that when operating in the unmanaged mode, management frames are treated differently, as defined in Table 19 on page 26. The following frames are forwarded to the Bridge Management entity in the managed mode:

- BPDU Frames—BPDUs are identified by the Bridge Group Address (01-80-C2-00-00-00) in the destination address field of a frame. The STP_STATE bits in the Port Control Register must be configured to permit BPDU reception on a particular port. A BPDU received on such a port is forwarded, with the Port ID of the receiving port, to the port configured in the Management Port ID register.
- Reserved Multicast Addressed Frames—Frames with IEEE 802.1 administered Reserved Multicast Addresses (between 01-80-C2-00-00-02 and 01-80-C2-00-00-0F in their DA field are forwarded only to the Management Port, with a header which includes the Port ID of the port from which the frame was received. Frames with thee All LANs Bridge Management Group Address (01-80-C2-00-00-10) as the DA are forwarded to all ports, with the Management Port again receiving the header information to identify the Port ID from which the frame was received.
- Directed Management Agent Frames—Packets with the DA equal to one of the MAC addresses associated with the Management Port. These addresses are generally entered as Static addresses by the management entity itself.
- Mirrored Frames—Ingress or egress port frames that have been assigned to be mirrored to the management port.

To transmit a frame from the Frame Management port, the management agent is responsible to encapsulate the actual management frame which is transmitted in its entirety, within an additional header and FCS field. The definition of this frame format is defined in Table 25 on page 40. For transmitted management frames, the resolution rule is as follows if the header OPCODE (see Table 24 on page 39) indicates that the frame is:

- A normal unicast or multicast address, then the frame is forwarded according to the address table resolution. Frames with broadcast addresses or multicast addresses not found in the address table are flooded to all ports.
- An Egress Directed frame, then the frame is forwarded to the Port ID identified in the header.

Section 3: System Functional Blocks

Overview

The BCM5325E includes the following functional blocks:

Media Access Controller

The BCM5325E contains six internal dual-speed MACs. The MACs automatically select 10-Mbit or 100-Mbit mode, CSMA/CD or full-duplex, based on the result of auto-negotiation. In FDX mode, IEEE 802.3x PAUSE-frame-based flow control is also determined through auto-negotiation. The MACs are compliant with IEEE 802.3, IEEE 802.3u, and IEEE 802.3x specifications.

Receive Function

The MAC initiates frame reception following the assertion of receive data valid indication from the physical layer. The MAC monitors the frame for the following error conditions:

- Receive error indication from the PHY
- Runt frame error if frame is fewer than 64 bytes
- CRC error
- Long frame error if frame is greater than 1536 bytes

If no errors are detected the frame is processed by the switch controller. Frames with errors are discarded.

TRANSMIT FUNCTION

Frame transmission begins with the switch controller queuing a frame to the MAC transmitter. The frame data is transmitted as received from the switch controller. The transmit controller is responsible for preamble insertion, carrier deferral, collision backoff, and inter-packet gap enforcement.

In half-duplex mode, when a frame is queued for transmission, the transmit controller behaves as specified by the IEEE 802.3 requirements for frame deferral. Following deferral, the transmitter adds 8 bytes of preamble and SFD to the frame data received from the switch controller. If, during frame transmission, a collision is observed and the collision window timer has not expired, the transmit controller asserts jam and then executes the backoff algorithm. The frame is retransmitted when appropriate. On the sixteenth consecutive collision the backoff algorithm starts over at the initial state, the collision counter is reset and attempts to transmit the current frame continuously. Following a late collision, the frame is aborted and the switch controller is allowed to queue the next frame for transmission.

While in full-duplex mode, the transmit controller ignores carrier activity and collision indication. Transmission begins after the switch controller queues the frame and the 96 bit times of IPG have been observed.

FLOW CONTROL

The BCM5325E implements an intelligent flow control algorithm to minimize the system impact resulting from flow control measures. Buffer memory allocation is adaptive to the status of each port's speed and duplex mode, providing an optimal balance between flow management and per-port memory depth. The BCM5325E initiates flow control in response to buffer memory conditions on a per-port basis.

The MACs are capable of flow control in both full-and half-duplex modes. In half-duplex mode, the MAC back pressures a receiving port by transmitting a 96-bit time-jam packet to the port. A single jam packet is asserted for each received packet for the duration of the time the port is in the flow control state.

Flow control in full-duplex mode functions as specified by the IEEE 802.3x requirements. In the receiver, MAC flow control frames are recognized and, when properly received, set the flow control pause time for the transmit controller. The pause time is assigned from the 2-byte pause time field following the pause opcode. MAC control PAUSE frames are not forwarded from the receiver to the switch controller.

When the switch controller requests flow control from a port, the transmit controller transmits a MAC control PAUSE frame with the pause time set to the PAUSE_QUANTA register value (default is set to maximum). When the condition that caused the flow control state is no longer present, a MAC control PAUSE frame is sent with the pause time field set to 0.

The flow control capabilities of the BCM5325E are enabled based on the results of auto-negotiation and the state of the ENFDXFLOW and ENHDXFLOW control signals loaded during reset. Flow control in half-duplex mode is independent of the state of the link partner's flow control capability. The following table provides for more detailed information.

Table 21: Flow Control Modes

LPFCCAP	*ENFDXFlow*	*ENHDXFLOW*	*Flow Control*	
			Full-Duplex	*Half-Duplex*
X	X	0	–	Disabled
X	X	1	–	Enabled
0	0	X	Disabled	–
0	1	X	Disabled	–
1	0	X	Disabled	–
1	1	X	Enabled	–

Note: LPFCCAP: Link Partner Flow Control Capability. Obtained from Result of auto-negotiation.

PHYSICAL LAYER TRANSCEIVER

ENCODER/DECODER

In 100BASE-TX mode, the transceiver transmits and receives a continuous data stream on twisted pair. During transmission, nibble wide (4-bit) data from the MAC is encoded into 5-bit code groups and inserted into the transmit data stream. The transmit packet is encapsulated by replacing the first two nibbles of preamble with a start of stream delimiter (J/K codes) and appending an end of stream delimiter (T/R codes) to the end of the packet. When the MII transmit error input is asserted during a packet, the transmit error code group (H) is sent in place of the corresponding data code group. The transmitter repeatedly sends the idle code group in between packets.

In 100BASE-TX mode, the encoded data stream is scrambled by a stream cipher block and then serialized and encoded into MLT3 signal levels. A multimode transmit DAC is used to drive the MLT3 data onto the twisted pair cable.

Following baseline wander correction, adaptive equalization and clock recovery in 100BASE-TX mode, the receive data stream is converted from MLT3 to serial NRZ data. The NRZ data is descrambled by the stream cipher block and then deserialized and aligned into 5-bit code groups.

The 5-bit code groups are decoded into 4-bit data nibbles and provided as the input data stream to the MAC. The start of stream delimiter is replaced with preamble nibbles and the end of stream delimiter and idle codes are replaced with all zeros. When an invalid code group is detected in the data stream, the transceiver asserts a receiver error indication to the MAC.

In 10BASE-T mode, Manchester encoding and decoding is performed on the data stream. The multimode transmit DAC performs pre-equalization for 100 meters of CAT-3 cable.

LINK MONITOR

In 100BASE-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. Signal levels are qualified using squelch detect circuits. When no signal or certain invalid signals are detected on the receive pair, the link monitor enters and remains in the Link Fail state where only idle codes are transmitted. When a valid signal is detected on the receive pair for a minimum period of time, the link monitor enters the Link Pass state and the transmit and receive functions are enabled.

In 10BASE-T mode, a link-pulse detection circuit constantly monitors the RD+/- pins for the presence of valid link pulses.

COLLISION DETECTION

In half-duplex mode, collisions are detected whenever the transceiver is simultaneously transmitting and receiving activity.

AUTOMATIC MDI CROSSOVER (AUTO-MDIX)

During auto-negotiation, one end of the link needs to perform an MDI crossover so that each transceiver's transmitter is connected to the other receiver. The BCM5325E can perform an automatic media dependent interface (MDI) crossover, eliminating the need for crossover cables or cross-wired (MDIX) ports. During auto-negotiation, the BCM5325E normally transmits on the RD± pin and receives on the TD± pin.

When connecting to another device that does not perform MDI crossover, the BCM5325E automatically switches its TD/RD± pin pairs when necessary to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function. The pair swaps automatically occur within the device and do not require user intervention.

AUTO-NEGOTIATION

Each internal transceiver contains the ability to negotiate its mode of operation over the twisted pair link using the auto-negotiation mechanism defined in the IEEE 802.3u specification. During auto-negotiation, each port automatically chooses its mode of operation by advertising its abilities and comparing them with those received from its link partner. The BCM5325E is configured to advertise IEEE 802.3x flow-control capability, and can also advertise that it is Next Page capable. The transceiver negotiates with its link partner and chooses the highest level of operation available for its own link. In FDX mode, flow control is also negotiated. In HDX mode, flow control is enabled/disabled based on pin strappings. The auto-negotiation algorithm supports the Parallel Detection function for legacy 10BASE-T devices and 100BASE-TX-only devices that do not support auto-negotiation. Auto-negotiation in the BCM5325E device also allows the optional Next Page capability to be advertised, and permits Next Page exchange with a similarly capable link partner. Next Page exchange sequences and their contents are controlled via software control of the on-chip registers.

DIGITAL ADAPTIVE EQUALIZER

The digital adaptive equalizer removes inter-symbol interference created by the transmission channel media. The equalizer accepts sampled unequalized data from the ADC on each channel and produces equalized data. The BCM5325E achieves an optimum signal-to-noise ratio by using a combination of feed-forward equalization and decision-feedback equalization. This powerful technique achieves a 100BASE-TX BER of less than 1×10^{-12} for transmission up to 100 meters on CAT-5 twisted-pair cable, even in harsh noise environments. The digital adaptive equalizers in the BCM5325E achieve performance close to theoretical limits. The all-digital nature of the design makes the performance very tolerant to on-chip noise. The filter coefficients are self-adapting to any quality of cable or cable length. Due to transmit pre-equalization in 10BASE-T mode and complete lack of ISI in 100BASE-FX mode, the adaptive equalizer is bypassed in these two modes.

ADC

The receive channel has a 6-bit, 125-MHz Analog-to-Digital Converter (ADC). The ADC samples the incoming data on the receive channel and produces a 6-bit output. The output of the ADC is fed to the digital adaptive equalizer. Advanced analog circuit techniques achieve low-offset, high-power supply noise rejection, fast settling time, and low bit error rate.

DIGITAL CLOCK RECOVERY/GENERATOR

The all-digital clock recovery and generator block creates all internal transmit and receive clocks. The transmit clock is locked to the 25-MHz clock input while the receive clock is locked to the incoming data stream. Clock recovery circuits optimized to MLT3, NRZI, and Manchester encoding schemes are included for use with each of the three different operating modes. The input data stream is sampled by the recovered clock and fed synchronously to the digital adaptive equalizer.

BASELINE WANDER CORRECTION

A 100BASE-TX data stream is not always DC balanced. Because the receive signal must pass through a transformer, the DC offset of the differential receive input can wander. This effect, known as baseline wander, can greatly reduce the noise immunity of the receiver. The transceiver automatically compensates for baseline wander by removing the DC offset from the input signal, and thereby significantly reduces the chance of a receive symbol error.

DIGITAL TO ANALOG CONVERTER

The multimode transmit Digital-to-Analog Converter (DAC) transmits MLT3-coded symbols in 100BASE-TX mode and Manchester-coded symbols in 10BASE-T mode. It performs programmable edge-rate control in 100BASE-TX mode, which decreases unwanted high frequency signal components, thus reducing EMI. High-frequency pre-emphasis is performed in 10BASE-T mode. The transmit DAC utilizes a current drive output that is well balanced and produces very low noise transmit signals.

STREAM CIPHER

In 100BASE-TX mode, the transmit data stream is scrambled to reduce radiated emissions on the twisted-pair cable. The data is scrambled by exclusive ORing the NRZ signal with the output of an 11-bit-wide Linear Feedback Shift Register (LFSR), which produces a 2047-bit, non-repeating sequence. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range and eliminating peaks at certain frequencies.

The receiver descrambles the incoming data stream by exclusive ORing it with the same sequence generated at the transmitter. The descrambler detects the state of the transmit LFSR by looking for a sequence representing consecutive idle codes. The descrambler locks to the scrambler state after detecting a sufficient number of consecutive idle code groups. The receiver does not attempt to decode the data stream unless the descrambler is locked. When locked, the descrambler continuously monitors the data stream to make sure that it has not lost synchronization. The receive data stream is expected to contain inter-packet idle periods. If the descrambler does not detect enough idle codes within 724 ms, it becomes unlocked, and the receive decoder is disabled. The descrambler is always forced into the unlocked state when a link failure condition is detected.

Stream cipher scrambling/descrambling is not used in 10BASE-T modes.

100BASE-FX FIBER MODE

The 10/100 port can be configured to operate in the 100BASE-FX compatible mode. The following sequence is required for configuring the preferred PHY ports to 100BASE-FX-compatible operation using a register write from the CPU. Each port's register can be programmed through page 0x10-0x14 respectively. A global write to page 19h enables writing to all the five ports' registers.

1. Write 2100h to the Table 104 on page 115. This forces the port to 100M full-duplex without auto-negotiation. Most FX applications require configuration for full-duplex.
2. Set bit 5 and bit 9 of the Table 113 on page 120. Bit 9 bypasses the scrambler and descrambler blocks (these scrambling functions are not required for 100BASE-FX operation). Additionally, setting bit 5 enables the 100BASE-FX Far-End-Fault function. Other bits within this register may already be set, so it is best to perform a read-modified write to ensure proper setting of this register.
3. Set bit 5 of hidden register address 0x2E–0x2F (pages 0x10–0x14). This changes the three-level MLT-3 code transmitted by the PHY to two-level binary, suitable for driving standard fiber transceivers. Additionally, the PHY receiver is configured to recognize binary signaling. This register access must also be in the form of a read-modified write.
4. Enable Internal EFX Signal Detect Function by writing to the following hidden registers:
   a. Write 0x008B to register 0x3E-0x3F (pages 0x10–0x14). This enables the shadow register.
   b. Write 0x0200 to register 0x32-0x33 (pages 0x10–0x14). This enables the internal Signal Detect function.
   c. Write 0x0084 to register 0x3A-0x3B (pages 0x10–0x14). This configures the TX amplitude for 1V pk-pk differential.
   d. Write 0x000B to register 0x3E-0x3F (pages 0x10–0x14). This disables the shadow register.
5. Set or Clear bits [9:0] of register address 0x26–0x27 (page 0x00). Setting bit 9 enables the full-duplex Flow Control Override function required because auto-negotiation has been disabled. Bits 8:0 allow individual per-port selection of Flow Control as desired (where bit 8 = MII, bit 7 = port 7... bit 0 = port 0).

For FX termination requirement, refer to the *Enhanced-FX-AN100 Application Note*.

FRAME MANAGEMENT

The BCM5325E provides a Frame Management block that works in conjunction with a selectable port interface to receive forwarded management frames directed to the switch. An external CPU connects via the selected port interface to process the forwarded frames and respond appropriately.

INDEPENDENT MANAGEMENT PORT

The MII Port can be designated as the Frame Management port, and is thus referred to as the Independent Management Port (IMP). This can be used to forward extensive management information to the external management agent, such as BPDUs, mirrored frames, or frames addressed to other static address entries that have been identified as a special interest to the management system.

Unicast, Multicast, and Broadcast traffic is forwarded to the IMP based on the state of the RX_UCST_EN, RX_MCST_EN and RX_BCST_EN bits of the "MII Port Control Register" on page 78, respectively. If these bits are cleared, no frame data is forwarded to the Frame Management Port, with the exception that frames meeting the Port Mirroring criteria.

The BCM5325E device intrusively tags frames destined to the management entity to allow the identity of the originating ingress port of a frame to be retained. Additional header information is inserted into the original frame, between the original SA field and Type/Length fields. The tag includes the BRCM Type (8874h) field and the BRCM Tag field. A recalculated FCS is appended to the resultant frame, before the frame is forwarded. The Management frame format is defined in the following table.

Table 22: Transmit/Receive Frame Format Over Management Port

Destination Address	Source Address	BRCM Type	BRCM Tag (32 bits)	Original Type/Length	Frame Data	Original FCS	Recalculated FCS

Similarly, the host system must insert the BRCM Type/Length and Tag fields into frames it wishes to send into the management port, to be routed to specific egress ports. The OPCODE within the Tag field determines how the frame is handled, and allows frames to be forwarded using the normal address lookup or via a Port ID designation within the Tag.

The BRCM Tag and BRCM Type/Length fields are transmitted with the convention of highest significant octet first, followed by next lowest significant octet, etc., and with the least significant bit of each octet transmitted out from the MAC first. So for the BRCM Type/Length field in Table 23 on page 38, the most significant octet would be transmitted first (bits 24:31), with bit 24 being the first bit transmitted.

Table 23 shows the format of the BRCM Tag field. The OPCODE field slightly modifies the use and validity of some fields in the Tag. Table 24 defines the supported OPCODEs, and Table 25 on page 40 identifies each of the other fields in the BRCM Tag in detail.

Table 23: BRCM Tag Format

31 29	28	27	26 16	15 12	11 10	9 8	7 6	5 4	3 2 1 0
Opcode= Unicast	MIR	MO	Frame Octet Count	Rsved		Dest Dev ID	Rsved	Scr Dev ID	Scr Port ID
Opcode= Multicast	MIR	MO	Frame Octet Count	Reserved				Scr Dev ID	Scr Port ID
Opcode= Egress Dir	MIR	MO	Frame Octet Count	Rsved		Dest Dev ID	Rsved	Scr Dev ID	Dest Port ID
Opcode= Ingress Dir	MIR	MO	Frame Octet Count	Rsved				Scr Dev ID	Scr Port ID

Table 24: OPCODE Field in BRCM Tag for Management Port Frame

OpCodes	*Name*	*Description*
0 0 0	Unicast	Normal unicast frames are forwarded using the address table lookup of the DA contained in the frame. If the address is unknown, the frame is flooded. The Source Device ID and Source Port ID fields in the BRCM Tag are required for the learning process. The management port may transmit or receive frames with this format.
0 0 1	Multicast	Normal multicast frames are forwarded using the address lookup of the DA contained in the frame. If the address is located in the address table, or the Multiport Address registers, it is forwarded to the port(s) specified in the entry. The Source Device ID and Source Port ID fields in the BRCM Tag are required for the learning process. The management port may transmit or receive frames with this format.
0 1 0	Egress Directed	An Egress Directed frame is sent by the host management system into the IMP port, and is forwarded to the Egress Port specified in the Destination Device ID and Destination Port ID fields in the BRCM Tag.
0 1 1	Ingress Directed	Frame received at an ingress port which had a destination address corresponding either to the Bridge Group (BPDU) Address or the All LAN Bridge Management Group (ALBMGA) Address. The Source Device ID and Source Port ID identify the ingress port the frame was initially received on.
1 x x	Reserved	Reserved

Table 25: Field in BRCM Tag for Management Port Frame

Field	*Name*	*Description*
MIR	Mirror Bit	The Mirror Bit tag is applied at the mirrored port. Ingress data received at an Ingress Mirror Port be classified as standard frame type (i.e., Unicast, Multicast, Ingress Frame-BPDU, etc.). Egress data transmitted at an Egress Mirror Port is classified there - mirrored egress frames are classified as standard frame types at the ingress port.
MO	Mirror Only	Indicates to ARL that the frame should only be forwarded to Mirroring port.
	Frame Octet Count	This 11-bit field incorporates the Octet Count of the entire Ethernet frame octet count starting at the DA field and inclusive of CRC, but not including the BRCM Type, BRCM Tag, and recalculated FCS.
Dest DevId	Destination Device ID	A 2-bit Chip ID field which indicates the destination Chip ID for Egress Directed frames.
Dest Portid	Destination Port ID	Indicates the destination Port ID for Egress Directed frames.
Reserved	Reserved	00
Src Portid	Source Port ID	Indicates the source Port ID for ingress directed frames.

SWITCH CONTROLLER

The core of the BCM5325E device is a cost effective and high performance switch controller. The controller manages packet forwarding between the MAC receive and transmit ports through the frame buffer memory with a store and forward architecture. The switch controller encompasses the functions of buffer management, memory arbitration and transmit descriptor queueing.

BUFFER MANAGEMENT

The frame buffer memory is divided into 256 bytes per page. Each packet received may allocated more than one page, of which, six pages are required for storing maximum 1536B frame data. Frame data is stored to the memory block as the packet is received. After reception, the frame is queued to the egress port(s) transmit queue. For unicast frames, following transmission of a packet from the frame buffer memory, the block of memory for the frame is released to the free buffer pool. If the frame is destined to multiple ports, the memory block is not released until all ports complete transmission of the frame.

MEMORY ARBITRATION

Processes requesting access to the internal memory include the receive and transmit frame data handlers, address resolution, learning and aging functions, and output port queue managers. These processes are arbitrated to provide fair access to the memory and minimize latency of critical processes to provide a fully nonblocking solution.

TRANSMIT OUTPUT PORT QUEUES

When the Quality of Service (QoS) function is turned off, the switch controller maintains an output port queue for each port. The queues are located in the internal memory and the maximum depth of the queue is 336 (i.e., 336 transmit descriptors). The queue depth becomes 256 for each output port when the QoS function is on. Transmit descriptors are updated after the packet has been received and the destination port resolved. One or two transmit descriptors are assigned to each destination port queue linking the destination with the frame data. For packets which have frame sizes larger than 1024 bytes, two transmit descriptors are required. In the case of multicast and broadcast packets, a transmit descriptor for the packet is assigned to the transmit descriptor queues of multiple ports.

For each port, frames are initiated for transmission with minimum IPG until the transmit descriptor queue of the port is empty.

When QoS is turned on, the single queue is split into four equal-sized priority queues. These four queues are maintained by the switch controller for each transmit port. When the receiving frame is identified by the QoS mechanism as specific priority, it is stored in its appropriate queue. The weighted fair scheduling is applied to the queues to select frames from both queues and prevent starvation.

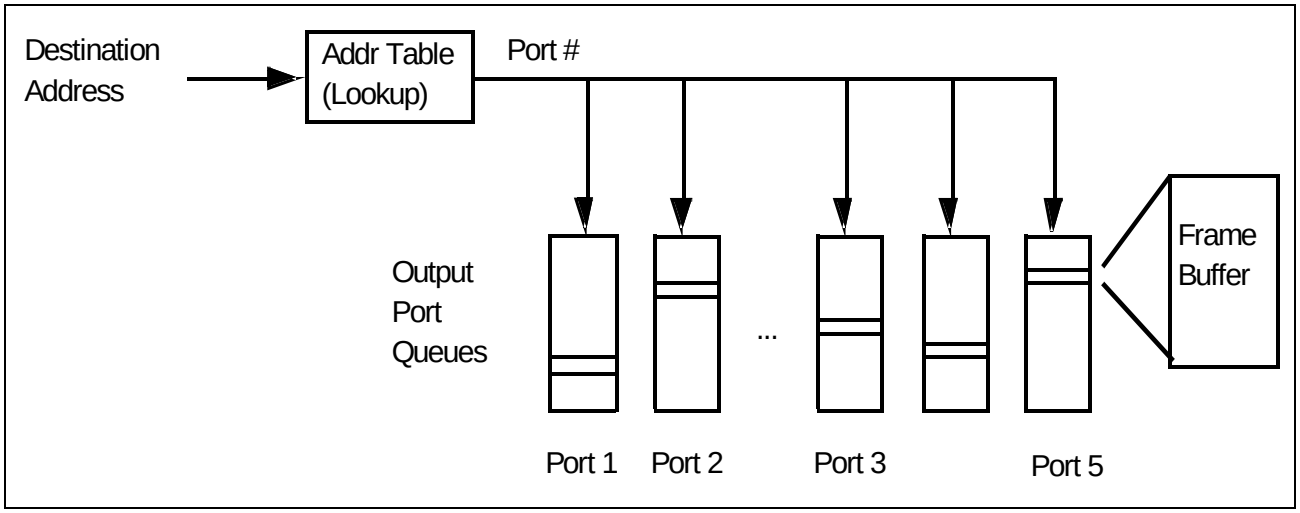


Figure 9: Transmit Output Queues

INTEGRATED HIGH-PERFORMANCE MEMORY

The BCM5325E includes 64 KB of integrated, high-performance RAM which stores all packet buffer and address table information; and eliminates the need for external memory. This allows for the implementation of extremely low-cost systems.

The internal RAM controller efficiently executes memory transfers and achieves non-blocking performance for five/six-port applications.

CLOCKING

The BCM5325E provides simple clock selection. From a single 25-MHz clock input, the device's internal clocks can operate anywhere from 50 MHz to 83 MHz; this effects the operation of the system logic and internal RAM. These options allow the best trade-offs with respect to performance, cost, and power.

MIB ENGINE

The Management Information Base (MIB) Engine is responsible for processing status words received from each port. Based on whether it is a receive status or transmit status, appropriate MIB counters are updated. The BCM5325XCT has two groups of four MIB counters on a per-port basis, and only one group of counters is used at a time.

MIB COUNTERS PER PORT

There are 8 MIB counters per port and are separated into two groups. The users can only select one group. The grouping info is shown below. The Table 62 on page 89 is used to select the group. The Table 126 on page 128 and Table 127 on page 129 contains the per port MIB values.

Group 0

- RxGoodPackets (16-bit)–The total number of bytes in all good packets received by a port (excluding framing bits but including FCS).
- TxPacket (16-bit)–The total number of good bytes of data transmitted by a port (excluding preamble but including FCS).
- RxUnicastPkts (16-bit)–The number of good packets received by a port that are addressed to a unicast address.
- TxUnicastPkts (16-bit)–The number of good packets transmitted by a port that are addressed to a unicast address.

Note: Group 0 counters are counting statistics in number of packets.

Group 1

- RxFCSErrors (16-bit)–The number of packets received by a port that have a length (excluding framing bits but including FCS) between 64 and 1522 bytes inclusive, and have a bad FCS with an integral number of bytes.
- TxCollisions (16-bit)–The number of collisions experienced by a port during packet transmissions.
- RxGoodOctets (16-bit)–The total number of bytes in all good packets received by a port (excluding framing bits but including FCS).
- TxOctets (16-bit)–The number of good packets transmitted by a port that are addressed to a unicast address.

Total number of counters per port: 4 x 2

Note: Group 1 counters are counting statistics in number of bytes.

The counter values in both groups are not available at the same time. (For example, switching the group in the middle of operation does not show the updated count value.) By selecting a group, the user is enabling the counters of the selected group, the counters in the unselected group are not counting.

Section 4: System Interfaces

Overview

The BCM5325E includes the following system interfaces:

MII Port

The BCM5325E provides a fully IEEE 802.3u-compatible MII interface as the sixth network port. This port can be configured to operate in Reverse MII mode by hardware strapping or by programming of the internal register. For more information, see "Reverse MII Port" on page 45.In its default mode after power-up, the MII operates as a normal MAC-based MII port, capable of interfacing directly to an external TX or FX transceiver. The port incorporates a sixth internal 10/100 Mbps MAC, and functions identically to the five integrated 10/100 Mbps ports. Frames are forwarded to the port under control of the forwarding model defined in Table 19 on page 26, depending on the state of the SW_FWDG_EN bit in the "Switch Mode Register" on page 79 and the state of the MANAGE_PORT bits in the "Global Management Configuration Register" on page 89.

Predecessors of the BCM5325E device allowed the MII management signals (MDC/MDIO) to interrogate the internal MII registers associated with the five integrated 10/100 Mbps PHYs. The BCM5325E can still support this mode, in which case configuration of the integrated PHYs requires the 2.5-MHz clock to be supplied to the BCM5325E MDC pin and any external MII-connected transceiver, and the external management device controls MDIO to select and configure all the PHYs appropriately. To operate in this mode, the external transceiver needs to support some signals in addition to the standard MII signals, so that the state of the external transceiver can be monitored by the BCM5325E. Individual active-low Link, Speed (100 Mbps), Duplex, and link partner Flow Control mode signals from the transceiver should be provided. An MII-based single 10/100 Mbps PHY, such as the BCM5202, provides these additional signals. With these additional signals, the BCM5325E generates port LEDs for the external MII-based PHY, equivalent to the LEDs of the internal transceivers.

The more typical use of the MII in a BCM5325E implementation is that the device is managed via the SPI interface. In this case, on sensing activity of the SPI interface, the BCM5325E takes control of the MII management pins, and sources the 2.5-MHz clock signal for MDC. The external PHY can be accessed by the management entity, since its MII registers are aliased to the Port 8 MII registers (Page 0x18). Access to MII registers in this page in the register map automatically generates an MDIO/MDC request to the external MII-based transceiver, allowing configuration control and status monitoring of the off-chip PHY port. The MII port uses the unique PHY address of A#A#_000 where A#A# is the bit inversion of the CHIP ID[1:0] bits. So the MII PHY address for CHIP ID[1:0] = 001 would be 10_000. The external PHY must be programmed/strapped to respond to the CHIP ID dependent PHY address. See Table 38 on page 75 for additional detail on internal and external PHY address values.

When an external transceiver is connected to the BCM5325E MII port and managed by the MDC/MDIO lines, the state of the link, speed, full/half-duplex and link partner flow control capabilities (among many others) can all be accessed via

software, and need not be provided as hardware pins. In order to preserve LED display capabilities for the MII port, an additional alias register is provided in the Control registers (Page 0x0), defined as the MII Port State Override register (Address 0x0E). This allows these status bits to be read from the external PHY and then written to this register, so that consistent LED status information for all six 10/100 ports can be preserved.

If no MII-based external transceiver is present, page 0x18 of the register space is not present, and returns indeterminate data when read.

REVERSE MII PORT

The BCM5325E device includes an enhanced MII mode that supports direct MAC-to-MAC connectivity. The BCM5325E device supports hardware or software selectable Reverse MII mode, which makes the BCM5325E MII interface appear as a 100-Mbps full-duplex PHY MII, as seen by the external MAC.

To support this Reverse MII mode, the clock-to-data timing has been modified. The TXC/RXC input clocks become 25-MHz clock outputs (identical to those of a PHY MII) that only support a 100-Mbps MII interface. Figure 10 shows the normal MII configuration and Figure 11 on page 46 shows the Reversed MII configuration.

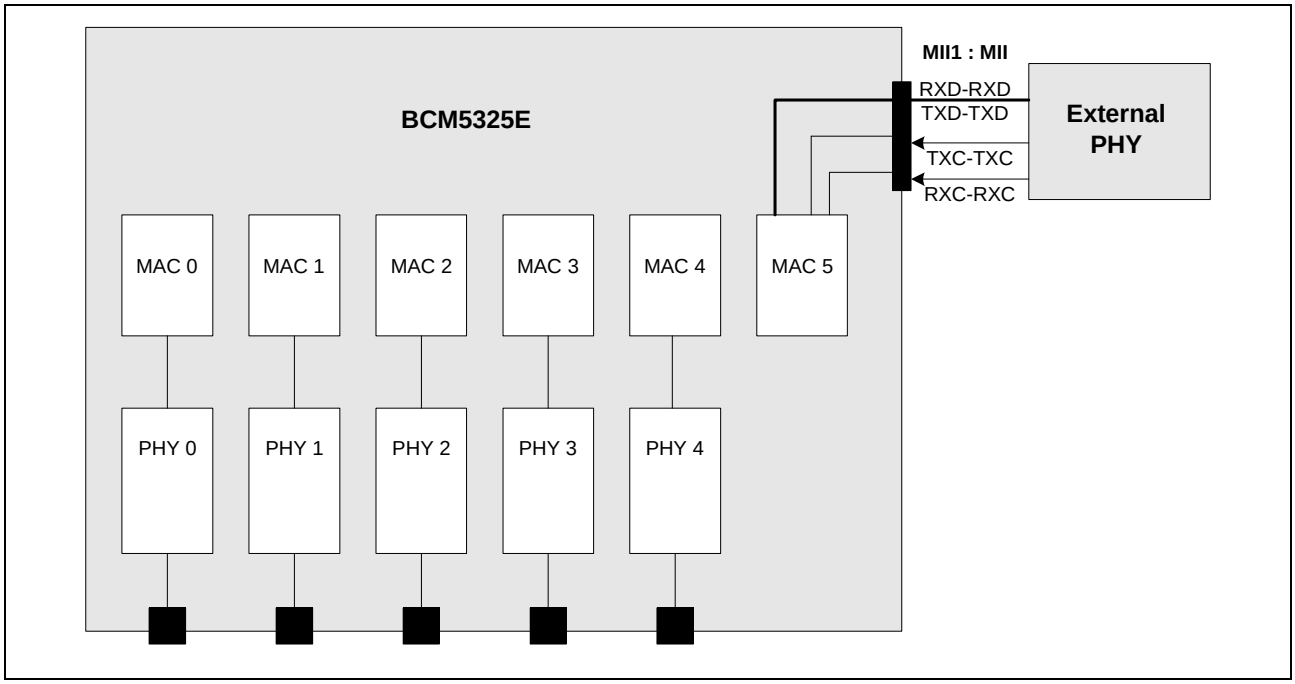


Figure 10: Normal MII Configuration

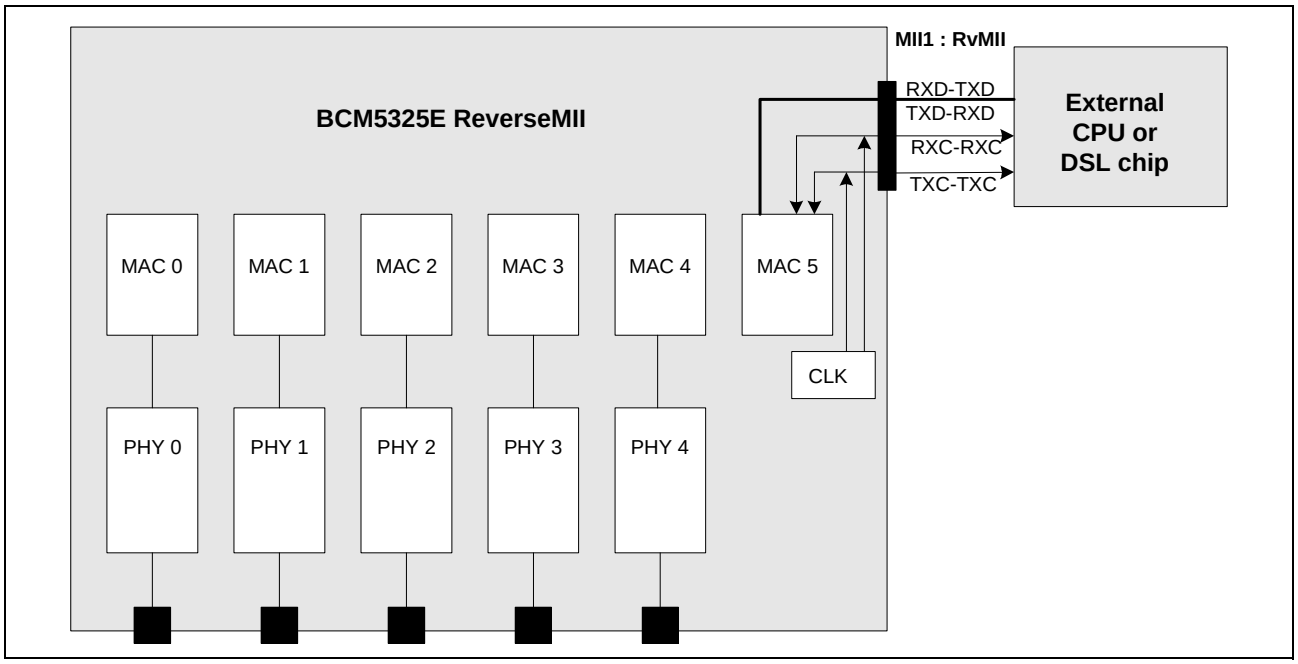
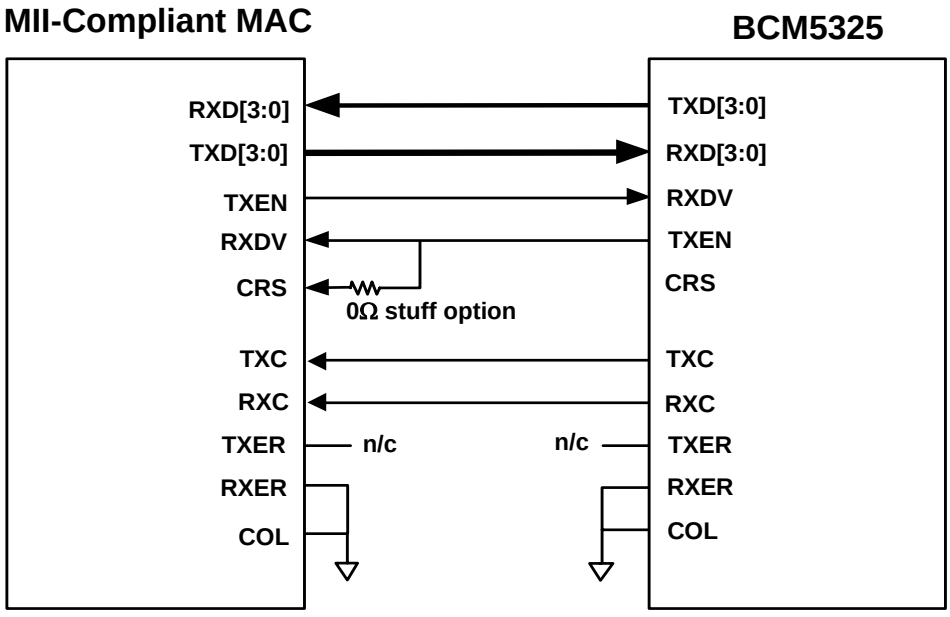


Figure 11: Reversed MII Configuration

Reverse MII mode is enabled by pulling RVMII_EN pin high or setting RvMII_EN, bit 4, of Table 43 on page 80.



BCM5325 devices support RvMII mode to connect MAC directly.

Figure 12: MAC-to-MAC MII Connection in Reverse MII Mode

PROGRAMMING INTERFACES

The BCM5325E can be programmed via the SPI Interface, the Pseudo PHY Interface or the EEPROM Interface. The SPI and EEPROM interfaces share a common pin set that is configured via the CPU_EEPROM_SEL strap pin. The "SPI Interface" on page 47 provides access for a general purpose microcontroller, allowing read and write access to the internal BCM5325E register space. It is configured to be compatible with the Motorola Serial Peripheral Interface (SPI) protocol. Alternatively, the "EEPROM Interface" on page 54 can be connected to an external EEPROM for writing register values upon power-up initialization.

The internal address space of the BCM5325E device is broken into a number of pages. Each page groups a logical set of registers associated with a specific function, for example, "Page 0x00: Control Registers" on page 76, "Page 0x01: Status Registers" on page 84, "Page 0x05: ARL Access Registers" on page 99, and so on. Each page provides a logical address space of 256 bytes, although, in general, only a small portion of the address space in each page is utilized.

All pages have the same registers from addresses 0xF0-0xFF, and all pages behave identically over this space, as shown in the "Global Registers" on page 148. Address FFh is the "Page Register" on page 148 and is accessible from any page. Writing a new binary value to these bits changes the currently accessible page. Address FEh is the "SPI Status Register" on page 148, and addresses 0xF0-0xF7 are the "SPI Data I/O Register" on page 148. These registers are used for writing and reading data to the register space.

Explanation follows for using the Serial Interface with an SPI compatible CPU ("SPI Interface" on page 47) or an EEPROM (see "EEPROM Interface" on page 54). Either mode can be selected with the strap pin, CPU_EEPROM_SEL. Either mode has access to the same register space. In addition, a description of using the Pseudo PHY Interface can be found in "Register Access through Pseudo PHY Interface" on page 55.

SPI INTERFACE

The BCM5325E can be controlled over a serial interface that is compatible with a subset of the Motorola Synchronous Serial Peripheral Interconnect (SPI) bus. The microcontroller interface consists of four signals: serial clock (SCK), slave select (SS), master-in/slave-out (MISO) and master-out/slave-in (MOSI). The BCM5325E always operates as an SPI slave device, in that it never initiates a transfer on the SPI and only responds to the read and write requests issued from a master device.

A layer of protocol is added to the basic SPI definition to facilitate transfers from the BCM5325E. This protocol establishes the definition of the first 2 bytes issued by the master to the BCM5325E slave during an SPI transfer. The first byte issued from the SPI master in any transaction is defined as a command byte, which is always followed by a register address byte, and any additional bytes are data bytes.

The SPI mode supports two different access mechanisms, normal SPI and fast SPI, determined by the content of the command byte. Figure 13 shows the normal SPI command byte, and Figure 14 shows the Fast SPI command byte. These two mechanisms should not be mixed in an implementation; the CPU should always initiate transfers consistently with only one of the two mechanisms.

0	1	1	MODE = 0	CHIP ID 2 (MSB)	CHIP ID 1	CHIP ID 0 (LSB)	Read/Write (0/1)

Figure 13: Normal SPI Command Byte

Byte Offset (MSB)	Byte Offset	Byte Offset (LSB)	MODE = 1	CHIP ID 2 (MSB)	CHIP ID 1	CHIP ID 0 (LSB)	Read/Write (0/1)

Figure 14: Fast SPI Command Byte

The MODE bit (bit 4) of the command byte determines the meaning of bits 7:5. If bit 4 is a 0, it is a normal SPI command byte, and bits 7:5 should be defined as 011b. If bit 4 is a 1, bits 7:5 indicate a fast SPI command byte, and bits 7:5 indicate the byte offset into the register that the BCM5325E starts to read from (byte offsets are not supported for write operations).

In both command bytes, bits[3:1] indicate the CHIP ID to be accessed. Because the BCM5325E operates as a single-chip system, the CHIP ID is 000. Note that the SS# signal must also be active for any BCM5325E device to recognize that it is being accessed.

Bit 0 of the command byte is the R/W signal (0 = Read, 1 = Write) and determines the transmission direction of the data.

The byte following the command byte is an 8-bit register address. Initially, this sets the page address, followed by another command byte that contains the register base address in that page, which is used as the location to store the next byte of data received in the case of a write operation, or the next address from which to retrieve data in the case of a read operation. This base address increments as each byte of data is transmitted/received, allowing a contiguous block data from a register to be stored/read in a single transmission. When the fast SPI command byte mode is used, the actual start location of a read operation can be modified by the offset contained in bits 7:5 of the command byte. Reading/writing data from/to separate registers, even if those registers are contiguous in the current page, must be performed by supplying a new command byte and register address for each register, with the address as defined in the appropriate page register map.

Non-contiguous blocks are also stored/read through the use of multiple transmissions, which allow a new command byte and register base address to be specified. The $\overline{SS}$ signal must remain low for the entire read or write transaction, as shown in Figure 15 and Figure 16, with the transaction terminated by the deassertion of the $\overline{SS}$ line by the master.

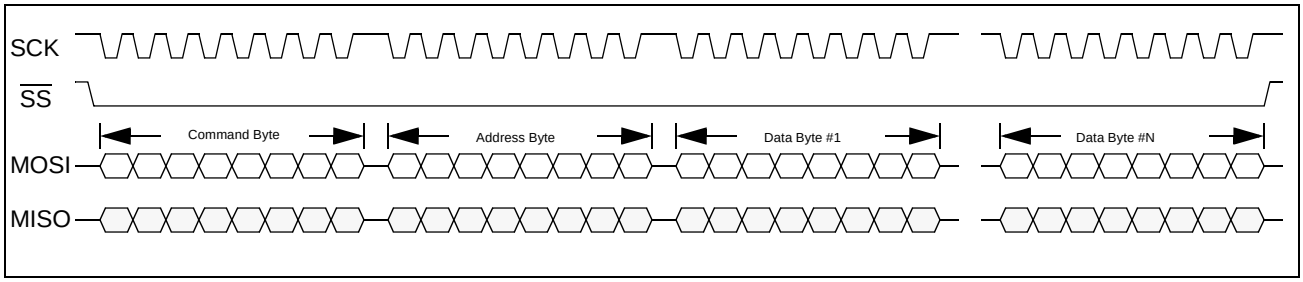


Figure 15: SPI Serial Interface Write Operation

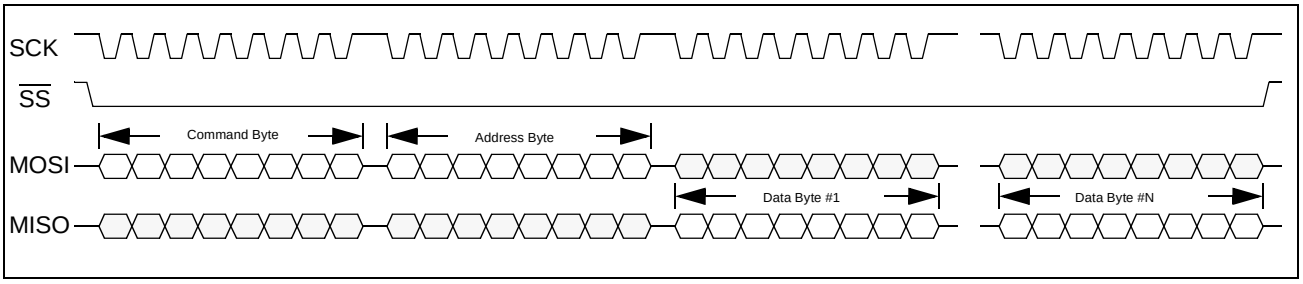


Figure 16: SPI Serial Interface Read Operation

The Serial Interface supports operation up to 2 MHz in SPI mode. A maximum of four devices can be cascaded/addressed.

Normal SPI Mode

Normal SPI mode allows single-byte read and multi-byte string write operations, with the CPU polling to monitor progress. Read operations are performed using the "SPI Status Register" on page 148 and "SPI Data I/O Register" on page 148. All read operations take the form:

```
<CMD, CHIP ID, R><REG ADDR>
```

where the first byte is the command byte with the appropriate CHIP ID and Read bits set, and the second byte is the register address.

All write operations are of the form:

```
<CMD, CHIP ID, W><REG ADDR><DATA0>...<DATAn>
```

where the first byte is the command byte with the appropriate CHIP ID and Write bits set, the second byte is the register address, and the remaining bytes are the exact number of data bytes appropriate for the selected register follow. Failure to provide the correct number of data bytes means the register write operation does not occur.

A simple flow chart for the read process is shown in Figure 17 on page 51.

To read a register, first the "Page Register" on page 148 is written (<CMD, CHIP ID, W><REG ADDR = FFh><DATA = NEW PAGE>). It is only necessary to write the page register when moving to a new page. Once in the correct page, a read operation is performed on the appropriate register (<CMD, CHIP ID, R><REG ADDR>). Once the SPI Status Register indicates that the data is available (RACK = 1), the data can be read. Data is read from the SPI Data I/O Register, located at 0xF0-0xF7on every page (so no page swap is necessary to read the data on any page). A read operation can access any or all of the bytes on a specific register, including the ability to start at any offset. For instance, reading from SPI Data I/O Register[0], reads the least significant byte of the register, and successive reads to SPI Data I/O Register[0] read the remaining bytes. However, reading the first byte from SPI Data I/O Register[2] reads the third byte of the register, and successive reads to SPI Data I/O Register[2] reads the remaining bytes of the register up to the most significant byte of the register. It is not necessary to read all bytes of a registers, only the bytes of interest. The SPI master can then move on to perform another read or write operation.

A flow chart for the write process is shown in Figure 18 on page 52. To write a register, the Page Register is written if necessary (<CMD, CHIP ID, W><REG ADDR = FFh><DATA = NEW PAGE>), then data is written to the selected register (<CMD, CHIP ID, W><REG ADDR><DATA0>...<DATAn>), where DATA0 is the least significant byte of the register, and DATAn is the most significant byte of the register, and the exact number of bytes is present as defined by the register width. No byte offset is provided for write operations, and all bytes must be present to activate the write process internal to the BCM5325E.

The following simple rules apply to the normal SPI mode:

- A write to the page register at any time causes the SPI state machine to reset.
- A read operation can access any number of bytes at any offset using the SPI Data I/O Register registers.
- A write operation must write the exact number of bytes to the register being accessed.
- The RXRDY/TXRDY flags in SPI Status Register must be checked after each 8-byte string has been read/written to ensure the next string is ready and can be accepted (since the largest internal register is 8 bytes, this restriction only applies to reading and writing frames via the SPI).

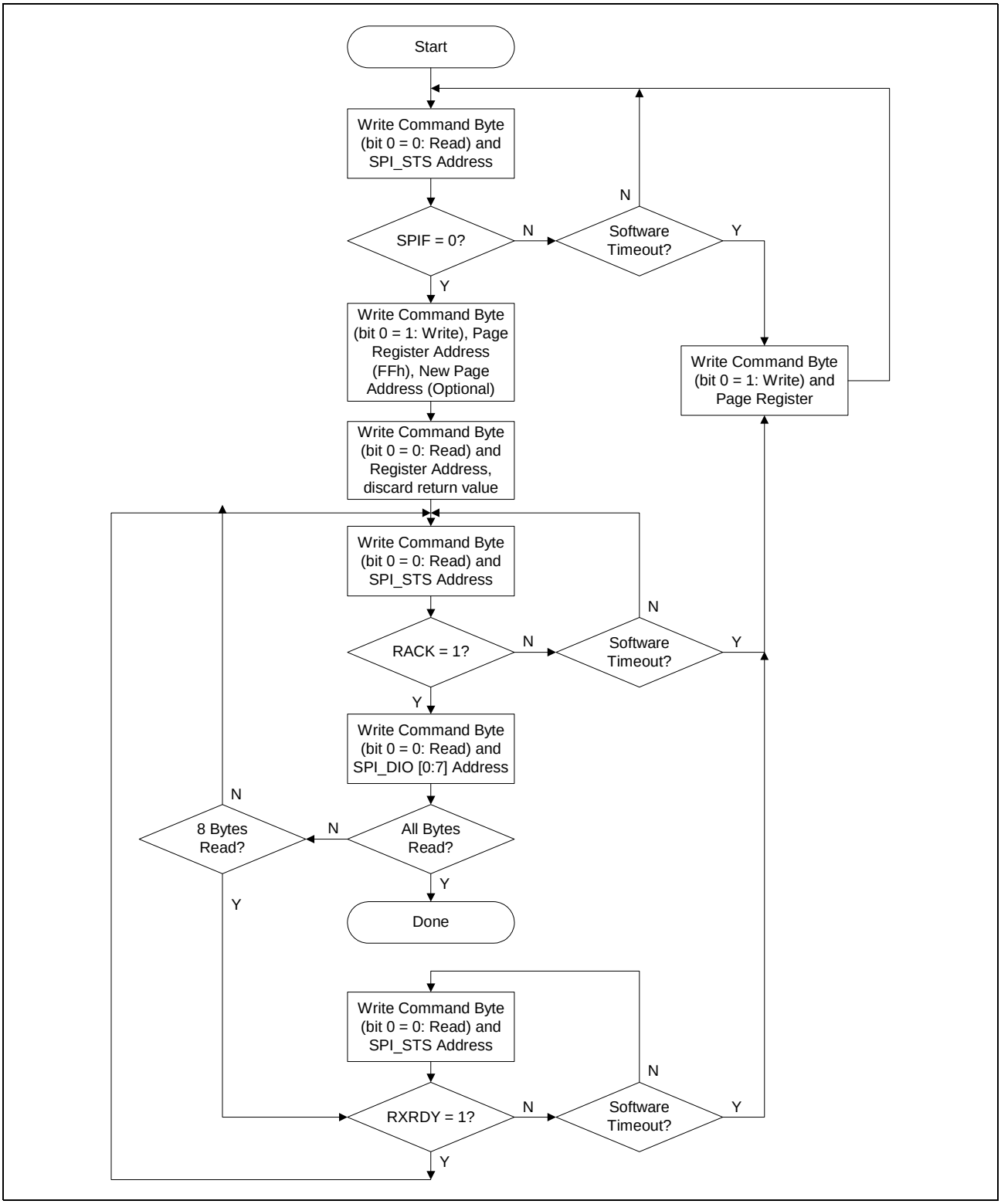


Figure 17: Normal SPI Mode Read Flow Chart

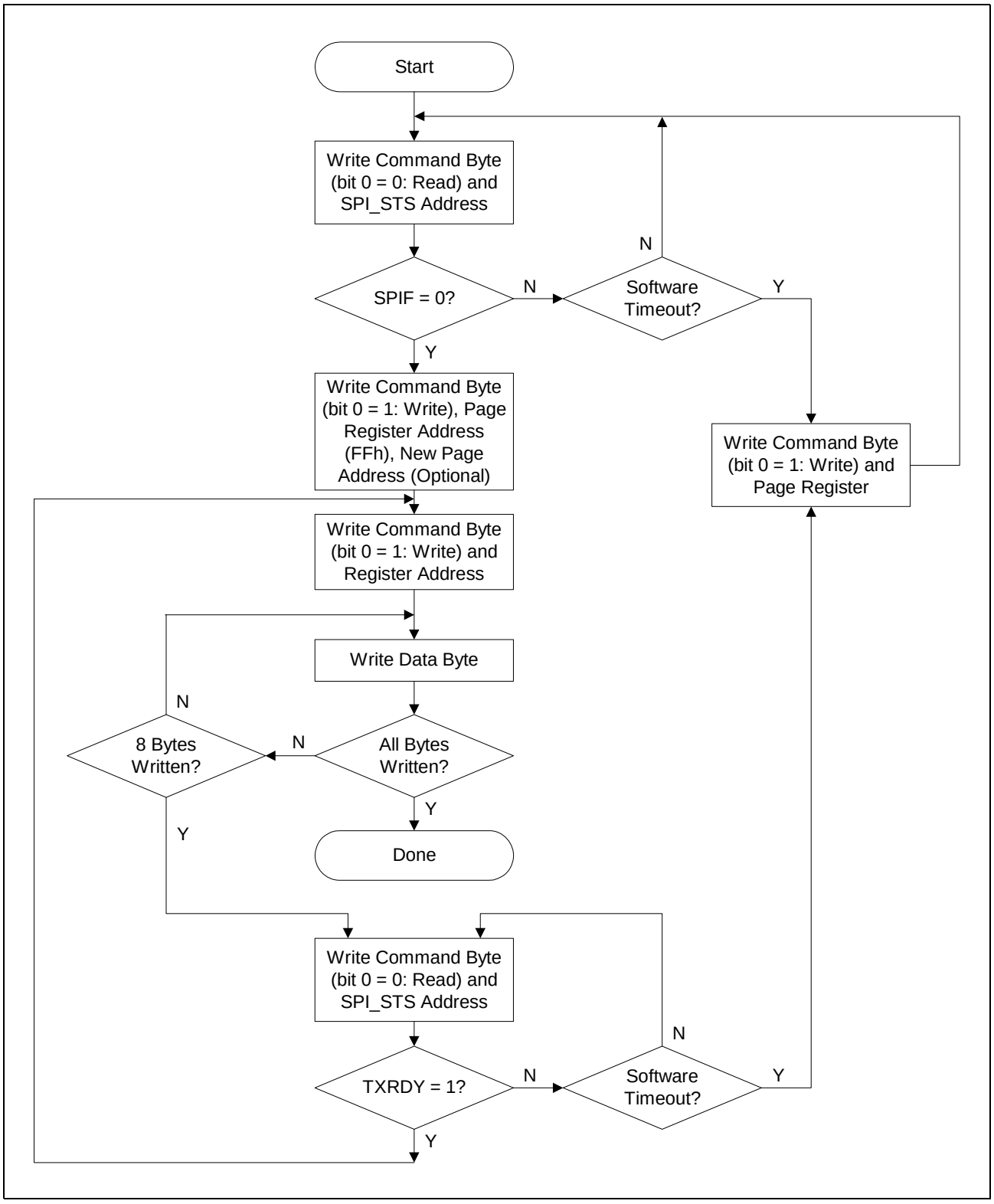


Figure 18: Normal SPI Mode Write Flow Chart

Fast SPI Mode

Fast SPI mode makes use of the fact that the SPI port is inherently full-duplex and provides an explicit acknowledge on read cycles to eliminate the polling of the SPI_STS register for RACK polling. Fast SPI mode requires the MODE bit in the command byte to be set as indicated in Figure 14 on page 48. Like normal SPI mode, fast SPI mode also supports byte offsets for read operations.

Read operations do not access the SPI Data I/O Register. Instead, status and data are output on the MISO line by the BCM5325E. Once the page register and the register within that page have been set, the master reads the MISO line state. The BCM5325E immediately puts out a byte string which indicates the state of the RACK bit in bit 0. Once bit 0 is sampled high, the next byte is the least significant byte of the read data, and successive bytes follow. Byte offset of the register is provided by using bits 7:5 of the command byte, to index from byte 0 (000) to byte 7 (111) as the first byte to be presented on MISO.

As an example, if command byte [7:0] = 011_1_001_0 that indicates a read offset of 3 (4th byte) in the register to be accessed (register 6 in this example). The RACK status bit is provided on the MISO line (00000001) when the read data (dddddddd) is to follow on the MISO line. An example of the timing is shown below.

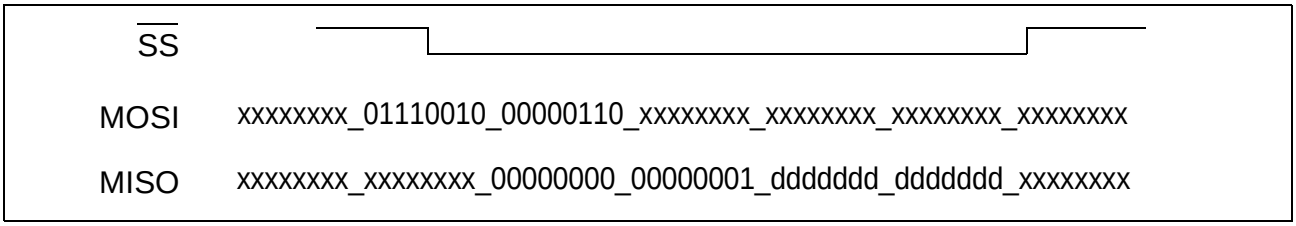


Figure 19: Timing Example

Write operations are identical in fast and normal SPI mode.

EEPROM Interface

The EEPROM interface enables the chip to download register programming instruction from an external low cost serial EEPROM, e.g., 93C46. For each programming instruction fetched from the EEPROM, the instruction is executed immediately for the particular register. A predefined magic code is expected as the first data entity (header) of the EEPROM. The EEPROM must be configured to x16 word format. The header contains a magic code and length information as shown in Table 26. The actual data stored in EEPROM is byte-swapped as shown in Table 27.

- Upper 9 bits are magic code 1AAh, which indicates valid data follows.
- Bit 6 is for speed indication. A 0 means normal speed. A 1 indicates speed up. Default is 0.
- Lower 6 bits indicate the total length of all entries. Only up to 64 words are allowed.

Table 26: EEPROM Header Format

15:8	***7***	***6***	***5:0***
Magic code (0xAA)	Magic code (1)	Speed	Total Entry Number

Table 27: EEPROM Contents

7	***6***	***5:0***	***15:8***
Magic code (1)	Speed	Total Entry Number	Magic code (0xAA)

After chip initialization, the header is read from the EEPROM and used to compare to the pre-defined magic code. When the fetched data does not match the predefined magic code, the EEPROM instruction fetch process is stopped. If the magic code is matched, fetching instructions continues until the instruction length as defined in the HEADER.

The following figure shows an EEPROM programming example.

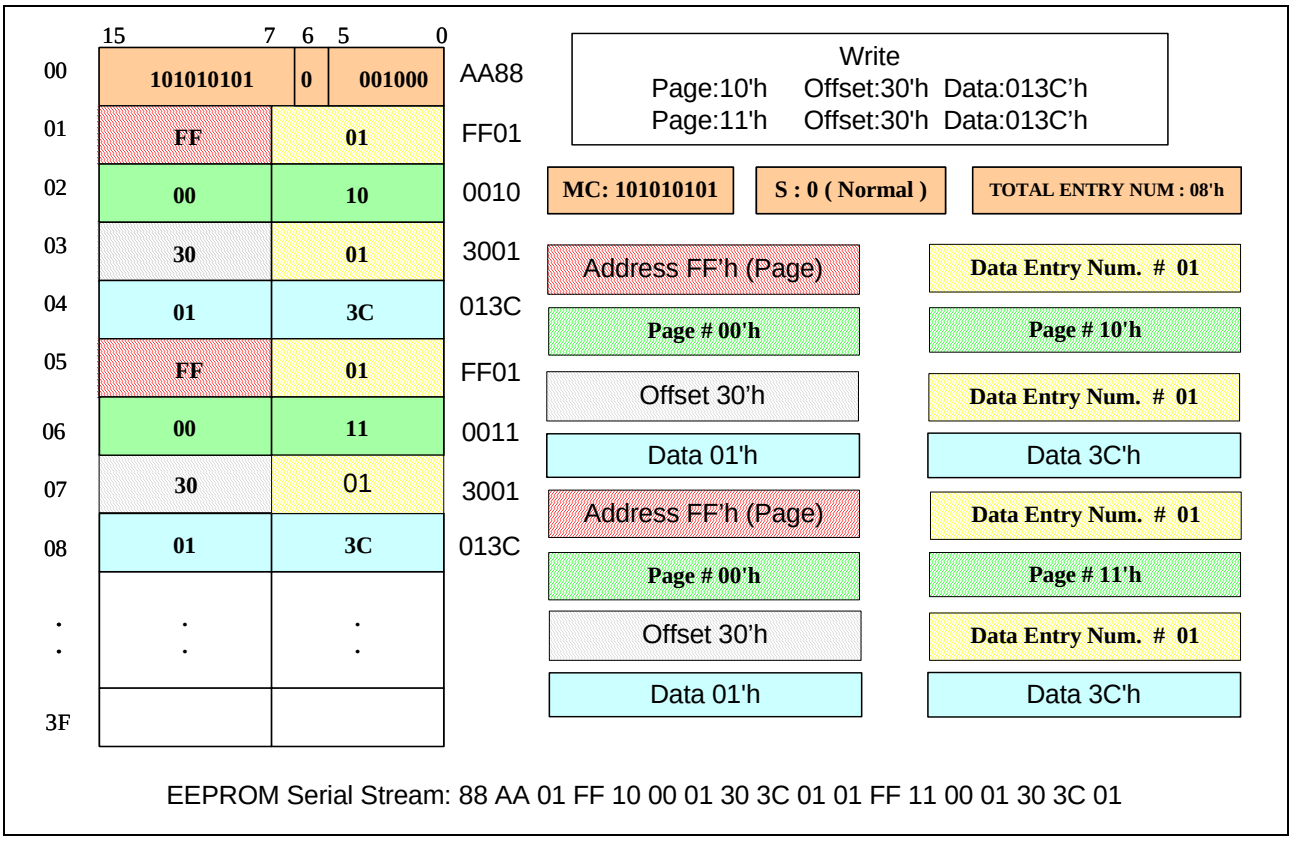


Figure 20: EEPROM Programming Example

The EEPROM Port shares the same pin with the SPI port. Either the SPI port or the EEPROM can be selected by using the CPU_EEPROM_SEL strap pin. The register space for the EEPROM port is the same as for the SPI port.

REGISTER ACCESS THROUGH PSEUDO PHY INTERFACE

As an alternative to the SPI interface, the complete BCM5325E register set can be accessed through the MDC/MDIO interface from the CPU MII port (or general purpose I/O). Within the BCM5325E, the MDC/CDIO interface is connected to the switches SPI interface logic, so that whatever is accessible via SPI is accessible via the BCM5325E MDC/MDIO pins. As long as there is no SPI clock driving the BCM5325E, the MDC/MDIO pins will revert to this mode of operation. MDC pin becomes input. The switch register space is organized into pages, each contains a certain set of registers. To access the switch register, both the page number and the register address need to be specified.

The switch registers are accessed through a pseudo PHY (PHY Address = 0x1E, which is not used by any of the physical PHYs on BCM5325E) MDC/MDIO path. The algorithm for read access to the switch registers is shown in Figure 21 on page 56. The algorithm for write access is shown in Figure 22 on page 57. Pseudo PHY MDC/MDIO interface has an addressing space of 32 as shown in Figure 23 on page 58. The first 16 registers are reserved by IEEE. Only addresses 16 to 32 can be used to access the switch registers. The MDC/MDIO registers used to access the switch registers are defined

in Table 28 on page 59. The switch register page number, register address, and access type are determined by register 16 and 17. The data read from a switch register or written to a switch register are stored in registers 24 to 27 (64 bits total).

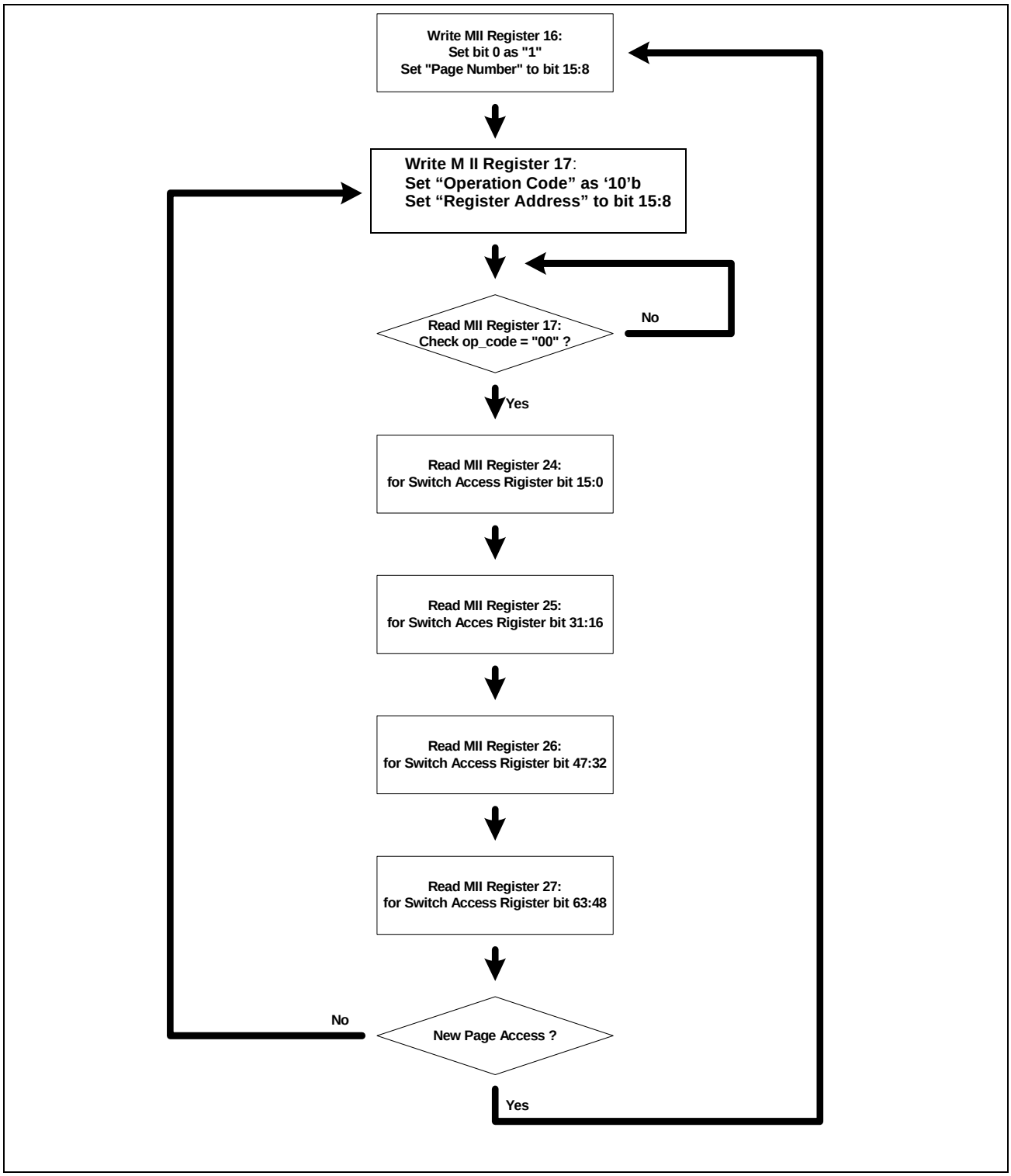


Figure 21: Read Access to Switch Register Set via Pseudo PHY (Phyad = 11110) MDC/MDIO Path

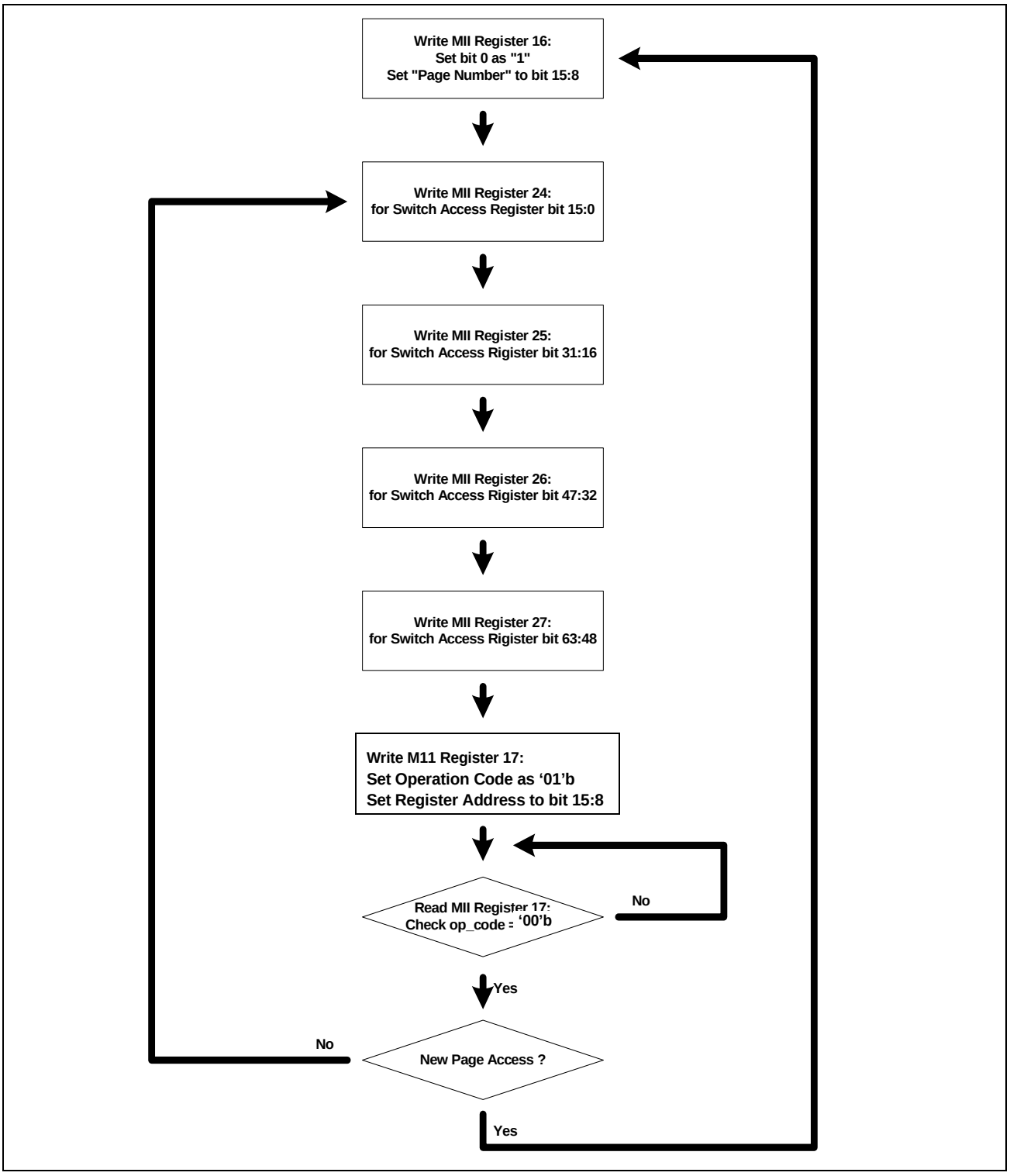


Figure 22: Write Access to Switch Register Set via Pseudo PHY (Phyad = 11110) MDC/MDIO Path

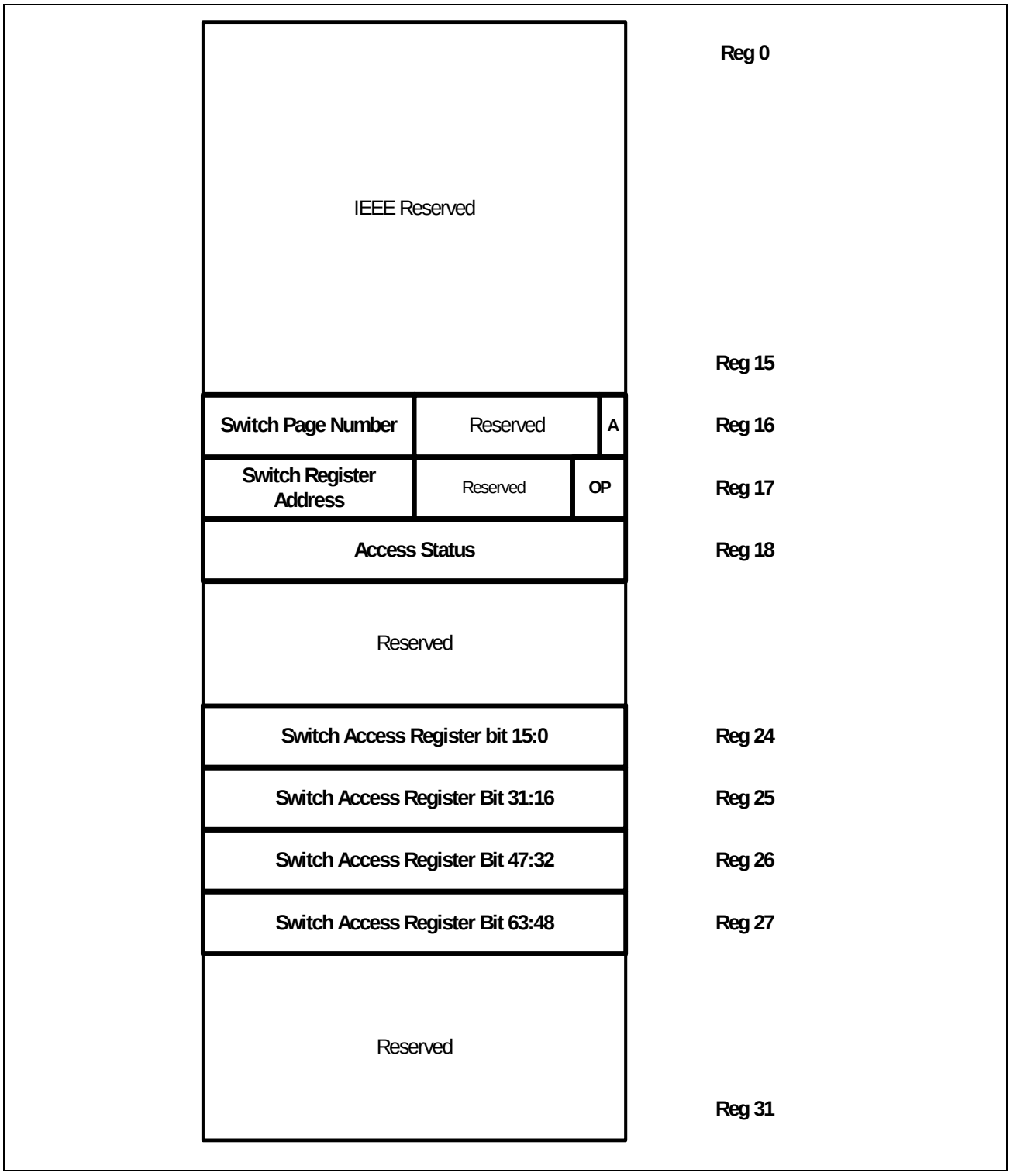


Figure 23: Pseudo PHY MII Register Map

Table 28: Pseudo PHY MII Register Definitions

Bits	*R/W*	*Description*
Register 16 (0x10)—Switch Register Set Access Control Register		
15:8	R/W	Switch Page Number
7:1	RSVD	Reserved
0	R/W	Switch Register Set MDC/MDIO Access Enable
Register 17 (0x11)—Switch Register Set Read/Write Control Register		
15:8	R/W	Switch Register Address
7:2	RSVD	Reserved
1:0	RW/SC	Op Code: • 00 = No Operation • 01 = Write Operation • 10 = Read Operation • 11 = Reserved
Register18 (0x12)—Switch Register Access Status Register		
15:2	RSVD	Reserved
1	RO/LH	Operation Error. This bit is set to show operation error when Op Code is 11.
0	RO/LH	Prohibit Access
Register 24 (0x18)—Switch Access Register		
15:0	R/W	Switch Access Register bits 15:0
Register 25 (0x19)—Switch Access Register		
31:16	R/W	Switch Access Register bits 31:16
Register 26 (0x1a)—Switch Access Register		
47:32	R/W	Switch Access Register bits 47:32
Register 27 (0x1b)—Switch Access Register		
63:48	R/W	Switch Access Register bits 63:48

MII MANAGEMENT (MDC/MDIO)

PHY ADDRESS

If the SPI interface is active, the MDC/MDIO pins have no access to the new BCM5325X status and configuration registers, nor do they allow the additional MII port to be configured or monitored. These functions must be provided via the SPI interface.

Each transceiver in the BCM5325E has a unique PHY address for MII management. The addresses are set through the PHY address pins. The pins are latched at the trailing end of reset. Transceiver 1 have the address yz000'b, where yz = 00'b. Transceivers 2-4 have addresses yz001'b through yz011'b, respectively.

Every time an MII write or read operation is executed, the transceiver compares the PHY address with its own PHY address definition. The operation is executed only when the addresses match.

REGISTER PROGRAMMING

Using MDC/MDIO for this mode only applies when the SPI interface is disabled. The BCM5325E fully complies with the IEEE 802.3u Media Independent Interface (MII) specification. The MII management interface registers of each port are serially written-to and read-from using a common set of MDIO and MDC pins. A single clock waveform must be provided to the BCM5325E at a rate up to 12.5 MHz through the MDC pin. The serial data is communicated on the MDIO pin. Every MDIO bit must have the same period as the MDC clock. The MDIO bits are latched on the rising edge of the MDC clock. MDC may be stopped between frames provided no timing requirements are violated. MDC must be active during each valid bit of every frame, including all preamble, instruction, address, data, and at least one idle bit. Every MII read or write instruction frame contains the fields summarized in Table 29.

When writing to the MDIO pin, the bit value must be stable for 10 ns before the rising edge of the MDC, and must be held valid for 10 ns after the rising edge of the MDC. When reading from the MDIO pin, the data bit is valid at the rising edge of the MDC until the next falling edge of the MDC.

Table 29: MII Management Frame Format

Operation	*PRE*	*ST*	*OP*	*PHYAD*	*REGAD*	*TA*	*Data*	*Direction*
Read	1... 1	01	10	AAAAA	RRRRR	ZZ	Z... Z	Driven to BCM5325E
						Z0	D... D	Driven by BCM5325E
Write	1... 1	01	01	AAAAA	RRRRR	10	D... D	Driven to BCM5325E

Example: To put a PHY with address 00001 into Loopback mode, issue the following write MII instruction:

```
1111 1111 1111 1111 1111 1111 1111 1111     0101 00001 00000 10 0100 0000 0000 0000
```

To determine if a PHY is in the link pass state, issue the following read MII instruction:

```
1111 1111 1111 1111 1111 1111 1111 1111     0110 00001 00001 ZZ ZZZZ ZZZZ ZZZZ ZZZZ
```

The External PHY drives the MDIO line during the last 17 bit times. If the link status is good, the third bit from the end (bit 2) is 1.

Table 30: MII Read And Write Instruction Contents

Content	*ID*	*Definition*
Preamble	PRE	To signal the beginning of an MII instruction after reset, at least 32 consecutive 1 bits must be written to the MDIO pin of the BCM5325E. A preamble of 32 1 bits is required only for the first read or write following reset. If bit 6 of MII register 0x01 is cleared, a preamble is always required. A preamble of fewer than 32 1 bits causes the remainder of the instruction to be ignored.
Start of Frame	ST	A 01 pattern indicates that the start of the instruction follows.
Operation Code	OP	A read instruction is indicated by 10, while a write instruction is indicated by 01.
PHY Address	PHYAD	A 5-bit PHY address follows, with the MSB transmitted first. The PHY address allows a single MDIO bus to access multiple PHY chips.
Register Address	REGAD	A 5-bit register address follows, with the MSB transmitted first. The addresses for the registers used by the BCM5325E are shown in Table 29 on page 60.
Turnaround	TA	The next bit times are used to avoid contention on the MDIO pin when a read operation is performed. When a write operation is being performed, 10 must be sent to the BCM5325E chip during these two bit times. When a read operation is being performed, the MDIO pin of the MAC must be put in a high-impedance state during these bit times. The BCM5325E transceiver drives the MDIO pin to 0 during the second bit time.
Data	–	The last 16 bits of the Instruction are the actual data bits. During a write operation, these bits are written to the MDIO pin with the most significant bit (MSB) transmitted first. During a read operation, the data bits are driven by the BCM5325E with the MSB transmitted first.

LED INTERFACES

The BCM5325E provides visibility per port of link status, port speed, duplex mode, combined transmit and receive activity, and collision. Both a parallel and serial interface are supplied to drive the status to the LEDs. The parallel interface provides the lowest cost solution for implementing LEDs. The serial interface provides up to five status indications per port; whereas, the parallel interface indicates only up to three. Combinations of serial and parallel status can also be effective in lowering the system cost.

During power-on and reset, the parallel LED signals are driven low and the serial interface shifts a continuous low value for 1.34s.

Note: When MAC4 and MAC5 are connected to the MII interface, LED will reflect the activities, and status of the MACs from External PHY Autoneg registers.

PARALLEL LED INTERFACE

Three pins per port, including the MII port, are provided for directly driving LED status: $\overline{\text{LEDA}}$, $\overline{\text{LEDB}}$, $\overline{\text{LEDC}}$. The LED mode configuration signals control the LED status type driven by each pin. Table 31: “LED Status Types,” on page 64 describes the selectable status types and Table 32: “LED Mode Matrix,” on page 64 gives a complete LED mode matrix for parallel interface.

SERIAL LED INTERFACE

A two pin serial interface, LEDDATA and LEDCLK, provides data and clock to enable external shift registers to capture the LED status indications from the BCM5325E for each internal port. The status encapsulated within the shift sequence is configured by the LED mode configuration signals. The configuration signals select both the number of status bits per port and the status type of each bit. The serial interface also provides an 8-bit value indicating the percentage of total bandwidth used by the switch.

The LEDCLK is generated by dividing the 25-MHz input clock by 16, providing a 640 ns clock period. The LEDDATA outputs are generated on the falling edge of the LEDCLK, and have adequate setup and hold time to be clock externally on the rising edge of LEDCLK. The shift sequence is a consecutive stream of 8-bit status words. The first word of the sequence is the LOAD status, followed by optional port status words. Each 8-bit port status word contains one bit for each port of the designated LED status type. The words are shifted MSB first. For a port status word, the MSB corresponds to port 4. The shift sequence is repeated every 42 ms.

Refer to Figure 24 on page 62 for an illustration of the serial LED shift sequence, Table 31 on page 64 for LED status Type, and Table 32 on page 64 for LED mode matrix.

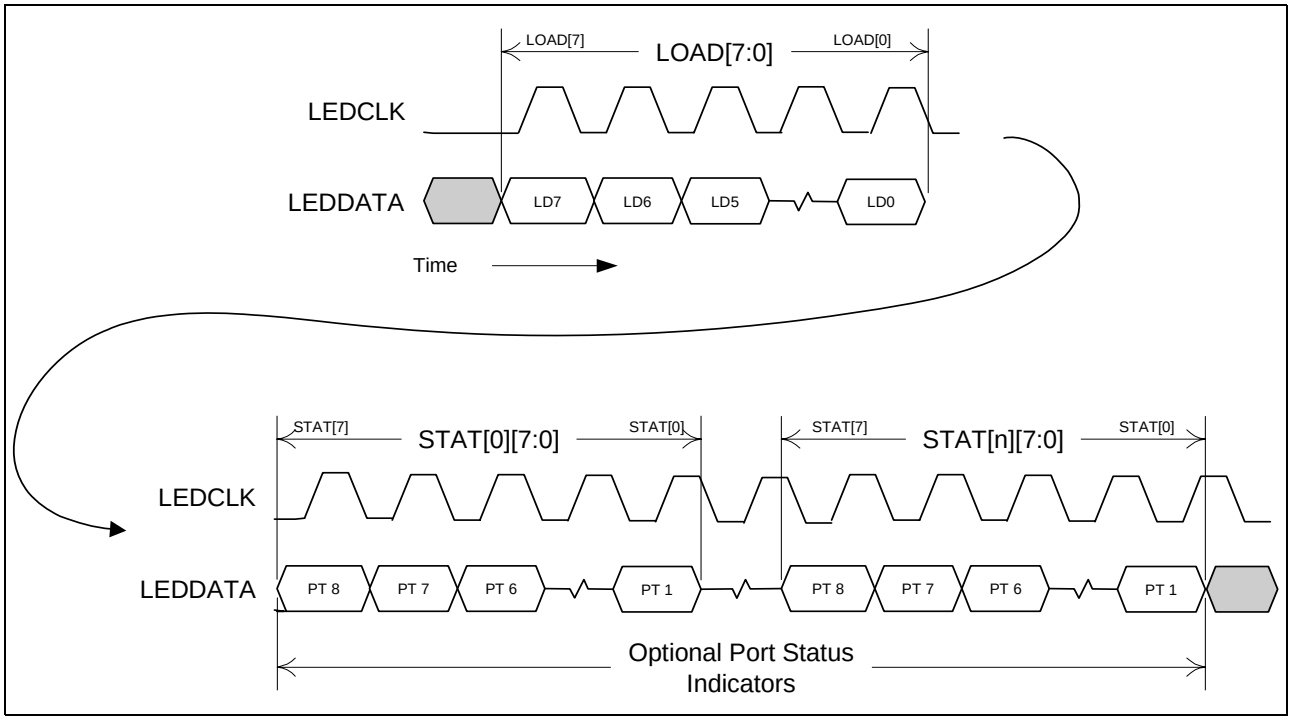


Figure 24: Serial LED Shift Sequence

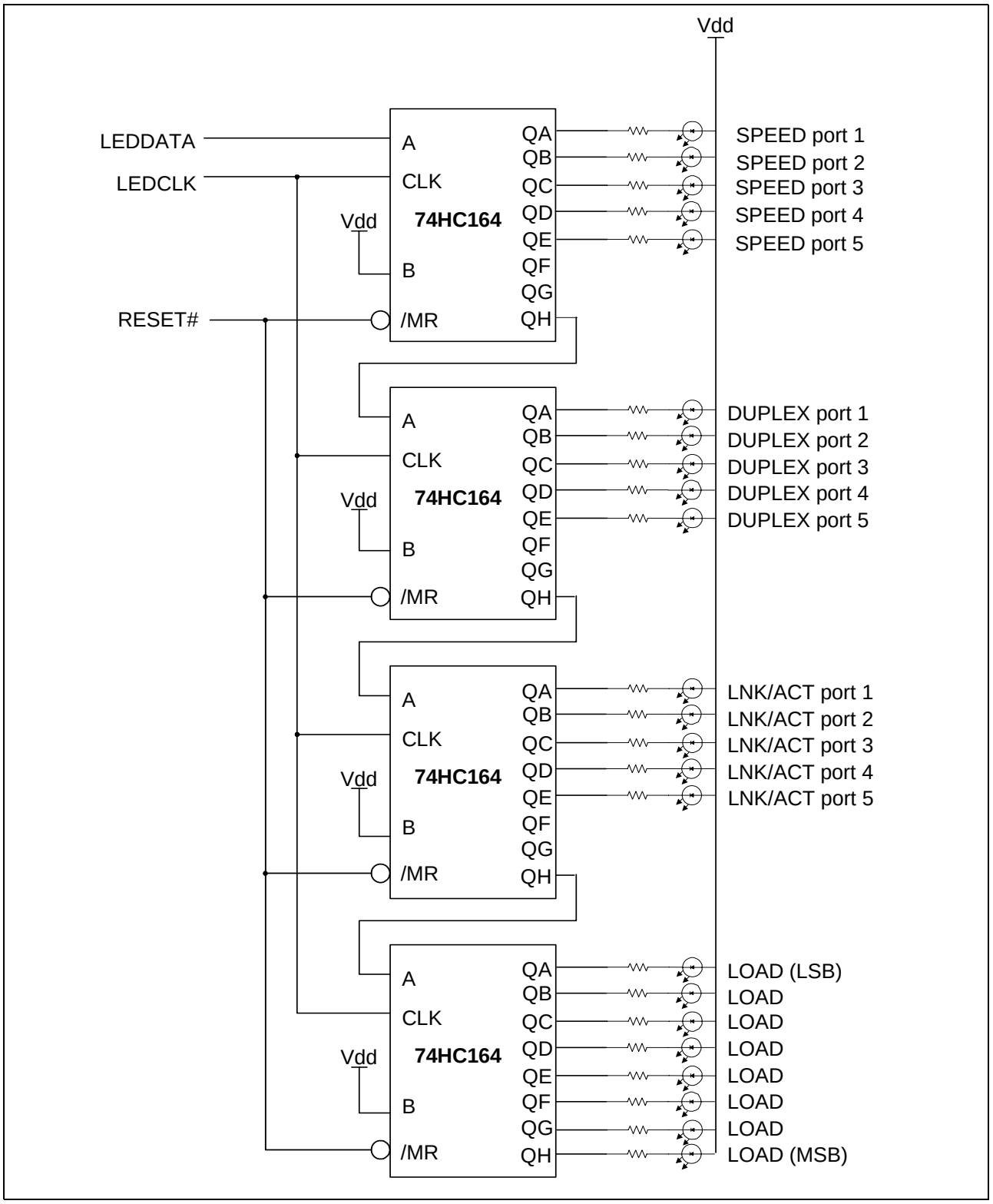


Figure 25: Example Circuit for Serial LED Mode

Table 31: LED Status Types

Name	*Description*
LOAD	Bandwidth utilization meter. An 8-bit value indicating the percentage of total bandwidth of the switch utilized over a 42-ms interval for packet data.
LNK/ACT	Link and activity status indicator. Low when link is established, blinking at 12 Hz when link is up and the port is transmitting and receiving.
LNK/ACT/SPD	Link, activity, and speed indicator. Active when link is up, blinking at 3 Hz when port is transmitting or receiving in 10-MB mode, and blinking at 12 Hz when the port is transmitting or receiving in 100-MB mode.
LNK	Link status indicator. Low when link is established and high when link is off.
DUPLEX	Duplex mode indicator. High for half-duplex or no link and low for full-duplex and link.
SPEED	Speed indicator. High for 10 Mbps or no link and low for 100 Mbps and link.
ACT	Activity. Low for 42 ms when transmit or receive activity is detected during previous 42-ms interval, and high during no activity or no link.
COLSN	Collision. Low for 42 ms when collision is detected during the previous 42-ms interval, and high in the absence of collisions or no link.
$\overline{\text{LEDERR}}$	Error indication. Internal memory fails self test during power-on reset. Low if failure occurs.

Table 32: LED Mode Matrix

LEDMode[2:0]	*LEDA*	*LEDB*	*LEDC*	*Shift Sequence*
000	LNK/ACT	DUPLEX	SPEED	RESVD (1 bit) $\overline{\text{LEDERR}}$ (1 bit) $\overline{\text{LOAD}}$ (8 bits) LNK/ACT (8 bits) DUPLEX (8 bits) SPEED (8 bits)
001	LNK/ACT/SPD	DUPLEX	–	RESVD (1 bit) $\overline{\text{LEDERR}}$ (1 bit) $\overline{\text{LOAD}}$ (8 bits) LNK/ACT/SPD (8 bits) DUPLEX (8 bits)
010	LNK	ACT	SPEED	RESVD (1 bit) $\overline{\text{LEDERR}}$ (1 bit) $\overline{\text{LOAD}}$ (8 bits) LINK (8 bits) ACTIVITY (8 bits) SPEED (8 bits) DUPLEX (8 bits)

Table 32: LED Mode Matrix (Cont.)

LEDMode[2:0]	*LEDA*	*LEDB*	*LEDC*	*Shift Sequence*
100	LNK/ACT	DUPLEX	SPEED	RESVD (1 bit) $\overline{\text{LEDERR}}$ (1 bit) $\overline{\text{LOAD}}$ (8 bits) LNK/ACT (8 bits) DUPLEX (8 bits) SPEED (8 bits) COLSN (8 bits)
101	LNK/ACT/SPD	DUPLEX	COLSN	RESVD (1 bit) $\overline{\text{LEDERR}}$ (1 bit) $\overline{\text{LOAD}}$ (8 bits) LNK/ACT/SPD (8 bits) DUPLEX (8 bits) COLSN (8 bits)
110	LNK	ACT	SPEED	RESVD (1 bit) $\overline{\text{LEDERR}}$ (1 bit) $\overline{\text{LOAD}}$ (8 bits) DUPLEX (8 bits) COLLISION (8 bits)

LOAD METER LED

The load meter LEDs provide a bar-graph indication of the percentage of total available bandwidth of the switch utilized by packet data over a periodic interval of 42 ms. The following table shows the bar-graph scale.

Table 33: Load Meter LED Decode

Load Value Load[7:0]	*Number of On LEDs*	*Bandwidth (%)*
11111111	0	<0.4 (all LEDs off)
11111110	1	less than 0.8
11111100	2	less than 1.6
11111000	3	less than 3.2
11110000	4	less than 6.4
11100000	5	less than 12.8
11000000	6	less than 25
10000000	7	less than 50
00000000	8	>50 (all LEDs on)

Section 5: Hardware Signal Definitions

The following table lists the conventions are used to identify the I/O types.

Table 34: I/O Signal Type Definitions

Type	*Description*	*Type*	*Description*
I	Input	O	Output
I/O	Bi-directional	O_{OD}	Open drain output
I_{PD}	Input with internal pulldown	O_{ODPM}	Open drain power management output
I_{PU}	Input with internal pullup	O_{3S}	Tri-stated signal
I_S	Input with Schmidt Trigger	B	Bias
GND	Ground	A	Analog
PWR	Power supply	$\overline{\text{OVERLINE}}$	Active low signal

Pin number in *Italic* font indicates pin is shared with multiple functions.

Configuration of the BCM5325E takes place during reset by loading device control values from hardware strapping pins. Some of the strapping pin are I/O pins and have secondary function during normal device operation. They should be configured with external pull-up or pull-down resistors. The strapping value is loaded during the reset sequence and the I/O pin returns to output operation after the completion of reset. Installing a pull-up or pull-down resistor to these pins other than the intended default value can have adverse affect on the function of the device.

Table 35: Signal Description

Signal Name	*Pin Number*	*Type*	*Description*
Media Connections			
RD5+/-	92/91	I/O_A	**Receive Pair.** Differential data from the media is received on the RD± signal pair.
RD4+/-	85/86		
RD3+/-	80/79		
RD2+/-	73/74		
RD1+/-	68/67		
TD5+/-	94/93	I/O_A	**Transmit Pair.** Differential data is transmitted to the media on the TD± signal pair.
TD4+/-	83/84		
TD3+/-	82/81		
TD2+/-	71/72		
TD1+/-	70/69		

Table 35: Signal Description (Cont.)

Signal Name	*Pin Number*	*Type*	*Description*
Clock/Reset			
XTALI/CK25	61	I	**25-MHz Crystal/Clock Input.** For a single-ended clock signal input, connect a 25-MHz (+/- 50 ppm) reference clock to the XTALI/CK25 pin. This pin must be driven with a continuous clock. Leave XTALO unconnected for this mode of operation. Alternatively, a 25-MHz parallel-resonant crystal can be connected between the XTALI and XTALO pins, with a 27-pF capacitor from each pin to GND. ***Note:*** This mode should only be used in a non-expanded system.
XTALO	62	O	
$\overline{\text{RESET}}$	128	I_S	**Reset.** Active Low. Resets the BCM5325E.
MII Port			
TXC	19	I/O_{PD}	**Transmit Clock.** For MII mode, 25-MHz input in 100BASE-X mode and 2.5 MHz in 10BASE-T mode. This clock must be a continuously driven input, generated from the PHY.
TXD[3]	*12*	I/O_{PD}	**Transmit Data Output.** Nibble-wide transmit data is output on these pins synchronously to TXC. TXD[3] is the most significant bit.
TXD[2]	*13*		
TXD[1]	*14*		
TXD[0]	17		
TXEN	18	I/O_{PU}	**Transmit Enable.** Indicates that the data nibble is valid on TXD[3:0].
TXER	20	I/O_{PD}	**Transmit Error.** Asserted while TXEN is active forces a transmission of invalid data code.
RXC	26	I/O_{PD}	**Receive Clock.** 25-MHz input in 100BASE-X mode and 2.5-MHz input in 10BASE-T mode. RXC needs to be continuously running. RXC may have an irregular period when RXDV = 0 at the beginning of a packet.
RXD[3]	34	I_{PD}	**Receive Data Inputs.** Nibble-wide receive data. RXD[3] is the most significant bit.
RXD[2]	33		
RXD[1]	31		
RXD[0]	30		
RXDV	29	I_{PD}	**Receive Data Valid.** Active high. RX_DV indicates that a receive frame is in progress, and the data present on the RXD output pins is valid.
RXER	25	I_{PD}	**Receive Error Detected.** Active high. Indicates that there has been an error for a received frame.
CRS	24	I_{PD}	**Carrier Sense.** Active high. Indicates receive activity on link.
COL	11	I/O_{PD}	**Collision Detect.** In half-duplex mode, active high input indicates that a collision has occurred. In full-duplex mode, COL remains low. COL is an asynchronous input signal.
Serial MII Interface			
MDIO	1	I/O_{PU}	**Management Data I/O.** This serial input/output bit is used to read from and write to the MII registers of the internal transceivers. The input data value on the MDIO pin is valid and latched on the rising edge of MDC.

Table 35: Signal Description (Cont.)

Signal Name	Pin Number	Type	Description
MDC	2	I/O_{PU}	**Management Data Clock.** MDC must be provided to the BCM5325E as an input to allow MII management functions. Clock frequencies up to 12.5 MHz are supported. If the BCM5325E detects SCK activity on the SPI interface, the BCM5325E sources a 2.5-MHz clock to the external PHY device.
$\overline{\text{LINK}}$	23	I_{PU}	**Link Status Indicator.** Active low indication of the link status of the transceiver connected at the MII port. When low, the link pass condition is indicated.
Bias			
RDAC	57	B	**DAC Bias Resistor.** Adjusts the drive level of the transmit DAC. A 1.24-kΩ 1% precision resistor must be connected between the RDAC pin and GND.
LEDs			
$\overline{\text{LED5A}}$ $\overline{\text{LED5B}}$ $\overline{\text{LED5C}}$ $\overline{\text{LED4A}}$ $\overline{\text{LED4B}}$ $\overline{\text{LED4C}}$ $\overline{\text{LED3A}}$ $\overline{\text{LED3B}}$ $\overline{\text{LED3C}}$ $\overline{\text{LED2A}}$ $\overline{\text{LED2B}}$ $\overline{\text{LED2C}}$ $\overline{\text{LED1A}}$ $\overline{\text{LED1B}}$ $\overline{\text{LED1C}}$	123 124 125 118 119 122 113 116 117 110 111 112 105 106 107	O	**Per Port LED Indicators.** See Table 32 on page 64 and Table 31 on page 64 for a functional description of these signals.
LEDCLK	*126*	I/O_{PD}	**LED Shift Clock**. Periodically active to enable the shift of LEDDATA into external registers. *Shared with LEDMODE[0].*
LEDDATA	*127*	I/O_{PD}	**LED Data Output.** Serial LED data is shifted out when LEDCLK is active. See Table 32 on page 64 and Table 31 on page 64 for a functional description of these signals. *Share with LEDMODE[1].*

Table 35: Signal Description (Cont.)

Signal Name	Pin Number	Type	Description
Serial Port Interface			
SCK	*7*	I/O_{PU}	**Serial Clock.** Clock input to the Serial Port Interface supplied by the SPI master. Supports up to 2 MHz. *Share with EEPROM's SCK.*
$\overline{SS}$	*8*	I/O_{PU}	**Slave Select.** Active low signal which enables a Serial Port Interface Read or Write operation. *Share with EEPROM's CS.*
MOSI	*6*	I/O_{PU}	**Master-Out/Slave-In.** Input signal which receives control and address information for the Serial Port Interface, as well as serial data during Write operations. *Share with EEPROM's DI.*
MISO	*5*	I/O_{PU}	**Master-In/Slave-Out.** Output signal from the BCM5325E driven with serial data during a Serial Port Interface Read operation. *Share with EEPROM's DO.*
EEPROM Interface			
SCK	*7*	I/O_{PU}	**Serial Data Clock.** Clock output to the EEPROM supplied by the BCM5325E. *Share with Serial Port Interface's SCK pin.*
CS	*8*	I/O_{PU}	**Chip Select.** Active high signal which enables an EEPROM read operation. Share with $\overline{SS}$ pin.
DO	*5*	I/O_{PU}	**Data Out.** Serial data output from the external EEPROM. *Share with MISO pin.*
DI	*6*	I/O_{PU}	**Data In.** Serial data input to the external EEPROM. *Share with MOSI pin.*
Configuration			
FREQ[1] FREQ[0]	37 36	I/O_{PD}	**Clock Frequency Select.** Selects internal operational clock speed. • FREQ[1:0] = 00: 50 MHz (Default for non-managed operation) • FREQ[1:0] = 01: 50 MHz • FREQ[1:0] = 10: 66 MHz (Default for managed operation) • FREQ[1:0] = 11: Reserved
ENFDXFLOW	100	I/O_{PU}	**Enable Automatic Full Duplex Flow Control.** In combination with the results of auto-negotiation, sets the flow control mode. See Table 21 on page 34 for more information.
ENHDXFLOW	101	I/O_{PU}	**Enable Automatic Backpressure** • ENHDXFLOW = 0: Half-duplex flow control is disabled. • ENHDXFLOW = 1: Half-duplex flow control is enabled. See Table 21 on page 34 for more information.

Table 35: Signal Description (Cont.)

Signal Name	Pin Number	Type	Description
HW_FWDG_EN	40	I_{PU}	**Forwarding Enable** • HW_FWDG_EN = 0: Frame forwarding is disabled at power-up. Typically implemented to support compliant IEEE 802.1 Spanning Tree Protocol in a managed application. • HW_FWDG_EN = 1: Frame forwarding is enabled (typical for unmanaged applications).
LEDMODE[2] LEDMODE[1] LEDMODE[0]	99 *127* *126*	I/O_{PU} I/O_{PD} I/O_{PD}	**LED Mode.** See Table 32 on page 64 for details. *LEDMODE[0] share with LEDCLK.* *LEDMODE[1] share with LEDDATA.*
MDIX_DIS	49	I_{PD}	**Auto-MDIX Disable** • MDIX_DIS = 0: Automatic TX cable swap detection is enabled. • MDIX_DIS = 1: Automatic TX cable swap detection is disabled.
$\overline{\text{MII\_FDX}}$	97	I/O_{PD}	**MII Duplex Operation** Sets the duplex setting of the MII port. Can be overridden by software through the MII Port State Override Register. • $\overline{\text{MII\_FDX}}$ = 1: MII port operates in half-duplex. • $\overline{\text{MII\_FDX}}$ = 0: MII port operates in full-duplex.
$\overline{\text{MII\_SPD100}}$	96	I/O_{PD}	**MII default Speed Operation** Sets the speed setting of the MII port. Can be overridden by software through the MII Port State Override Register. • $\overline{\text{MII\_SPD100}}$ = 0: MII port operates at 100 Mbps. • $\overline{\text{MII\_SPD100}}$ = 1: MII port operates at 10 Mbps.
RVMII_EN	4	I/O_{PD}	**Reverse MII Mode Enable** • 1: Reverse MII • 0: Normal MII (default)
CPU_EEPROM_SEL	47	I_{PU}	**CPU or EEPROM Interface Selection** • 0: Disables SPI interface, and allows for connection to EEPROM. • 1: Configures SPI interface to connect to CPU.
TXD[0]	17	I_{PD}	This pin should be pulled down with an external resistor. This is an engineering test pin, and should be pulled down during power-up.
TXD[1]	14	I_{PD}	This pin should be pulled down with an external resistor. This is an engineering test pin, and should be pulled down during power-up.

Table 35: Signal Description (Cont.)

Signal Name	*Pin Number*	*Type*	*Description*
Power			
VDDC	9, 21, 45, 103, 115	PWR	**1.8V Digital Core VDD**
GNDC	15, 27, 51, 109, 120	GND	**Digital Core GND**
VDDP	10, 22, 44, 98, 104, 114	PWR	**3.3V Digital Periphery (Output Buffer) VDD**
GNDP	16, 28, 35, 50, 102, 108, 121	GND	**Digital Periphery (Output Buffer) GND**
VDDA	65, 76, 77, 88, 89	PWR	**1.8V Analog VDD**
GNDA	66, 75, 78, 87, 90	GND	**Analog GND**
VDDBIAS		PWR	**Bias Circuit VDD**
GNDBIAS	58	GND	**Bias Circuit GND**
VDDPLL	59	PWR	**1.8V PLL Circuit VDD**
GNDPLL	64	GND	**PLL Circuit GND**
VDDXTAL	60	PWR	**3.3V XTAL VDD**
GNDXTAL	63	GND	**XTAL Circuit GND**
No Connect			
DNC	3, 32, 38, 39, 41, 42, 46, 48, 52, 43, 53, 54, 55, 95	DNC	**Do Not Connect.** The pins listed in this block are for test purposes only and should not be connected (float). Do not connect these pins together.

PIN ASSIGNMENT LIST

PIN ASSIGNMENT BY PIN NUMBER

Table 36: Pin Assignment by Pin Number

Pin	Signal Name
1	MDIO
2	MDC
3	DNC
4	RVMII_EN
5	MISO/DO
6	MOSI/DI
7	SCK/SCK
8	$\overline{SS}$ /CS
9	VDDC
10	VDDP
11	COL
12	TXD[3]
13	TXD[2]
14	TXD[1]/pulldown
15	GNDC
16	GNDP
17	TXD[0]/pulldown
18	TXEN
19	TXC
20	TXER
21	VDDC
22	VDDP
23	$\overline{LINK}$
24	CRS
25	RXER
26	RXC
27	GNDC
28	GNDP
29	RXDV
30	RXD[0]
31	RXD[1]
32	DNC
33	RXD[2]
34	RXD[3]

Pin	Signal Name
35	GNDP
36	FREQ[0]
37	FREQ[1]
38	DNC
39	DNC
40	HW_FWDG_EN
41	DNC
42	DNC
43	DNC
44	VDDP
45	VDDC
46	DNC
47	CPU_EEPROM_SEL
48	DNC
49	MDIX_DIS
50	GNDP
51	GNDC
52	DNC
53	DNC
54	DNC
55	DNC
56	VDDBIAS
57	RDAC
58	GNDBIAS
59	VDDPLL
60	VDDXTAL
61	XTALI/CK25
62	XTALO
63	GNDXTAL
64	GNDPLL
65	VDDA
66	GNDA
67	RD1-
68	RD1+

Pin	Signal Name
69	TD1-
70	TD1+
71	TD2+
72	TD2-
73	RD2+
74	RD2-
75	GNDA
76	VDDA
77	VDDA
78	GNDA
79	RD3-
80	RD3+
81	TD3-
82	TD3+
83	TD4+
84	TD4-
85	RD4+
86	RD4-
87	GNDA
88	VDDA
89	VDDA
90	GNDA
91	RD5-
92	RD5+
93	TD5-
94	TD5+
95	DNC
96	MII_SPD100
97	MII_FDX
98	VDDP
99	LEDMODE[2]
100	ENFDXFLOW
101	ENHDXFLOW
1 02	GNDP

Pin	Signal Name
103	VDDC
104	VDDP
105	$\overline{LED1A}$
106	$\overline{LED1B}$
107	$\overline{LED1C}$
108	GNDP
109	GNDC
110	$\overline{LED2A}$
111	$\overline{LED2B}$
112	$\overline{LED2C}$
113	$\overline{LED3A}$
114	VDDP
115	VDDC
116	$\overline{LED3B}$
117	$\overline{LED3C}$
118	$\overline{LED4A}$
119	$\overline{LED4B}$
120	GNDC
121	GNDP
122	$\overline{LED4C}$
123	$\overline{LED5A}$
124	$\overline{LED5B}$
125	$\overline{LED5C}$
126	LEDCLK/LEDMODE[0]
127	LEDDATA/LEDMODE[1]
128	$\overline{RESET}$

PIN ASSIGNMENT BY SIGNAL NAME

Table 37: Pin Assignment by Signal Name

Signal Name	Pin
COL	11
CPU_EEPROM_SEL	47
CRS	24
DNC	32
DNC	38
DNC	39
DNC	41
DNC	42
DNC	43
DNC	46
DNC	48
DNC	52
DNC	55
DNC	3
DNC	95
DNC	54
DNC	53
ENFDXFLOW	100
ENHDXFLOW	101
FREQ[0]	36
FREQ[1]	37
GNDA	66
GNDA	75
GNDA	78
GNDA	87
GNDA	90
GNDBIAS	58
GNDC	15
GNDC	27
GNDC	51
GNDC	109
GNDC	120
GNDP	16
GNDP	28
GNDP	35
GNDP	50
GNDP	102
GNDP	108
GNDP	121
GNDPLL	64
GNDXTAL	63
HW_FWDG_EN	40
$\overline{\text{LED1A}}$	105
$\overline{\text{LED1B}}$	106
$\overline{\text{LED1C}}$	107
$\overline{\text{LED2A}}$	110
$\overline{\text{LED2B}}$	111
$\overline{\text{LED2C}}$	112
$\overline{\text{LED3A}}$	113
$\overline{\text{LED3B}}$	116
$\overline{\text{LED3C}}$	117
$\overline{\text{LED4A}}$	118
$\overline{\text{LED4B}}$	119
$\overline{\text{LED4C}}$	122
$\overline{\text{LED5A}}$	123
$\overline{\text{LED5B}}$	124
$\overline{\text{LED5C}}$	125
LEDCLK/LEDMODE[0]	126
LEDDATA/LEDMODE[1]	127
LEDMODE[2]	99
$\overline{\text{LINK}}$	23
MDC	2
MDIO	1
MDIX_DIS	49
MII_FDX	97
MISO/DO	5
MOSI/DI	6
DNC	43
RD1-	67
RD1+	68
RD2-	74
RD2+	73
RD3-	79
RD3+	80
RD4-	86
RD4+	85
RD5-	91
RD5+	92
RDAC	57
$\overline{\text{RESET}}$	128
RVMII_EN	4
RXC	26
RXD[0]	30
RXD[1]	31
RXD[2]	33
RXD[3]	34
RXDV	29
RXER	25
SCK/SCK	7
$\overline{\text{SS}}$ /CS	8
TD1-	69
TD1+	70
TD2-	72
TD2+	71
TD3-	81
TD3+	82
TD4-	84
TD4+	83
TD5-	93
TD5+	94
TXC	19
TXD[0]/pulldown	17
TXD[1]/pulldown	14
TXD[2]	13
TXD[3]	12
TXEN	18
TXER	20
VDDA	65
VDDA	76
VDDA	77
VDDA	88
VDDA	89
VDDBIAS	56
VDDC	9
VDDC	21
VDDC	45
VDDC	103
VDDC	115
VDDP	10
VDDP	22
VDDP	44
VDDP	98
VDDP	104
VDDP	114
VDDPLL	59
VDDXTAL	60
XTALI/CK25	61
XTALO	62

Section 6: Register Definitions

REGISTER NOTATIONS

In the Register description tables, the following notation in the R/W column is used to describe the ability to read or write:

- R/W = Read or write
- RO = Read only
- LH = Latched high. Clear after read operation
- LL = Latched low. Clear after read operation
- H = Fixed high
- L = Fixed low
- SC = Self clear after read

Reserved bits must be written as the default value and ignored when read.

GLOBAL SWITCH REGISTER MAP

The following table lists the pages defined in the BCM5325E switch core.

Table 38: Switch Global Page Register Map

Page	*Description*
0x00	"Page 0x00: Control Registers" on page 76
0x01	"Page 0x01: Status Registers" on page 84
0x02	"Page 0x02: Management/Mirroring Registers" on page 88
0x03	Reserved
0x04	"Page 0x04: ARL Control Register" on page 93
0x05	"Page 0x05: ARL Access Registers" on page 99
0x06–0x07	Reserved
0x08	"Page 0x08: Memory Access Registers" on page 107
0x09	Reserved
0x0A	"Page 0x0A: IEEE 802.1X Control Registers" on page 109
0x0B–0x0F	Reserved
0x10	"Page 0x10–0x14, 0x19: PHY Port Registers" Port 0 on page 114
0x11	"Page 0x10–0x14, 0x19: PHY Port Registers" Port 1 on page 114
0x12	"Page 0x10–0x14, 0x19: PHY Port Registers" Port 2 on page 114
0x13	"Page 0x10–0x14, 0x19: PHY Port Registers" Port 3 on page 114
0x14	"Page 0x10–0x14, 0x19: PHY Port Registers" Port 4 on page 114
0x15–0x1F	Reserved
0x18	"Page 0x18: MII Port External PHY Registers" on page 126
0x19	"Page 0x10–0x14, 0x19: PHY Port Registers" Global Write on page 114
0x20	"Page 0x20–0x24: Port MIB Registers" Port 0 on page 128
0x21	"Page 0x20–0x24: Port MIB Registers" Port 1 on page 128
0x22	"Page 0x20–0x24: Port MIB Registers" Port 2 on page 128
0x23	"Page 0x20–0x24: Port MIB Registers" Port 3 on page 128
0x24	"Page 0x20–0x24: Port MIB Registers" Port 4 on page 128
0x25–0x27	Reserved
0x28	"Page 0x20–0x24: Port MIB Registers" MII Port on page 128
0x29–0x2F	Reserved
0x30	"Page 0x30: QoS Registers" on page 130
0x31	"Page 0x31: Port-Base VLAN Registers" on page 135
0x32–0x33	Reserved
0x34	"Page 0x34: IEEE 802.1Q VLAN Registers" on page 136
0x35	"Page 0x35: Multicast/Broadcast/DLF Suppression Register" on page 146
0x36–0xFF	Reserved
Maps to All Pages	"Global Registers (Maps to All Pages)" on page 148

PAGE 0X00: CONTROL REGISTERS

Table 39: Control Registers (Page 0x00)

ADDR	Bits	Register Name
0x00	8	"10/100 Port Control Register" Port 0 on page 77
0x01	8	"10/100 Port Control Register" Port 1 on page 77
0x02	8	"10/100 Port Control Register" Port 2 on page 77
0x03	8	"10/100 Port Control Register" Port 3 on page 77
0x04	8	"10/100 Port Control Register" Port 4 on page 77
0x05–0x07	–	Reserved
0x08	8	"MII Port Control Register" on page 78
0x09–0x0A	–	Reserved
0x0B	8	"Switch Mode Register" on page 79
0x0C–0x0D	–	Reserved
0x0E	8	"MII1 Port State Override Register" on page 80
0x0F	8	"Power Down Mode Register" on page 80
0x10–0x11	16	"LED Flash Control Register" on page 81
0x12–0x13	16	"LEDa Control Register" on page 81
0x14–0x15	16	"LEDb Control Register" on page 82
0x16–0x17	16	"LEDc Control Register" on page 82
0x18–0x20	–	Reserved
0x21	8	"Multicast IP Address Control Register" on page 83
0x22–0x24	–	Reserved
0x25	8	"WAN Port Select Register" on page 83
0x26–0x27	16	"Protected Mode Control Register" on page 83
0x28–0xEF	–	Reserved
0xF0	8	"SPI Data I/O Register" on page 148
0xF1	8	"SPI Data I/O Register" on page 148
0xF2	8	"SPI Data I/O Register" on page 148
0xF3	8	"SPI Data I/O Register" on page 148
0xF4	8	"SPI Data I/O Register" on page 148
0xF5	8	"SPI Data I/O Register" on page 148
0xF6	8	"SPI Data I/O Register" on page 148
0xF7	8	"SPI Data I/O Register" on page 148
0xF8–0xFD	–	Reserved
0xFE	8	"SPI Status Register" on page 148
0xFF	8	"Page Register" on page 148

10/100 PORT CONTROL REGISTER

Table 40: 10/100 Port Control Register (Page 0x00: Address 0x00–0x04)

Bit	Name	R/W	Description	Default
7:5	STP_STATE[2:0]	R/W	CPU writes the current computed states of its spanning tree algorithm for this port. • 000 = No spanning tree • 001 = Disabled state • 010 = Blocking state • 011 = Listening state • 100 = Learning state • 101 = Forwarding state • 110–111 = Reserved For more information, see "Bridge Management" on page 29.	000
4:2	Reserved	RO	Write as 00, ignore when read.	00
1	TX_DISABLE	R/W	Disables the transmit function of the port at the MAC level. For more information, see "Media Access Controller" on page 32.	0
0	RX_DISABLE	R/W	Disables the receive function of the port at the MAC level. For more information, see "Media Access Controller" on page 32.	0

MII PORT CONTROL REGISTER

Table 41: MII Port Control Register (Page 0x00: Address 0x08)

Bit	Name	R/W	Description	Default
7:5	STP_STATE[2:0]	R/W	Spanning tree protocol state CPU writes the current computed states of its spanning tree algorithm for this port. • 000 = No spanning tree (unmanaged mode) • 001 = Disabled state • 010 = Blocking state • 011 = Listening state • 100 = Learning state • 101 = Forwarding state • 110–111 = Reserved Ignored when SW_FWDG_MODE = Unmanaged. For more information, see “Bridge Management” on page 29.	001
4	RX_UCST_EN	R/W	Receive unicast enable Enables the receipt of unicast frames on the IMP when the IMP is configured as the frame management port, and the frame was flooded due to no matching address table entry. When cleared, unicast frames that meet the mirror ingress/egress rules are forwarded to the frame management port. Ignored if the IMP is not selected as the frame management port. For more information, see “Frame Management” on page 38.	0
3	RX_MCST_EN	R/W	Receive multicast enable Enables the receipt of multicast frames on the IMP when the IMP is configured as the frame management port, and the frame was flooded due to no matching address table entry. When cleared, multicast frames that meet the mirror ingress/egress rules are forwarded to the frame management port. Ignored if the IMP is not selected as the frame management port. For more information, see “Frame Management” on page 38.	0
2	RX_BCST_EN	R/W	Receive broadcast enable Enables the receipt of broadcast frames on the IMP when the IMP is configured as the frame management port. When cleared, broadcast frames that meet the mirror ingress/egress rules are forwarded to the frame management port. Ignored if the IMP is not selected as the frame management port. For more information, see “Frame Management” on page 38.	0
1	TX_DISABLE	R/W	Disables the transmit function of the port at the MAC level.	0
0	RX_DISABLE	R/W	Disables the receive function of the port at the MAC level.	0

SWITCH MODE REGISTER

Table 42: Switch Mode Register (Page 0x00: Address 0x0B)

Bit	Name	R/W	Description	Default
7:4	Reserved	RO	Write as 0x00, ignore when read.	0x00
3	NOBLKCD	R/W	Do not to block carrier detected signal. • 1 = Do not block, txport always defers to crs. • 0 = Block CD (compatible with BCM5328)	0
2	RTRY_LMT_DIS	R/W	Retry limit disable When set, disables the Retry limit on all MAC ports (10BASE-T/100BASE-TX). Causes a MAC port in half-duplex operation, to continue to retry the same packet regardless of the number of collision attempts. Default operation discards a transmit frame after 15 retry attempts (16 attempts total).	1
1	SW_FWDG_EN	R/W	Software forwarding enable • SW_FWDG_EN = 1: Frame forwarding is enabled. • SW_FWDG_EN = 0: Frame forwarding is disabled. Read from HW_FWDG_EN pin on power-on. Can be overwritten subsequently. For frame-management switch implementations, the switch should be configured to disable forwarding on power-on, to allow the processor to configure the internal address table and other parameters, before frame forwarding is enabled.	HW_FWDG_EN pin value
0	FRAME_MANAGE_MODE	R/W	Frame-management mode Programmed from the inverse of the HW_FWDG_EN pin at power-on. Can be overwritten subsequently. • 0 = Default. • 1 = Frame-management mode The ARL treats reserved multicast addresses differently dependent on this selection. See Table 3 on page 15 for a precise definition.	Inverse of HW_FWDG_EN pin value

MII1 PORT STATE OVERRIDE REGISTER

Table 43: MII1 Port State Override Register (Page 0x00: Address 0x0E)

Bit	Name	R/W	Description	Default
7	MII SW Override	RW	MII software override 0 = Use MII hardware status. 1 = Use contents of this register. ***Note:*** To override any of the following fields in this register, set this bit to 1.	0
6:5	Reserved	R/W	Write as 00, ignore when read.	00
4	RvMII Mode	R/W	Reversed MII mode setting • 0 = Normal MII mode • 1 = Reversed MII mode	0
3	LP_FLOW_CNTRL	R/W	Link partner flow control capability • 0 = Not PAUSE capable • 1 = PAUSE capable	0
2	SPEED100	R/W	Speed • 0 = 10 Mbps • 1 = 100 Mbps	0
1	FDX	R/W	Full-duplex • 0 = Half-duplex • 1 = Full-duplex	0
0	LINK	R/W	Link status • 0 = Link fail • 1 = Link pass	0

POWER DOWN MODE REGISTER

Table 44: Power Down Mode Register (Page 0x00: Address 0x0F)

Bit	Name	R/W	Description	Default
7:5	Reserved	R/W	Write as 000, ignore when read.	000
4:1	PORT[4:1]_POWER_DOWN	R/W	Port 4:1 power-down register Disables all clocking to an individual PHY port. • 0 = PHY is enabled. • 1 = PHY is disabled. Only port 1 to 4 can power-down.	0000
0	PORT[0]_POWER_DOWN	R/W	Do not set bit 0 to a 1. Doing so disables the PLL power and the switch function.	0

LED FLASH CONTROL REGISTER

Table 45: LED Flash Control Register (Page 00h: Address 10h)

Bit	*Name*	*R/W*	*Description*	*Default*
15: 8	Reserved	–	–	0
7:0	Flash Timer	R/W	The value determines the LED flash rate. 0 being the fastest flashing rate, and FF being the slowest flashing rate.	02

LEDA CONTROL REGISTER

Table 46: LEDa Control Register (Page 00h: Address 12h)

Bit	*Name*	*R/W*	*Description*	*Default*
15: 10	Reserved	–	–	111111
9:0	LED Control	R	Software Control for Parallel LED Interface For testing purposes, the mode of each LED can be controlled for each port-based on the mapping below: • Bit[9:8] = Port 4 • Bit[7:6] = Port 3 • Bit[5:4] = Port 2 • Bit[3:2] = Port 1 • Bit[1:0] = Port 0 The value of the bits will control the operation as shown: • 11 = Normal Mode • 10 = Flsh Mode • 01 = ON Mode • 00 = OFF Mode	0x3ff

LEDB CONTROL REGISTER

Table 47: LEDa Control Register (Page 00h: Address 14h)

Bit	Name	R/W	Description	Default
15: 10	Reserved	–	–	111111
9:0	LED Control	R	Software Control for Parallel LED Interface For testing purposes, the mode of each LED can be controlled for each port-based on the mapping below: • Bit[9:8] = Port 4 • Bit[7:6] = Port 3 • Bit[5:4] = Port 2 • Bit[3:2] = Port 1 • Bit[1:0] = Port 0 The value of the bits will control the operation as shown: • 11 = Normal Mode • 10 = Flsh Mode • 01 = ON Mode • 00 = OFF Mode	0x3ff

LEDC CONTROL REGISTER

Table 48: LEDa Control Register (Page 00h: Address 16h)

Bit	Name	R/W	Description	Default
15: 10	Reserved	–	–	111111
9:0	LED Control	R	Software Control for Parallel LED Interface For testing purposes, the mode of each LED can be controlled for each port-based on the mapping below: • Bit[9:8] = Port 4 • Bit[7:6] = Port 3 • Bit[5:4] = Port 2 • Bit[3:2] = Port 1 • Bit[1:0] = Port 0 The value of the bits will control the operation as shown: • 11 = Normal Mode • 10 = Flsh Mode • 01 = ON Mode • 00 = OFF Mode	0x3ff

MULTICAST IP ADDRESS CONTROL REGISTER

Table 49: Multicast IP Address Control Register (Page 0x00: Address 0x21)

Bit	Name	R/W	Description	Default
7:1	Reserved	R/W	Write as 0x00, ignore when read.	0x00
0	IP_MULTICAST	R/W	When set to a 1, it supports the new 4K IP multicast address scheme.	0

WAN PORT SELECT REGISTER

Table 50: WAN Port Select Register (Page 0x00: Address 0x25)

Bit	Name	R/W	Description	Default
7:6	Reserved	R/W	Write as 00, ignore when read.	00
5	Enable Man2WAN	R/W	• 0 = Management port (IMP) can forward only to egress direct frame to WAN port. • 1 = Management port (IMP) can forward either egress-direct or non-egress direct frame to WAN port	1
4:0	WAN port Select[4:0]	R/W	Select which port (4:0) is the WAN port. Only one port can be selected as WAN port. If all bits are zero, WAN port mode is disabled. IMP port can not be a WAN port.	0

PROTECTED MODE CONTROL REGISTER

Table 51: Protected Mode Control Register (Page 0x00: Address 0x26–0x27)

Bit	Name	R/W	Description	Default
15:12	Reserved	R/W	Write as 0x0, ignore when read.	0x0
8	Protected portmap[8]	R/W	Protected portmap for MII port. When the rx port is set in this portmap, the frames received by this port are not forwarded to any ports that are set in the portmap. In a normal mode, this portmap is all 0, which means that frames can be forwarded to any ports.	1
7:5	Reserved	R/W	Write as 00, ignore when read.	00
4:0	Protected portmap[4:0]	R/W	Protected portmap for port 0–4.When the rx port is set in this portmap, the frames received by this port are not forwarded to any ports that are set in the portmap. In a normal mode, this portmap is all 0, which means that frames can be forwarded to any ports.	0

PAGE 0X01: STATUS REGISTERS

Table 52: Status Registers (Page 0x01)

ADDR	Bits	Register Name
0x00–0x01	16	"Link Status Summary" on page 84
0x02–0x03	16	"Link Status Change" on page 85
0x04–0x05	16	"Port Speed Summary" on page 85
0x06–0x07	16	"Duplex Status Summary" on page 86
0x08–0x09	16	"Pause Status Summary" on page 86
0x0A–0x45	–	Reserved
0x46	8	"BIST Status" on page 87
0x47–0xFE	–	Reserved
0xF0	8	"SPI Data I/O Register" 0 on page 148
0xF1	8	"SPI Data I/O Register" 1 on page 148
0xF2	8	"SPI Data I/O Register" 2 on page 148
0xF3	8	"SPI Data I/O Register" 3 on page 148
0xF4	8	"SPI Data I/O Register" 4 on page 148
0xF5	8	"SPI Data I/O Register" 5 on page 148
0xF6	8	"SPI Data I/O Register" 6 on page 148
0xF7	8	"SPI Data I/O Register" 7 on page 148
0xF8–0xFD	–	Reserved
0xFE	8	"SPI Status Register" on page 148
0xFF	8	"Page Register" on page 148

LINK STATUS SUMMARY

Table 53: Link Status Summary Register (Page 0x01: Address 0x00–0x01)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	Write as 0x00, ignore when read.	0x00
8	LINK_STATUS[MII]	RO	Link status Indicating the link status of MII interface. • 0 = Link fail • 1 = Link pass	0
7:5	Reserved	RO	Write as 000, ignore when read.	000
4:0	LINK_STATUS[4:0]	RO	Link status A 5-bit field indicating the link status for each 10BASE-T/100BASE-TX port (bits 0–4 = 10BASE-T/ 100BASE-TX ports). • 0 = Link fail • 1 = Link pass	00000

LINK STATUS CHANGE

Table 54: Link Status Change Register (Page 0x01: Address 0x02–0x03)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	Write as 0x000, ignore when read.	0x00
8	LINK_STATUS_CHANGE[MII]	RC	MII link status change Indicating the link status changed for MII interface. • 0 = Link fail • 1 = Link pass	0
7:5	Reserved	RO	Write as 000, ignore when read.	000
4:0	LINK_STATUS_CHANGE[4:0]	RC	Link status change A 5-bit field indicating that the link status for an individual 10BASE-T/100BASE-TX port had changed since the last read operation (bits 0–4 = 10BASE-T/100BASE-TX ports). Upon change of link status, a bit remains set until cleared by a read operation. • 0 = Link status constant • 1 = Link status change	0

PORT SPEED SUMMARY

Table 55: Port Speed Summary Register (Page 0x01: Address 0x04–0x05)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	Write as 0x00, ignore when read.	0x00
8	MII PORT_SPEED[MII]	RO	Port Speed A 1-bit field indicating the operating speed for the MII port. • 0 = 10 Mbps • 1 = 100 Mbps ***Note:*** Port speed for the MII port can only be reported for an external transceiver by using the CPU to read the port speed via the MCD/MDIO interface and write this back to the MII port status override register (Page 0x0, Address 0x14).	0
7:5	Reserved	RO	Write as 000, ignore when read.	000
5:0	PORT_SPEED[4:0]	RO	Port speed A 5-bit field indicating the operating speed for each 10BASE-T/100BASE-TX port. • 0 = 10 Mbps • 1 = 100 Mbps	0

DUPLEX STATUS SUMMARY

Table 56: Duplex Status Summary Register (Page 0x01: Address 0x06–0x07)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	Write as 0x00, ignore when read.	0x00
8	MII DUPLEX_STATE[MII]	RO	Duplex state A 1-bit field indicating the half/full-duplex state for the MII port. • 0 = Half-duplex • 1 = Full-duplex ***Note:*** The duplex state for the MII port can only be reported for an external transceiver by using the CPU to read the half/full-duplex state via the MCD/MDIO interface and write this back to the MII port status override register (Page 0x0, Address 0x14)	0
7:5	Reserved	RO	Write as 001, ignore when read.	001
4:0	DUPLEX_STATE[4:0]	RO	Duplex state A 6-bit field indicating the half/full-duplex state for each 10BASE-T/100BASE-TX port. • 0 = Half-duplex • 1 = Full-duplex	0

PAUSE STATUS SUMMARY

Table 57: Pause Status Summary Register (Page 0x01: Address 0x08–0x09)

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	Write as 0x00, ignore when read.	0x00
8	PAUSE_STATE[MII]	RO	MII pause state A 1-bit field indicating the pause state for the MII port. • 0 = Half-duplex • 1 = Full-duplex ***Note:*** The pause state for the MII port can only be reported for an external transceiver by using the CPU to read the negotiated pause state via the MCD/MDIO interface and write this back to the MII port status override register (Page 0x0, Address 0x14)	0
7:5	Reserved	RO	Write as 000, ignore when read.	000
4:0	PAUSE_STATE[4:0]	RO	Pause state A 5-bit field indicating the PAUSE state for each 10BASE-T/100BASE-TX port. • 0 = Half-duplex • 1 = Full-duplex	0

BIST STATUS

Table 58: BIST Status Register (Page 0x01: Address 0x46)

Bit	*Name*	*R/W*	*Description*	*Default*
7:2	Reserved	RO	Write as 0x00, ignore when read.	0x00
1	MEM_ERR	RC	Internal packet buffer memory error. Set to indicate the packet buffer memory failed the internal self test during initialization/power-up.	0
0	Reserved	RC	Write as 0, ignore when read.	0

PAGE 0X02: MANAGEMENT/MIRRORING REGISTERS

Table 59: Management Mode Registers (Page 0x02)

ADDR	Bits	Register Name
0x00	8	"Global Management Configuration Register" on page 89
0x02	8	"Revision ID Register" on page 89
0x01–0x03	–	Reserved
0x04–0x05	16	"MIB Mode Select Register" on page 89
0x06–0x09	32	"Aging Time Control Register" on page 90
0x0A–0x0F	–	Reserved
0x10–0x11	16	"Mirror Capture Control Register" on page 90
0x12–0x13	16	"Ingress Mirror Control Register" on page 91
0x14–0x15	16	"Ingress Mirror Divider Register" on page 91
0x16–0x1B	–	Reserved
0x1C–0x1D	16	"Egress Mirror Control Register" on page 92
0x1E–0x1F	16	"Egress Mirror Divider Register" on page 92
0x20–0xEF	–	Reserved
0xF0	8	"SPI Data I/O Register" 0 on page 148
0xF1	8	"SPI Data I/O Register" 1 on page 148
0xF2	8	"SPI Data I/O Register" 2 on page 148
0xF3	8	"SPI Data I/O Register" 3 on page 148
0xF4	8	"SPI Data I/O Register" 4 on page 148
0xF5	8	"SPI Data I/O Register" 5 on page 148
0xF6	8	"SPI Data I/O Register" 6 on page 148
0xF7	8	"SPI Data I/O Register" 7 on page 148
0xF8–0xFD	–	Reserved
0xFE	8	"SPI Status Register" on page 148
0xFF	8	"Page Register" on page 148

GLOBAL MANAGEMENT CONFIGURATION REGISTER

Table 60: Global Management Configuration Register (Page 0x02: Address 0x00)

Bit	Name	R/W	Description	Default
7:6	MANAGE_PORT	R/W	Frame management port Defines the physical port processing management frames directed to the switch. • 00 – 01 = No frame-management port • 10 = MII port (In-band management port) • 11 = Reserved These bits are ignored when Frame_Manage_Mode = Default in the switch mode register, and the device behaves as if there is no defined management port.	10
5:4	Reserved	R/W	Write as 00, ignore when read.	00
3	Enable IGMP IP layer snooping	R/W	When asserted, IGMP IP layer snooping is enabled. As incoming frame has value 2 in IP header's protocol field and not IGMP query, it is forwarded to CPU port.	
2	Reserved	R/W	Write as 0, ignore when read.	
1	RX_BPDU_EN	R/W	Receive BPDU enable Enables all ports to receive BPDUs and forward to the defined physical management port. Management CPU must set this bit to globally allow BPDUs to be received.	0
0	RST_MIB_CNTRS	R/W	Reset MIB counters Resets all MIB counters for all ports to zero (pages 0x20–0x28). The host must set the bit and then clear the bit in successive write cycles to activate the reset operation.	0

REVISION ID REGISTER

Table 61: Revision ID Register (Page 0x02: Address 0x02)

Bit	Name	R/W	Description	Default
1:0	Rev ID	R/W	01 for A1 00 for A0	

MIB MODE SELECT REGISTER

Table 62: MIB Mode Select Register (Page 0x02: Address 0x04–0x05)

Bit	Name	R/W	Description	Default
15:6	Reserved	R/O	Write as 0x00, ignore when read.	0x000

Table 62: MIB Mode Select Register (Page 0x02: Address 0x04–0x05) (Cont.)

Bit	Name	R/W	Description	Default
5:0	MIB Mode Select	R/W	Select group of MIB counters • 0 = To select group-0 of MIB counters. • 1 = To select group-1 of MIB counters. There are four MIB counters for each port, two receive MIB counters and two transmit MIB counters. Each MIB counter is 16 bits. • 5: MII port. (Port-8) • 0–4: 10/100BASE-T ports	0x00

AGING TIME CONTROL REGISTER

Table 63: Aging Time Control Register (Page 0x02: Address 0x06–0x09)

Bit	Name	R/W	Description	Default
31:20	Reserved	R/O	Write as 0x000, ignore when read.	0x000
19:0	AGE_TIME	R/W	Specifies the aging time in seconds for dynamically learned address. Maximum age time is 1,048,575s. ***Note:*** While IEEE 802.1D specifies a range of values of 10–1,000,000 s, this register does not enforce this range. Setting the AGE_TIME to zero disables the aging process.	0x12C'h

MIRROR CAPTURE CONTROL REGISTER

Table 64: Mirror Capture Control Register (Page 0x02: Address 0x10–0x11)

Bit	Name	R/W	Description	Default
15	MIRROR_ENABLE	R/W	Global enable/disable for all mirroring on this chip. When reset, mirroring is disabled. When set, mirroring is enabled according to the ingress and egress control rules, to the port designated by the MIRROR_CAPTURE_PORT.	0
14:11	Reserved	R/O	Write as 0x0, ignore when read.	0x0
10:0	CAPTURE_PORT	R/W	Mirror capture port Bit mask which identifies the single unique port which is designated as the port to which all ingress and/or egress traffic is mirrored on this chip/system. Bit(s): • 0–4 = 10BASE-T/100BASE-TX ports • 5–7 = 000 • 8 = MII/IMP • 9 = 0 • 10 = Reserved	0

For more information, see “Port Mirroring” on page 9.

INGRESS MIRROR CONTROL REGISTER

Table 65: Ingress Mirror Control Register (Page 0x02: Address 0x12–0x13)

Bit	Name	R/W	Description	Default
15:14	Reserved	R/O	Write as 00, ignore when read.	00
13	IN_DIV_EN	R/W	Ingress divider enable Mirror every n^{th} received frame (n represents the IN_MIRROR_DIV defined in "Ingress Mirror Divider Register (page 02h: Address 14h)" below) that has passed through the IN_MIRROR_FILTER.	0
12:11	Reserved	R/O	Write as 00, ignore when read.	00
10:0	IN_MIRROR_MASK	R/W	Ingress mirror port mask. An 11-bit mask that selectively allows any port with its corresponding bit set to be mirrored to the port identified by the MIRROR_CAPTURE_PORT value. Note that while multiple bits in a device may be set, severe congestion and/or frame loss may occur if excessive bandwidth from the mirrored port(s) is directed to the MIRROR_CAPTURE_PORT. Bit(s): • 0–4 = 10BASE-T/100BASE-TX ports • 5:7 = Reserved • 8 = MII • 9 = 0 • 10 = Reserved	0x000

For more information, see "Port Mirroring" on page 9.

INGRESS MIRROR DIVIDER REGISTER

Table 66: Ingress Mirror Divider Register (Page 0x02: Address 0x14–0x15)

Bit	Name	R/W	Description	Default
15:10	Reserved	R/O	Write as 00000, ignore when read.	00000
9:0	IN_MIRROR_DIV	R/W	Ingress mirror divider Receive frames that have passed the IN_MIRROR_FILTER rule can further be pruned to reduce the overall number of frames returned to the MIRROR_CAPTURE_PORT. When the IN_DIV_EN bit in the ingress mirror control register is set, frames that pass the IN_MIRROR_FILTER rule are further divided by the value loaded into this register, so that only one in n frames (where n = IN_MIRROR_DIV+1) is mirrored.	0x000

For more information, see "Port Mirroring" on page 9.

EGRESS MIRROR CONTROL REGISTER

Table 67: Egress Mirror Control Register (Page 0x02: Address 0x1C–0x1D)

Bit	Name	R/W	Description	Default
15:14	Reserved	R/O	Write as 00, ignore when read.	00
13	OUT_DIV_EN	R/W	Egress divider enable Mirror every nth transmitted frame (n represents the OUT_MIRROR_DIV defined below in "Egress Mirror Divider Register (page 02h: Address 1Eh)") that has passed through the OUT_MIRROR_FILTER.	0
12:11	Reserved	R/O	Write as 00, ignore when read.	00
10:0	OUT_MIRROR_MASK	R/W	Egress mirror port mask An 11-bit mask that selectively allows any port with its corresponding bit set, to be mirrored to the port identified by the MIRROR_CAPTURE_PORT value. Note that while multiple bits in a device may be set, severe congestion and/or frame loss may occur if excessive bandwidth from the mirrored port(s) is directed to the MIRROR_CAPTURE_PORT. Bit(s): • 0–4 = 10BASE-T/100BASE-TX ports • 5:7 = reserved • 8= MII • 9 = 0 • 10 = Reserved	0x000

For more information, see “Port Mirroring” on page 9.

EGRESS MIRROR DIVIDER REGISTER

Table 68: Egress Mirror Divider Register (Page 0x02: Address 0x1E–0x1F)

Bit	Name	R/W	Description	Default
15:10	Reserved	R/O	Write as 0x00, ignore when read.	0x00
9:0	OUT_MIRROR_DIV	R/W	Egress mirror divider Transmit frames that have passed the OUT_MIRROR_FILTER rule can further be pruned to reduce the overall number of frames returned to the MIRROR_CAPTURE_PORT. When the OUT_DIV_EN bit in the egress mirror control register is set, frames that pass the OUT_MIRROR_FILTER rule are further divided by the value loaded into this register, so that only one in n frames (where n = OUT_MIRROR_DIV+1) is mirrored.	0x000

For more information, see “Port Mirroring” on page 9.

PAGE 0X04: ARL CONTROL REGISTER

Table 69: ARL Control Registers (Page 0x04)

ADDR	Bits	Register Name
0x00	8	"Global ARL Configuration Register" on page 94
0x01–0x03	–	Reserved
0x04–0x09	64	"BPDU Multicast Address Register" on page 94
0x0A–0x0F	–	Reserved
0x10–0x15	48	"Multiport Address 1 Register" on page 95
0x16–0x17	16	"Multiport Vector 1 Register" on page 95
0x18–0x1F	–	Reserved
0x20–0x25	48	"Multiport Address 2 Register" on page 96
0x26–0x27	16	"Multiport Vector 2 Register" on page 96
0x28–0x2F		Reserved
0x30–0x31	16	"Secure Source Port Mask" on page 97
0x32–0x33	16	"Secure Destination Port Mask" on page 97
0x34–0xEF	–	Reserved
0xF0	8	"SPI Data I/O Register" 0 on page 148
0xF1	8	"SPI Data I/O Register" 1 on page 148
0xF2	8	"SPI Data I/O Register" 2 on page 148
0xF3	8	"SPI Data I/O Register" 3 on page 148
0xF4	8	"SPI Data I/O Register" 4 on page 148
0xF5	8	"SPI Data I/O Register" 5 on page 148
0xF6	8	"SPI Data I/O Register" 6 on page 148
0xF7	8	"SPI Data I/O Register" 7 on page 148
0xF8–0xFD	–	Reserved
0xFE	8	"SPI Status Register" on page 148
0xFF	8	"Page Register" on page 148

GLOBAL ARL CONFIGURATION REGISTER

Table 70: Global ARL Configuration Register (Page 0x04: Address 0x00)

Bit	Name	R/W	Description	Default
7:5	Reserved	R/O	Write as 000, ignore when read.	000
4	MPORT_ADDR_EN	R/W	Multiport address enable When set by the host, enables the multiport address 1 and 2 registers, and their associated multiport vector 1 and 2 registers. This enables these registers in the ARL search. Note that if only one multiport address is required, the host should write both multiport address/vector entries to the same value. For more information, see "Using the Multiport Addresses" on page 29.	0
3:1	Reserved	R/O	Write as 000, ignore when read.	000
0	HASH_DISABLE	R/W	Hash function disable Disables the hash function of the ARL table so that entries are directly mapped to the table, instead of being hashed to an index. • 1: Disable hash function. • 0: Enable hash function. For more information see "Address Table Organization" on page 23.	0

BPDU MULTICAST ADDRESS REGISTER

Table 71: BPDU Multicast Address Register (Page 0x04: Address 0x04–0x09)

Bit	Name	R/W	Description	Default
47:0	BPDU_MC_ADDR	R/\W	BPDU multicast address Defaults to the IEEE 802.1 defined reserved multicast address for the bridge group address. Programming to an alternate value allows support of proprietary protocols in place of the normal spanning tree protocol. Frames with a matching DA to this address is forwarded only to the designated management port. The BPDU_MC_ ADDR is stored in canonical format.	01-80-C2-00-00-00

MULTIPORT ADDRESS 1 REGISTER

Table 72: Multiport Address 1 Register (Page 0x04: Address 0x10–0x15)

Bit	Name	R/W	Description	Default
47:0	MPORT_ADDR_1	R/W	Multiport address 1. Allows a frames with a matching DA to this address to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the multiport vector 1 register. Must be enabled using the MPORT_ADDR_EN bit in the global ARL configuration register. The MPORT_ADDR_1 is stored in canonical format.	00-00-00-00-00-00

For more information, see "Using the Multiport Addresses" on page 29.

MULTIPORT VECTOR 1 REGISTER

Table 73: Multiport Vector 1 Register (Page 0x04: Address 0x16–0x17)

Bit	Name	R/W	Description	Default
15:11	Reserved	R/O	Write as 0x00, ignore when read.	0x00
10:0	MPORT_VCTR_1	R/W	Multiport vector 1. A bit mask corresponding to the physical ports on the chip. A frame with a DA matching the content of the multiport address 1 register is forwarded to each port with a bit set in the multiport vector 1-bit map. Bit(s): • 0–4: 10BASE-T/100BASE-TX ports • 5–7: Reserved • 8: MII ports • 9: 0 • 10: Reserved	0x000

For more information, see "Using the Multiport Addresses" on page 29.

MULTIPORT ADDRESS 2 REGISTER

Table 74: Multiport Address 2 Register (Page 0x04: Address 0x20–0x25)

Bit	Name	R/W	Description	Default
47:0	MPORT_ADDR_2	R/W	Multiport address 2. Allows a frames with a matching DA to this address to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the multiport vector 2 register. Must be enabled using the MPORT_ADDR_EN bit in the global ARL configuration register. The MPORT_ ADDR_2 is stored in canonical format.	00-00-00-00-00-00

For more information, see "Using the Multiport Addresses" on page 29.

MULTIPORT VECTOR 2 REGISTER

Table 75: Multiport Vector 2 Register (Page 0x04: Address 0x26–0x27)

Bit	Name	R/W	Description	Default
15:11	Reserved	R/O	Write as 0x00, ignore when read.	0x00
10:0	MPORT_VCTR_2	R/W	Multiport vector 2. A bit mask corresponding to the physical ports on the chip. A frame with a DA matching the content of the multiport address 2 register is forwarded to each port with a bit set in the multiport vector 2-bit map. Bit(s): • 0–4: 10BASE-T/100BASE-TX ports • 5–7: Reserved • 8: MII ports • 9: 0 • 10: Reserved	0x000

For more information, see "Using the Multiport Addresses" on page 29.

SECURE SOURCE PORT MASK

Table 76: Secure Source Port Mask (Page 0x04: Addresses 0x30–0x31)

Bit	Name	R/W	Description	Default
15:11	Reserved	R/O	Write as 0x00, ignore when read.	0x00
10:0	SECSRC_PORTMASK	R/W	Secure source port mask A bit mask corresponding to the physical ports on the chip. A frame with a destination address which corresponds to a port with a bit set in this mask is dropped if the frame's source port does not have its corresponding bit set in the secure destination port mask. Bit(s): • 0–4: 10BASE-T/100BASE-TX ports • 5–7: Reserved • 8: MII ports • 9: 0 • 10: Reserved	0x000

SECURE DESTINATION PORT MASK

Table 77: Secure Destination Port Mask (Page 0x04: Addresses 0x32–0x33)

Bit	Name	R/W	Description	Default
15:11	Reserved	R/O	Write as 0x00, ignore when read.	0x00
10:0	SECDEST_PORTMASK	R/W	Secure destination port mask A bit mask corresponding to the physical ports on the chip. A frame with a destination address which corresponds to a port with a bit NOT set in secure source port mask is dropped if the frame's source port does not have its corresponding bit set in the secure destination port mask. Bit(s): • 0–4: 10BASE-T/100BASE-TX ports • 5–7: Reserved • 8: MII ports • 9: 0 • 10: Reserved	0x000

Example: Usage of Secure Source and Destination Port Mask Registers

- A five-port switch case: P4, P3, P2, P1, P0
- Set SECSRC_PORTMASK = [11000]
- Set SECDEST_PORTMASK = [10101]

If a broadcast packet comes in from:

- P0, the destination port map is [11110]. Because some bits are set in SECSRC_PORTMASK, the ARL logic checks to see if bit 0 in SECDEST_PORTMASK is set. If the answer is YES, the ARL does not change the destination port map.
- P1, the destination port map is [11101]. Because some bits are set in SECSRC_PORTMASK, the ARL logic checks to see if bit 1 in SECDEST_PORTMASK is set. If the answer is NO, the ARL logic changes the destination port map as[11101] and ~[11000] = [00101]. The result is that this broadcast packet only floods to ports P2 and P0.

PAGE 0X05: ARL ACCESS REGISTERS

Table 78: ARL Access Registers (Page 0x05)

ADDR	Bits	Register Name
0x00	8	"ARL Read/Write Control Register" on page 100
0x01–0x0F	–	Reserved
0x02–0x07	48	"MAC Address Index Register" on page 100
0x08	8	"VID Table Index Register" on page 101
0x09–0x0F	–	Reserved
0x10–0x17	64	"ARL Entry 0 Register" on page 101
0x18–0x1F	64	"ARL Entry 1 Register" on page 102
0x20	8	"ARL Search Control Register" on page 104
0x21–0x23	–	Reserved
0x24–0x2B	64	"ARL Search Result Register" on page 105
0x2C	8	"ARL Search Result Extension Register" on page 106
0x2D–0x2F	–	Reserved
0x30	8	"VID Entry 0 Register" on page 106
0x31	–	Reserved
0x32	8	"VID Entry 1 Register" on page 106
0x33–0xEF	–	Reserved
0xF0	8	"SPI Data I/O Register" 0 on page 148
0xF1	8	"SPI Data I/O Register" 1 on page 148
0xF2	8	"SPI Data I/O Register" 2 on page 148
0xF3	8	"SPI Data I/O Register" 3 on page 148
0xF4	8	"SPI Data I/O Register" 4 on page 148
0xF5	8	"SPI Data I/O Register" 5 on page 148
0xF6	8	"SPI Data I/O Register" 6 on page 148
0xF7	8	"SPI Data I/O Register" 7 on page 148
0xF8–0xFD	–	Reserved
0xFE	8	"SPI Status Register" on page 148
0xFF	8	"Page Register" on page 148

ARL Read/Write Control Register

Table 79: ARL Read/Write Control Register (Page 0x05: Address 0x00)

Bit	Name	R/W	Description	Default
7	START/DONE	R/W (SC)	Start/done command Write as 1 to initiate a read or write command, after first loading the MAC_ADDR_INDX register with the MAC address for which the ARL entry is to be read or written. The BCM5325E resets the bit to indicate a write operation completed, or a read operation has completed and data from the bin entry is available in ARL entry 0/1 Note that both ARL entry 0 and 1 are both always read/written by the BCM5325E when accessing the address table locations in memory.	0
6:1	Reserved	RO	Write as 0x00, ignore when read.	0x00
0	ARL_R/W	R/W	ARL read/write • 1 = Read • 0 = Write	

For more information, see “Accessing the ARL Table Entries” on page 28.

MAC Address Index Register

Table 80: MAC Address Index Register (Page 0x05: Address 0x02–0x07)

Bit	Name	R/W	Description	Default
47:0	MAC_ADDR_INDX	R/W	MAC address index The MAC address for which status is to be read or written. By writing the 48-bit SA or DA address, and initiating a read command, the complete ARL bin location (2 entries deep) is returned in the ARL entry 0/1 locations. Both entries are 64 bits wide. Initiating a write command writes the contents of ARL entry 0/1 to the specified bin location (2 entries deep) and overwrites the current contents of the bin, regardless of the status of the valid bit(s) in each entry. The MAC_ADDR_INDX is stored in canonical format.	00-00-00-00-00-00

For more information, see “Accessing the ARL Table Entries” on page 28.

VID TABLE INDEX REGISTER

Table 81: VID Table Index Register (Page 0x05: Address 0x08)

Bit	Name	R/W	Description	Default
8:4	Reserved	RO	Write as 0x00, ignore when read	0x0
3:0	VID_TBL_INDX	R/W	VID table index. When VID_MAC hash enable asserted (page 0x31, addr 0x14), VID_TBL_INDX and MAC_ADDR_INDX is used for hashing ARL table entry when CPU use ARL read/write control (page 0x05, addr 0x0). to access ARL table. There are 16 VLAN entries, there are 4 bits VID that can be changed by users. The most significant 8 bits are fixed and are programmed (page 0x34, address 0x09 bits [11:4]).	0x0

For more information, see "Accessing the ARL Table Entries" on page 28.

ARL ENTRY 0 REGISTER

Table 82: ARL Entry 0 Register (Page 0x05: Address 0x10–0x17)

Bit	Name	R/W	Description	Default
63	VALID0	R/W	Valid Set to indicate that a valid MAC address is stored in the MACADDR0 field, and that the entry has not aged out or been freed by the management processor. Reset when an entry is empty, the address has been aged out by the internal aging process, or the external management processor has invalidated the entry. Automatic learning takes place if an address location is not valid and has not been marked as static.	0
62	STATIC0	R/W	Static Set to indicate that the entry is controlled by the external management processor, and automatic learning and aging of the entry won't take place. When cleared, the internal learning and aging process controls the validity of the entry.	
61	AGE0	R/W	Age Set to indicate that an address entry has been learned or accessed. Reset by the internal aging algorithm. If the internal aging process detects a Valid entry has remained unused for the period set by the AGE_TIME, and the entry has not been marked as static, the entry has the valid bit cleared. The age bit is ignored if the entry has been marked as static.	
60:59	Priority	R/W	Priority bits.	00
58:52	Reserved	RO	Write as 0x00, ignore when read.	0x00

Table 82: ARL Entry 0 Register (Page 0x05: Address 0x10–0x17) (Cont.)

Bit	Name	R/W	Description	Default
51:48	PORTID0	R/W	Unicast port identification The port number which identifies where the station with unique MACADDR0 is connected. 0000 = port 0 0001 = port 1 0010 = port 2 0011 = port 3 0100 = port 4 1000 = MII port Others = Invalid	
47:0	MACADDR0	R/W	MAC address 0 The MACADDR0 is stored in canonical format.	00-00-00-00-00-00
For multicast MAC address, the bit 60:48 becomes the multicast port mask. These 13 bits define the egress port mask when set. Bit(s): • [60:55] = Reserved • [54] = CPU • [53] = MII • [52:48] = 10/100 ports				

For more information, see “Accessing the ARL Table Entries” on page 28.

ARL Entry 1 Register

Table 83: ARL Entry 1 Register (Page 0x05: Address 0x18–0x1F)

Bit	Name	R/W	Description	Default
63	VALID1	R/W	Valid Set to indicate that a valid MAC address is stored in the MACADDR1 field, and that the entry has not aged out or been freed by the management processor. Reset when an entry is empty, the address has been aged out by the internal aging process, or the external management processor has invalidated the entry. Automatic learning takes place if an address location is not valid and has not been marked as static.	0
62	STATIC1	R/W	Static Set to indicate that the entry is controlled by the external management processor, and automatic learning and aging of the entry won’t take place. When cleared, the internal learning and aging process controls the validity of the entry.	

Table 83: ARL Entry 1 Register (Page 0x05: Address 0x18–0x1F) (Cont.)

Bit	Name	R/W	Description	Default
61	AGE1	R/W	Age Set to indicate that an address entry has been learned or accessed. Reset by the internal aging algorithm. If the internal aging process detects a valid entry has remained unused for the period set by the AGE_TIME, and the entry has not been marked as static, the entry has the valid bit cleared. The age bit is ignored if the entry has been marked as static.	
60:59	Priority	R/W	Priority bits	00
58:52	Reserved	RO	Write as 0x00, ignore when read.	0x00
51:48	PORTID1	R/W	Unicast port identification The port number which identifies where the station with unique MACADDR1 is connected. • 0000 = port 0 • 0001 = port 1 • 0010 = port 2 • 0011 = port 3 • 0100 = port 4 • 1000 = MII port • Others = Invalid	
47:0	MACADDR1	R/W	MAC address 1 The MACADDR1 is stored in canonical format.	
For multicast MAC address, the bit 60:48 becomes the multicast port mask. These 13 bits define the egress port mask when set. Bit(s): • [60:55] = Reserved • [54] = CPU • [53] = MII • [52:48] = 10/100 ports				

For more information, see “Accessing the ARL Table Entries” on page 28.

ARL Search Control Register

Table 84: ARL Search Control Register (Page 0x05: Address 0x20)

Bit	Name	R/W	Description	Default
7	START/DONE	R/W (SC)	Start/done Write as 1 to initiate a sequential search of the ARL entries, returning each entry that is currently occupied (Valid = 1 and AGE = 0) in the ARL search result register. Reading the ARL search result Register causes the ARL search to continue. The BCM5325E clears this bit to indicate the entire ARL entry database has been searched.	0
6:1	Reserved	RO	Write as 0x00, ignore when read.	0x00
0	ARL_SR_VALID		ARL search result is valid Set by the BCM5325E to indicate that an ARL entry is available in the ARL search result register. Reset by a host read to the ARL search result register, which causes the ARL search process to continue through the ARL entries until the next entry is found with a valid bit is set.	

For more information, see “Accessing the ARL Table Entries” on page 28.

ARL SEARCH RESULT REGISTER

Table 85: ARL Search Result Register (Page 0x05: Address 0x24–0x2B)

Bit	*Name*	*R/W*	*Description*	*Default*
63	VALID	RO	Valid Indicates a valid MAC address is stored in the MACADDR field, and that the entry has not aged out or been freed by the management processor. All entries returned by the ARL search process has the valid bit set.	
62	STATIC	RO	Static Set to indicate that the entry is controlled by the external management processor, and automatic learning and aging of the entry won't take place. All entries with the static bit set is returned by the ARL search process. When cleared, the internal learning and aging process controls the validity of this entry.	
61	AGE	RO	Age Set to indicate that this address entry has been learned or accessed. Reset by the internal aging algorithm. The ARL search process returns an entry if it is valid and/or static, the age bit is irrelevant.	
60:57	Reserved	RO	Write as 0, ignore when read.	0
56:53	VLAN ID (unicast)	RO	VLAN ID of the corresponding port.	0x0
52	Reserved (unicast)	RO	Write as 0, ignore when read.	0
51:48	PORTID (unicast)	RO	Port Identification The port number which identifies where the station with unique MACADDR is connected. • 0000 = port 0 • 0001 = port 1 • 0010 = port 2 • 0011 = port 3 • 0100 = port 4 • 1000 = MII Port • Others = Invalid	
47:0	MACADDR	RO	MAC address The unique MAC address of the station occupying this ARL entry. The MACADDR is stored in canonical format.	
For multicast MAC address, the bit 52:48 becomes the multicast port mask. These bits define the egress port mask when set. Bit[52:48] = 10/100 port map [4:0]				

For more information, see "Accessing the ARL Table Entries" on page 28.

ARL Search Result Extension Register

Table 86: ARL Search Result Extension Register (Page 0x05: Address 0x2C)

Bit	Name	R/W	Description	Default
7:3	Reserved	RO	Write as 0x00, ignore when read.	0x00
2	Reserved (unicast) PortMap [MII] (multicast)	RO	Write as 0, ignore when read for unicast MAC address. The MII port of the multicast destination port map field for multicast MAC address (bit 40 of MAC address is 1).	0
1:0	Priority	RO	The priority field of ARL table. This is valid for either unicast or multicast MAC address.	0

For more information, see "Accessing the ARL Table Entries" on page 28.

VID Entry 0 Register

Table 87: VID Entry 0 Register (Page 0x05: Address 0x30)

Bit	Name	R/W	Description	Default
7:4	Reserved	RO	Write as 0x0, ignore when read.	0x0
3:0	ARL VLAN ID Entry 0	R/W	When VID_MAC hash enable asserted (page 0x31, addr 0x14) and CPU use ARL read/write control (page 0x05, addr 0x0) to access ARL table, ARL_VID_Entry_0 is written to bin 0 of ARL table entry. The BCM5325E has 16 VLAN entries, there are only 8 bits VID can be changed by users. These bits are programmed (page 0x34, addr. 0x9 [11:4]).	0x00

VID Entry 1 Register

Table 88: VID Entry 1 Register (Page 0x05: Address 0x32)

Bit	Name	R/W	Description	Default
7:4	Reserved	RO	Write as 0x0, ignore when read.	0x0
3:0	ARL VLAN ID Entry 1	R/W	When VID_MAC hash enable asserted (page 0x31, addr 0x14) and CPU use ARL read/write control (Page 0x05, Addr 0x0) to access ARL table, ARL_VID_Entry_1 is written to bin 1 of ARL table entry. The BCM5325E has 16 VLAN entries, there are only 8 bits VID can be changed by users. These bits are programmed (page 0x34, addr. 0x9 [11:4]).	0x00

PAGE 0X08: MEMORY ACCESS REGISTERS

Table 89: Memory Access Registers (Page 0x08)

Address	Bits	Register Name
0x00–0x03	32	"Memory Read/Write Control Register" on page 107
0x04–0x0B	64	"Memory Read/Write Data Register" on page 108
0x0C	8	"Memory Read/Write VID Register" on page 108
0x0D–0xEF		Reserved
0xF0	8	"SPI Data I/O Register" 0 on page 148
0xF1	8	"SPI Data I/O Register" 1 on page 148
0xF2	8	"SPI Data I/O Register" 2 on page 148
0xF3	8	"SPI Data I/O Register" 3 on page 148
0xF4	8	"SPI Data I/O Register" 4 on page 148
0xF5	8	"SPI Data I/O Register" 5 on page 148
0xF6	8	"SPI Data I/O Register" 6 on page 148
0xF7	8	"SPI Data I/O Register" 7 on page 148
0xF8–0xFD	–	Reserved
0xFE	8	"SPI Status Register" on page 148
0xFF	8	"Page Register" on page 148

MEMORY READ/WRITE CONTROL REGISTER

Table 90: Memory Read/Write Control Register (Page 0x08: Address 0x00–0x03)

Bit	Name	R/W	Description	Default
19	START/DONE	R/W	Start/done command Write as 1 to initiate a read or write memory location after first loading the MEM_ADDR with the address which is to be read or written. The BCM5325E resets the bit to indicate that a write operation is completed, or a read operation has completed and data from the memory location is available in memory entry register. Note that the entire 64-bit memory entry is always read/written by the BCM5325E when accessing the RAM.	0
18	MEM_R/W	R/W	Memory read/write • 1 = Read • 0 = Write	0
17:16	Reserved	RO	Write as 00, ignore when read.	00
13:0	MEM_ADDR	RW	The 14-bit memory address that points to a unique 64-bit memory entry in the internal RAM. The address location has its contents read into the memory entry register, or that the contents of the memory entry register is written to the internal RAM location specified. Note that the addressing format is incremented by one for every 64-bit entry.	–

MEMORY READ/WRITE DATA REGISTER

Table 91: Memory Read/Write Data Register (Page 0x08: Address 0x04–0x0B)

Bit	Name	R/W	Description	Default
63:0	RAM_DATA[63:0]	R/W	The 64 bits of data to be written to memory, or data that has been read from memory, as configured in the memory read/write control register, prior to setting the start bit.	–

MEMORY READ/WRITE VID REGISTER

Table 92: Memory Read/Write VID_Mem Register (Page 0x08: Address 0x0C)

Bit	Name	R/W	Description	Default
3:0	VID_MEM[3:0]	R/W	The 4 bits of data to be written to VID memory, or data that has been read from VID memory, as configured in the memory read/write control register, prior to setting the start bit. This register is valid only when the address is in the range of 0x1C00 ~ 0x1FFF which corresponds to ARL table area.	–

PAGE 0X0A: IEEE 802.1X CONTROL REGISTERS

Table 93: IEEE 802.1X Control Register (Page 0x0A)

Address	Bits	Register Name
0x00–0x4B	16	Reserved
0x4C–0x4D	16	"IEEE 802.1X Control 1 Register" on page 110
0x4E–0x4F	16	"IEEE 802.1X Control 2 Register" on page 110
0x64–0x65	16	"Queue 0 TXDSC Control 3 Register" on page 111
0x072–0x73	16	"Queue 1 TXDSC Control 3 Register" on page 111
0x80–0x81	16	"Queue 2 TXDSC Control 3 Register" on page 111
0x8E–0x8F	16	"Queue 3 TXDSC Control 3 Register" on page 112
0x90–0x93	–	Reserved
0x94–0x95	16	"Multicast DLF Drop Control Register (Page 0x0A: Address 0X94-0x95)" on page 112
0x96–0x97	16	"Unicast DLF Drop Control Register (Page 0x0A: Address 0x96-0x97)" on page 113
0x98–0xEF	–	Reserved
0xF0	8	"SPI Data I/O Register" 0 on page 148
0xF1	8	"SPI Data I/O Register" 1on page 148
0xF2	8	"SPI Data I/O Register" 2 on page 148
0xF3	8	"SPI Data I/O Register" 3 on page 148
0xF4	8	"SPI Data I/O Register" 4 on page 148
0xF5	8	"SPI Data I/O Register" 5 on page 148
0xF6	8	"SPI Data I/O Register" 6 on page 148
0xF7	8	"SPI Data I/O Register" 7 on page 148
0xF8h–0xFD	–	Reserved
0xFE	8	"SPI Status Register" on page 148
0xFF	8	"Page Register" on page 148

IEEE 802.1X CONTROL 1 REGISTER

Table 94: IEEE 802.1X Control 1 Register (Page 0x0A: Address 0x4C–0x4D)

Bit	Name	R/W	Description	Default
15:2	RESERVED	RO	Write as 0x0000, ignore when read.	0x0000
1	BPDU_EAPOL_EN	R/W	BPDU and EAPOL packet enable Setting this bit allows BPDU and EAPOL frames (but no other traffic) to be forwarded on ports set in the "IEEE 802.1X Control 2 Register" on page 110.	
0	RESERVED	RO	Write as 0, ignore when read.	0

For more information, see "IEEE 802.1X Port-Based Security" on page 11.

IEEE 802.1X CONTROL 2 REGISTER

Table 95: IEEE 802.1X Control 2 Register (Page 0x0A: Address 0x4E–0x4F)

Bit	Name	R/W	Description	Default
15:9	RESERVED	RO	Write as 0x00, ignore when read.	0x00
8:0	802.1X_EN	R/W	IEEE 802.1X enable Setting the bit of a corresponding port, enables IEEE 802.1X. When set, all incoming frames are blocked at the corresponding port. The only exception is BPDU and EAPOL frames when "BPDU_EAPOL_EN" on page 110 is set. Bit(s): • 0–4: 10/100BASE-T ports • 5–7: Reserved • 8: MII Port	

For more information, see "IEEE 802.1X Port-Based Security" on page 11.

QUEUE 0 TXDSC CONTROL 3 REGISTER

Note: Broadcom recommends the user not change this register unless advised by Broadcom.

Table 96: Queue 0 TxDsc Control 3 Register (Page 0Ah: Address 0x64-0x65)

Bit	Name	R/W	Description	Default
15:8	RESERVED	R/W	–	–
7:5	RESERVED	RO	–	0h
4:0	Q0_quota_size	R/W	The round robin weight for priority queue 0.	0h
Note: The user must make sure bits 15:8 are not mistakenly changed when changing Q0_quota_size.				

QUEUE 1 TXDSC CONTROL 3 REGISTER

Note: Broadcom recommends the user not change this register unless advised by Broadcom.

Table 97: Queue 1 TxDsc Control 3 Register (Page 0Ah: Address 0x72-0x73)

Bit	Name	R/W	Description	Default
15:8	RESERVED	R/W	–	–
7:5	RESERVED	RO	–	0h
4:0	Q1_quota_size	R/W	The round robin weight for priority queue 1. 1Q = 1h 2Q = 2h 3Q = 4h 4Q = 8h	0h
Note: The user must make sure bits 15:8 are not mistakenly changed when changing Q1_quota_size.				

QUEUE 2 TXDSC CONTROL 3 REGISTER

Note: Broadcom recommends the user not change this register unless guided by Broadcom.

Table 98: Queue 2 TxDsc Control 3 Register (Page 0Ah: Address 0x80-0x81)

Bit	Name	R/W	Description	Default
15:8	RESERVED	R/W	–	–
7:5	RESERVED	RO	–	0h

Table 98: Queue 2 TxDsc Control 3 Register (Page 0Ah: Address 0x80-0x81) (Cont.)

Bit	Name	R/W	Description	Default
4:0	Q2_quota_size	R/W	The round robin weight for priority queue 2. 1Q = 0h 2Q = 0h 3Q = 1h 4Q = 1h	0h
Note: The user must make sure bits 15:8 are not mistakenly changed when changing Q2_quota_size.				

QUEUE 3 TXDSC CONTROL 3 REGISTER

Note: Broadcom recommends the user not change this register unless guided by Broadcom.

Table 99: Queue 3 TxDsc Control 3 Register (Page 0Ah: Address 0x8E-0x8F)

Bit	Name	R/W	Description	Default
15:8	RESERVED	R/W	–	–
7:5	RESERVED	RO	–	0h
4:0	Q3_quota_size	R/W	The round robin weight for priority queue 3. 1Q = 0h 2Q = 0h 3Q = 0h 4Q = 2h	0h
Note: The user must make sure bits 15:8 are not mistakenly changed when changing Q3_quota_size.				

MULTICAST DLF DROP CONTROL REGISTER

Table 100: Multicast DLF Drop Control Register (Page 0x0A: Address 0X94-0x95)

Bit	Name	R/W	Description	Default
15:12	RESERVED	RO	Write as 0x0, ignore when read.	0x0
11	Mcast_DLF_drop_enable	R/W	Enable the multicast DLF frame drop mode.	0
10:9	RESERVED	RO	Write as 00, ignore when read.	00
8	Mcast_DLF_portmap[MII]	R/W	When this bit is set, if the multicast frame has an ARL miss, the frame is flooded only to the MII port. This map is valid only when Mcast_DLF_drop_enable = 1.	0
7:5	RESERVED	RO	Write as 000, ignore when read.	000
4:0	Mcast_DLF_portmap[4:0]	R/W	When is port map is set, if the multicast frame has an ARL miss, the frame is flooded only to the ports that are set in this portmap. This map is valid only when Mcast_DLF_drop_enable = 1	0x00

UNICAST DLF DROP CONTROL REGISTER

Table 101: Unicast DLF Drop Control Register (Page 0x0A: Address 0x96-0x97)

Bit	Name	R/W	Description	Default
15:12	RESERVED	RO	Write as 0x0, ignore when read.	0x0
11	Ucast_DLF_drop_enable	R/W	Enable the unicast DLF frame drop mode.	0
10:9	RESERVED	RO	Write as 00, ignore when read.	00
8	Ucast_DLF_portmap[MII]	R/W	When this bit is set, if the unicast frame has an ARL miss, the frame is flooded only to the MII port. This map is valid only when Ucast_DLF_drop_enable = 1.	0
7:5	RESERVED	RO	Write as 000, ignore when read.	000
4:0	Ucast_DLF_portmap[4:0]	R/W	When is port map is set, if the unicast frame has an ARL miss, the frame is flooded only to the ports that are set in this portmap. This map is valid only when Ucast_DLF_drop_enable = 1.	0x00

PAGE 0X10–0X14, 0X19: PHY PORT REGISTERS

Note: Page 0x10 through 0x14, and 0x19 can not be accessed through Pseudo MDIO interface. Use MDIO PHY address 0x00 through 0x04 to access these registers. These pages can only be accessed by the SPI interface.

Table 102: PHY Port Register Page Summary

Page	Description
0x10	Port 0
0x11	Port 1
0x12	Port 2
0x13	Port 3
0x14	Port 4
0x19	Global Write to all PHYs*

* Writing to Register Page 0x19 affects a write to the corresponding offset of every PHY Port Register page, including the MII Port External PHY Port Register page.

Table 103: Switch Port Registers (Page 0x10–0x14, 0x19)

ADDR	Bits	Description
0x00–0x01	16	"PHY Port Control Register" on page 115
0x02–0x03	16	"PHY Port Status Register" on page 116
0x04–0x07	16	"PHY Identifier Registers" on page 116
0x08–0x09	16	"Auto-Negotiation Advertisement Register" on page 117
0x0A–0x0B	16	"Auto-Negotiation Link Partner (LP) Ability Register" on page 117
0x0C–0x0D	16	"Auto-Negotiation Expansion Register" on page 118
0x0E–0x0F	16	"Auto-Negotiation Next Page Register" on page 118
0x10–0x11	16	"Link Partner Next Page Register" on page 119
0x12–0x1D	–	Reserved
0x1E–0x1F	16	"DPM Register" on page 119
0x20–0x21	16	"100BASE-X Auxiliary Control Register" on page 120
0x22–0x23	16	"100BASE-X Auxiliary Status Register" on page 120
0x24–0x25	16	"100BASE-X Receive Error Counter" on page 121
0x26–0x27	16	"100BASE-X False Carrier Sense Counter" on page 121
0x28–0x2F	–	Reserved
0x30–0x31	16	"Auxiliary Control/Status Register" on page 121
0x32–0x33	16	"Auxiliary Status Summary Register" on page 122
0x34–0x35	16	"DPM Interrupt Register" on page 124
0x36–0x37	16	"Auxiliary Mode 2 Register" on page 124
0x38–0x39	16	"10BASE-T Auxiliary Error and General Status Register" on page 124
0x3A–0x3B	–	Reserved
0x3C–0x3D	16	"Auxiliary Multiple PHY Register" on page 125

Table 103: Switch Port Registers (Page 0x10–0x14, 0x19) (Cont.)

ADDR	Bits	Description
0x3E–0x3F	16	"Broadcom Test Register" on page 125
0x40–0xEF	–	Reserved
0xF0	8	"SPI Data I/O Register" 0 on page 148
0xF1	8	"SPI Data I/O Register" 1 on page 148
0xF2	8	"SPI Data I/O Register" 2 on page 148
0xF3	8	"SPI Data I/O Register" 3 on page 148
0xF4	8	"SPI Data I/O Register" 4 on page 148
0xF5	8	"SPI Data I/O Register" 5 on page 148
0xF6	8	"SPI Data I/O Register" 6 on page 148
0xF7	8	"SPI Data I/O Register" 7 on page 148
0xF8–0xFD	–	Reserved
0xFE	8	"SPI Status Register" on page 148
0xFF	8	"Page Register" on page 148

PHY Port Control Register

Table 104: PHY Port Control Register (Pages 0x10–0x14, 0x19, Address 0x00–0x01)

Bit	Name	R/W	Description	Default
15	Reset	R/W (SC)	• 1 = PHY reset. • 0 = Normal operation	0
14	Loopback	R/W	• 1 = Loopback mode • 0 = Normal operation	0
13	Forced Speed Selection	R/W	• 1 = 100 Mbps • 0 = 10 Mbps	1
12	Auto-negotiation Enable	R/W	• 1 = Auto-negotiation enable • 0 = Auto-negotiation disable	1
11:10	RESERVED	RO	• 0 = Normal operation	0
9	Restart Auto-negotiation	R/W (SC)	• 1 = Restart auto-negotiation process. • 0 = Normal operation	0
8	Duplex Mode	R/W	• 1 = Full-duplex • 0 = Half-duplex	0
7:0	RESERVED	RO	Write as 0x00, ignore when read.	0x00

PHY PORT STATUS REGISTER

Table 105: PHY Port Status Register (Pages 0x10–0x14, 0x19, Address 0x02–0x03)

Bit	Name	R/W	Description	Default
15	100BASE-T4 Capability	RO	0 = Not 100BASE-T4 capable	0
14	100BASE-TX FDX Capability	RO	1 = 100BASE-TX full-duplex capable	1
13	100BASE-TX Capability	RO	1 = 100BASE-TX half-duplex capable	1
12	10BASE-T FDX Capability	RO	1 = 10BASE-T full-duplex capable	1
11	10BASE-T Capability	RO	1 = 10BASE-T half-duplex capable	1
10:6	Reserved	RO	Write as 0x0, ignore when read.	0x0
5	Auto-negotiation Complete	RO	• 1 = Auto-negotiation process is completed. • 0 = Auto-negotiation process is incomplete.	0
4	Reserved	RO	Write as 0, ignore when read.	0
3	Auto-negotiation Capability	RO	• 1 = Auto-negotiation capable • 0 = Not auto-negotiation capable	1
2	Link Status	RO LL	• 1 = Link is up (Link pass state). • 0 = Link is down (Link fail state).	0
1	Jabber Detect	RO LH	• 1 = Jabber condition is detected. • 0 = Jabber condition is not detected.	0
0	Extended Capability	RO	1 = Extended register capable	1

PHY IDENTIFIER REGISTERS

Table 106: PHY Identifier Registers (Pages 0x10–0x14, 0x19, Address 0x04–0x07)

Bit	Name	R/W	Description	Default
15:0	Switch Port Address 00010	RO	PHYID HIGH	0x0143
15:0	Switch Port Address 00011	RO	PHYID LOW	0xBC30

AUTO-NEGOTIATION ADVERTISEMENT REGISTER

Table 107: Auto-Negotiation Advertisement Register (Pages 0x10-0x14, 0x19, Address 0x08–0x09)

Bit	Name	R/W	Description	Default
15	Next Page	R/W	• 1 = Next page operation is supported. • 0 = Next page operation is disabled.	0
14	RESERVED	RO	Write as 0, ignore when read.	0
13	Remote Fault	R/W	1 = Transmit remote fault	0
12:11	Reserved Technologies	RO	Ignore when read.	00
10	Advertise Pause Capability	R/W	1 = Pause operation for full-duplex.	1
9	Advertise 100BASE-T4	R/W	0 = Do not advertise T4 capability.	0
8	Advertise 100BASE-X FDX	R/W	• 1 = Advertise 100BASE-X full-duplex. • 0 = Do not advertise 100BASE-X full-duplex.	1
7	Advertise 100BASE-X	R/W	1 = Advertise 100BASE-X.	1
6	Advertise 10BASE-T FDX	R/W	• 1 = Advertise 10BASE-T full-duplex. • 0 = Do Not Advertise 10BASE-T full-duplex.	1
5	Advertise 10BASE-T	R/W	1 = Advertise 10BASE-T.	1
4:0	Advertise Selector Field	R/W	Fixed value: indicates IEEE 802.3.	00001

AUTO-NEGOTIATION LINK PARTNER (LP) ABILITY REGISTER

Table 108: Auto-Negotiation Link Partner Ability Register (Pages 0x10-0x14, 0x19, Address 0x0A–0x0B)

Blt	Name	R/W	Description	Default
15	LP Next Page	RO	Link partner next page bit.	0
14	LP Acknowledge	RO	Link partner acknowledge bit.	0
13	LP Remote Fault	RO	Link partner remote fault indicator.	0
12:11	Reserved Technologies	RO	Write as 00, ignore when read.	00
10	LP Advertise Pause	RO	Link partner has pause capability.	0
9	LP Advertise 100BASE-T4	RO	Link partner has 100BASE-T4 capability.	0
8	LP Advertise 100BASE-X FDX	RO	Link partner has 100BASE-X FDX capability.	0
7	LP Advertise 100BASE-X	RO	Link partner has 100BASE-X capability.	0
6	LP Advertise 10BASE-T FDX	RO	Link partner has 10BASE-T FDX capability.	0
5	LP Advertise 10BASE-T	RO	Link partner has 10BASE-T capability.	0
4:0	Link Partner Selector Field	RO	Link partner selector field.	0x00

Note: The values contained in the Auto-negotiation Link Partner Ability register are only guaranteed to be valid after auto-negotiation has successfully completed, as indicated by bit 5 of the Switch Port Status Register.

AUTO-NEGOTIATION EXPANSION REGISTER

Table 109: Auto-Negotiation Expansion Register (Pages 0x10-0x14, 0x19, Address 0x0C–0x0D)

Bit	Name	R/W	Description	Default
15:5	RESERVED	RO	Write as 0x000, ignore when read.	0x000
4	Parallel Detection Fault	RO LH	• 1 = Parallel detection fault. • 0 = No parallel detection fault.	0
3	Link Partner Next Page Able	RO	• 1 = Link partner has next page capability. • 0 = Link partner does not have next page capability.	0
2	Next Page Able	RO	• 1 = Next page is enabled. • 0 = Next page capability.	1
1	Page Received	RO	• 1 = New page has been received. • 0 = New page has not been received.	0
0	Link Partner Auto-negotiation Able	RO LH	• 1 = Link partner has auto-negotiation capability. • 0 = Link partner does not have auto-negotiation capability.	0

AUTO-NEGOTIATION NEXT PAGE REGISTER

Table 110: Next Page Transmit Register (Pages 0x10-0x14, 0x19, Address 0x0E–0x0F)

Bit	Name	R/W	Description	Default
15	Next Page	R/W	• 1 = Additional next page(s) follows. • 0 = Last page	0
14	RESERVED	R/W	When writing to this register, preserve the existing value of this field by doing a read/modify write.	0
13	Message Page	R/W	• 1= Message page • 0 = Unformatted page	1
12	Acknowledge 2	R/W	• 1 = Complies with message. • 0 = Cannot comply with message.	0
11	Toggle	RO	• 1 = Previous value of the transmitted link code word equalled logic zero. • 0 = Previous value of the transmitted link code word equalled logic one.	0
10:0	Message/Unformatted Code Field	R/W	–	001h

LINK PARTNER NEXT PAGE REGISTER

Table 111: Link Partner Next Page Register (Pages 0x10-0x14, 0x19, Address 0x10-0x11)

Bit	Name	R/W	Description	Default
15	Next Page	RO	• 1 = Additional next page(s) follows. • 0 = Last page	0
14	RESERVED	RO	When writing to this register, preserve the existing value of this field by doing a read/modify write.	0
13	Message Page	RO	• 1= Message page • 0 = Unformatted page	0
12	Acknowledge 2	RO	• 1 = Complies with message • 0 = Cannot comply with message	0
11	Toggle	RO	• 1 = Previous value of the transmitted link code word equalled logic zero. • 0 = Previous value of the transmitted link code word equalled logic one.	0
10:0	Message/Unformatted Code Field	RO		0x000

DPM REGISTER

Access when Table 123 on page 125 is set.

Table 112: DPM Register (Pages 0x10-0x14, 0x19, Address 0x1E–0x1F)

Bit	Name	R/W	Description	Default
15:11	FLPWIDTH[4:0]	R/W	FLP width increment • 1: increment • 0: Normal	0
10:7	Reserved	RO	Write as 0x0, ignored when read.	0x0
6	DPMCONT: Continuous DPM Detect Enable	R/W	Continuous DPM detect enable • 0 = Stop after detecting a DPM capable link partner. • 1 = Continue detecting a DPM capable link partner.	0
5	Reserved	RO	Write as 0, ignored when read.	0
4	LPXTND: Extend Link Pulse width	R/W	• 0 = Normal link pulse width (100ns). • 1 = Set link pulse width to 150ns.	0
3	MISMTCH: Word mismatch	RO	1 = Fast link pulse word mismatch occurred during DPM detection indicating that the link partner not a DPM link partner.	0
2	DPMSTAT: Status	RO	1 = Link partner is DPM capable.	0
1	ANRSTRT: Restart	R/W	1 = Restart auto-negotiation (identical to register 0 bit 9), but used for DPM detection.	0
0	DPMDETEN: DPM enable	R/W	1 = Enable DPM detection mode.	0

100BASE-X AUXILIARY CONTROL REGISTER

Table 113: 100BASE-X Auxiliary Control Register (Pages 0x10-0x14, 0x19, Address 0x20–0x21)

Bit	Name	R/W	Description	Default
15:14	RESERVED		When writing to this register, preserve the existing value of this field by doing a read/modify write.	10
13	Transmit Disable	R/W	• 1 = Transmitter disabled in PHY. • 0 = Normal operation.	0
12:11	RESERVED	RO	When writing to this register, preserve the existing value of this field by doing a read/modify write.	00
10	Bypass 4B5B Encoder/Decoder	R/W	• 1 = Transmit and receive 5B codes. • 0 = Normal interface.	0
9	Bypass Scrambler/Descrambler	R/W	• 1 = Scrambler and descrambler disabled. • 0 = Scrambler and descrambler enabled.	0
8	Bypass NRZI Encoder/Decoder	R/W	• 1 = NRZI encoder and decoder are disabled. • 0 = NRZI encoder and decoder are enabled.	0
7	Bypass Receive Symbol Alignment	R/W	• 1 = 5B receive symbols not aligned. • 0 = Receive symbols aligned to 5B boundaries.	0
6	Baseline Wander Correction Disable	R/W	• 1 = BASEline wander correction disabled. • 0 = BASEline wander correction enabled.	0
5	FEF Enable	R/W	• 1 = Far-end fault enabled. • 0 = Far-end fault disabled.	0
4:0	RESERVED	R/W	When writing to this register, preserve the existing value of this field by doing a read/modify write.	0x0

100BASE-X AUXILIARY STATUS REGISTER

Table 114: 100BASE-X Auxiliary Status Register (Pages 0x10-0x14, 0x19, Address 0x22–0x23)

Bit	Name	R/W	Description	Default
15:10	RESERVED	RO	When writing to this register, preserve the existing value of this field by doing a read/modify write.	0x00
9	Locked	RO	• 1 = Descrambler locked. • 0 = Descrambler unlocked.	0
8	Current 100BASE-X Link Status	RO	• 1 = Link pass • 0 = Link fail	0
7	Far-end Fault	RO	• 1 = Far-end fault detected. • 0 = No far-end fault detected.	0
6	RESERVED	RO	When writing to this register, preserve the existing value of this field by doing a read/modify write.	0
5	False Carrier Detected	RO LH	• 1 = False carrier detected since last read. • 0 = No false carrier since last read.	0
4	Bad ESD Detected	RO LH	• 1 = ESD error detected since last read. • 0 = No ESD error since last read.	0
3	Receive Error Detected	RO LH	• 1 = Receive error detected since last read. • 0 = No receive error since last read.	0

Table 114: 100BASE-X Auxiliary Status Register (Pages 0x10-0x14, 0x19, Address 0x22–0x23) (Cont.)

Bit	Name	R/W	Description	Default
2	Transmit Error Detected	RO LH	• 1 = Transmit error code received since last read. • 0 = No transmit error code received since last read.	0
1	Lock Error Detected	RO LH	• 1 = Lock error detected since last read. • 0 = No lock error since last read.	0
0	MLT3 Code Error Detected	RO LH	• 1 = MLT3 code error detected since last read. • 0 = No MLT3 code error since last read.	0

100BASE-X Receive Error Counter

Table 115: 100BASE-X Receive Error Counter (Pages 0x10-0x14, 0x19, Address 0x24–0x25)

Bit	Name	R/W	Description	Default
15:0	Receive Error Counter	R/W	Number of non-collision packets with receive errors since last read.	0x00

This counter increments each time the BCM5325E receives a non-collision packet containing at least one receive error. The counter automatically clears itself when read. When the counter reaches its maximum value, 0xFF, it stops counting receive errors until cleared.

100BASE-X False Carrier Sense Counter

Table 116: 100BASE-X False Carrier Sense Counter (Pages 0x10-0x14, 0x19, Address 0x26–0x27)

Bit	Name	R/W	Description	Default
15:8	Reserved	RO	Write as 0x00, Ignore when read.	0x00
7:0	False Carrier Sense Counter	R/W	Number of false carrier sense events since last read.	0x00

This counter increments each time the BCM5325E detects a false carrier on the receive input. The counter automatically clears itself when read. When the counter reaches its maximum value, 0xFF, it stops counting false carrier sense errors until cleared.

Auxiliary Control/Status Register

Table 117: Auxiliary Control/Status Register (Pages 0x10–0x14, 0x19, Address 0x30–0x31)

Bit	Name	R/W	Description	Default
15	Jabber Disable	R/W	• 1= Jabber function disabled in PHY. • 0 = Jabber function enabled in PHY.	0
14	Link Disable	R/W	• 1 = Link integrity test disabled in PHY. • 0 = Link integrity test is enabled in PHY.	0
13:8	Reserved	RO	Write as 0x00, ignore when read.	0x00

Table 117: Auxiliary Control/Status Register (Pages 0x10–0x14, 0x19, Address 0x30–0x31) (Cont.)

Bit	Name	R/W	Description	Default
7:6	HSQ : LSQ	R/W	These two bits define the squelch mode of the 10BASE-T carrier sense mechanism: • 00 = Normal squelch • 01 = Low squelch • 10 = High squelch • 11 = Not allowed	00
5:2	Reserved	RO	Ignore when read.	0xF
1	Speed Indication	RO	• 1 = 100BASE-X • 0 = 10BASE-T	0
0	Full-Duplex Indication	RO	• 1 = Full-duplex active • 0 = Full-duplex not active	0

AUXILIARY STATUS SUMMARY REGISTER

Table 118: Auxiliary Status Summary Register (Pages 0x10–0x14, 0x19, Address 0x32–0x33)

Bit	Name	R/W	Description	Default
15	Auto-negotiation Complete	RO	• 1 = Auto-negotiation process is completed. • 0 = Auto-negotiation process is not completed.	0
14	Auto-negotiation Complete Acknowledge	RO LH	• 1 = Auto-negotiation completed acknowledge state. • 0 = State not entered since last read.	0
13	Auto-negotiation Acknowledge Detected	RO LH	• 1 = Auto-negotiation acknowledge detected. • 0 = State not entered since last read.	0
12	Auto-negotiation Ability Detect	RO LH	• 1 = Entered auto-negotiation ability detect state. • 0 = State not entered since last read.	0
11	Auto-negotiation Pause	RO	• 1 = BCM5325E and link partner pause operation bit set. • 0 = BCM5325E and link partner pause operation bit not set.	0
10:8	Auto-negotiation HCD	RO	• 000 = No highest common denominator • 001 = 10BASE-T • 010 = 10BASE-T full-duplex • 011 = 100BASE-TX • 100 = 100BASE-T4 • 101 = 100BASE-TX full-duplex • 11x = Undefined	000
7	Auto-negotiation Parallel Detection Fault	RO LH	• 1 = Parallel detection fault • 0 = Parallel link fault is not detected.	0
6	Reserved	RO	When writing to this register, preserve the existing value of this field by doing a read/modify write.	0
5	Link Partner Page Received	RO LH	• 1 = New page has been received. • 0 = New page has not been received.	0
4	Link Partner Auto-negotiation Ability	RO	• 1 = Link partner is auto-negotiation capable. • 0 = Link partner does not perform auto-negotiation.	0

Table 118: Auxiliary Status Summary Register (Pages 0x10–0x14, 0x19, Address 0x32–0x33) (Cont.)

Bit	*Name*	*R/W*	*Description*	*Default*
3	Speed Indicator	RO	• 1 = 100 Mbps • 0 = 10 Mbps	0
2	Link Status	RO LL	• 1 = Link is up (link pass state). • 0 = Link is down (link fail state).	0
1	Auto-negotiation Enabled	RO	• 1 = Auto-negotiation is enabled. • 0 = Auto-negotiation is disabled.	1
0	Full Duplex Indication	RO	• 1 = Full-duplex is active. • 0 = Full-duplex is inactive.	0

The Auxiliary Status Summary Register contains copies of redundant status bits found elsewhere within the Switch Port Register space. Descriptions for each of these individual bits can be found associated with their primary register descriptions.

DPM Interrupt Register

Access when Table 123 on page 125 is set.

Table 119: DPM Interrupt Register (Pages 0x10–0x14, 0x19, Address 0x34–0x35)

Bit	Name	R/W	Description	Default
15:13	Reserved	RO	Write as 100, ignored when read.	100
12	DPM Mask	R/W	DPM interrupt mask. When bit is set, DPM will not generate interrupt.	1
11:6	Reserved	RO	Write as 11100, ignored when read.	11100
5	DPM Interrupt	RO LH	DPM interrupt bit	0
4:0	Reserved	RO	Write as 0x00, ignored when read.	0x00

Auxiliary Mode 2 Register

Table 120: Auxiliary Mode 2 (Pages 0x10–0x14, 0x19, Address 0x36–0x37)

Bit	Name	R/W	Description	Default
15:0	Reserved Bits	RO	These are Broadcom reserved bits. Do not write.	–

10BASE-T Auxiliary Error and General Status Register

Table 121: 10BASE-T Auxiliary Error and General Status Register (Pages 0x10–0x14, 0x19, Address 0x38–0x39)

Bit	Name	R/W	Description	Default
15:14	Reserved	RO	Write as 00, ignore when read.	00
13	MDIX Status	RO	• 0 = MDI is in use. • 1 = MDIX is in use.	0
12	MDIX Manual Swap	R/W	• 0 = MDI or MDIX if MDIX is not disabled. • 1 = Force MDIX.	0
11	HP Auto-MDIX disable	R/W	• 0 = HP Auto-MDIX enabled. • 1 = HP Auto-MDIX disabled.	0
10	Manchester Code Error	RO	1 = Manchester code error (10BASE-T).	0
9	EOF Error	RO	1 = EOF detection error (10BASE-T).	0
8	Reserved	RO	When writing to this register, preserve the existing value of this field by doing a read/modify write.	0
7:5	Reserved	RO	When writing to this register, preserve the existing value of this field by doing a read/modify write.	001
4:2	Reserved	RO	When writing to this register, preserve the existing value of this field by doing a read/modify write.	0
1	Speed Indication	RO	• 1 = 100BASE-X • 0 = 10BASE-T	0
0	Full-duplex Indication	RO	• 1 = Full-duplex is active. • 0 = Full-duplex is inactive.	0

All error bits in the Auxiliary Error Status Register are read-only and are latched high. When certain types of errors occur in the BCM5325E, 1 or more corresponding error bits become 1. They remain so until the register is read, or until a chip reset

occurs. All such errors necessarily result in data errors, and are indicated by a high value on the RXER output pin at the time the error occurs.

AUXILIARY MULTIPLE PHY REGISTER

Table 122: Auxiliary Multiple PHY Register (Pages 0x10–0x14, 0x19, Address 0x3C–0x3D)

Bit	Name	R/W	Description	Default
15	HCD_TX_FDX	RO	1 = Auto-negotiation result is 100BASE-TX full-duplex.	0
14	HCD_T4	RO	1 = Auto-negotiation result is 100BASE-T4.	0
13	HCD_TX	RO	1 = Auto-negotiation result is 100BASE-TX.	0
12	HCD_10BASE-T_FDX	RO	1 = Auto-negotiation result is 10BASE-T full-duplex.	0
11	HCD_10BASE-T	RO	1 = Auto-negotiation result is 10BASE-T.	0
10:9	RESERVED	RO	Write as 00, ignore when read.	00
8	Restart Auto-negotiation	R/W (SC)	• 1 = Restart auto-negotiation process. • 0 = (No effect)	0
7	Auto-negotiation Complete	RO	• 1 = Auto-negotiation process completed. • 0 = Auto-negotiation process not completed.	0
6	Acknowledge Complete	RO	1 = Auto-negotiation acknowledge completed.	0
5	Acknowledge Detected	RO	1 = Auto-negotiation acknowledge detected.	0
4	Ability Detect	RO	1 = Auto-negotiation is waiting for LP ability.	0
3	Super Isolate	R/W	• 1 = Super isolate mode • 0 = Normal operation	0
2:0	Reserved	RO	When writing to this register, preserve the existing value of this field by doing a read/modify write.	0x0

BROADCOM TEST REGISTER

Table 123: Broadcom Test (Pages 0x10–0x14, 0x19, Address 0x3E–0x3F)

Bit	Name	R/W	Description	Default
15:8	Reserved	RO	These Broadcom test register bits are reserved and should never be written.	–
7	Shadow register enable	RW	Shadow register enable. • 1 = Enable shadow registers. • 0 = Disable shadow registers. Perform a read, modify and write to change this bit setting.	0
6:0	Reserved	RO	These Broadcom test register bits are reserved and should never be written.	–

PAGE 0X18: MII PORT EXTERNAL PHY REGISTERS

Note: The MII port can be connected to an external PHY. The registers of the external PHY can be read/written via register page 0x18. Information on the External PHY Registers should be obtained from the external PHY data sheet. Data contained in register page 0x18 is obtained by polling the registers of the external PHY via the MDC/MDIO interface. The actual values or meanings of these bits are controlled by the external PHY. The following table maps the external PHY register address to the BCM5325E offset address.

Table 124: MII Port External PHY Registers (Page 0x18)

External PHY Register Address	*Offset Address*	*Bits*	*IEEE Register Name*
0x00	0x00–0x01	16	MII Control Register
0x01	0x02–0x03	16	MII Status Register
0x02–0x03	0x04–0x07	32	PHY Identifier Register
0x04	0x08–0x09	16	Auto-negotiation Advertisement Register
0x05	0x0A–0x0B	16	Auto-negotiation Link Partner Ability Register
0x06	0x0C–0x0D	16	–
0x07	0x0E–0x0F	16	–
0x08	0x10–0x11	16	–
0x09	0x12–0x13	16	–
0x0A	0x14–0x15	16	–
0x0B	0x16–0x17	16	–
0x0C	0x18–0x19	16	–
0x0D	0x1A–0x1B	16	–
0x0E	0x1C–0x1D	16	–
0x0F	0x1E–0x1F	16	–
0x10	0x20–0x21	16	–
0x11	0x22–0x23	16	–
0x12	0x24–0x25	16	–
0x13	0x26–0x27	16	–
0x14	0x28–0x29	16	–
0x15	0x2A–0x2B	16	–
0x16	0x2C–0x2D	16	–
0x17	0x2E–0x2F	16	–
0x18	0x30–0x31	16	–
0x19	0x32–0x33	16	–
0x1A	0x34–0x35	16	–
0x1B	0x36–0x37	16	–
0x1C	0x38–0x39	16	–
0x1D	0x3A–0x3B	16	–
0x1E	0x3C–0x3D	16	–
0x1F	0x3E–0x3F	16	–

Table 124: MII Port External PHY Registers (Page 0x18) (Cont.)

External PHY Register Address	*Offset Address*	*Bits*	*IEEE Register Name*
—	0x51–0xEF		Reserved
—	0xF0	8	SPI Data I/O Register 0
—	0xF1	8	SPI Data I/O Register 1
—	0xF2	8	SPI Data I/O Register 2
—	0xF3	8	SPI Data I/O Register 3
—	0xF4	8	SPI Data I/O Register 4
—	0xF5	8	SPI Data I/O Register 5
—	0xF6	8	SPI Data I/O Register 6
—	0xF7	8	SPI Data I/O Register 7
—	0xF8–0xFD	—	Reserved
—	0xFE	8	SPI Status Register
—	0xFF	8	Page Register

PAGE 0X20–0X24: PORT MIB REGISTERS

Table 125: Port MIB Register Page Summary

Page	Description
0x20	Port 1
0x21	Port 2
0x22	Port 3
0x23	Port 4
0x24	Port 5
0x28	MII port

Table 126: Port MIB Group 0 Registers (Pages 0x20–0x24, 0x28) with Page 0x02, Address 0x04 MIB Mode Select =0

ADDR	Bits	Description
0x00–0x01	16	TxGoodPkts Total number of good packets that are received by this port.
0x02–0x03	16	TxUnicastPkts Total number of good packets transmitted by this port that are addressed to be a unicast address.
0x04–0x05	16	RxGoodPkts Total number of good packets that are received by this port.
0x06–0x07	16	RxUnicastPkts Total number of unicast good packets that are received by this port.
0x08–0xEF	–	Reserved
0xF0	8	"SPI Data I/O Register" 0 on page 148
0xF1	8	"SPI Data I/O Register" 1 on page 148
0xF2	8	"SPI Data I/O Register" 2 on page 148
0xF3	8	"SPI Data I/O Register" 3 on page 148
0xF4	8	"SPI Data I/O Register" 4 on page 148
0xF5	8	"SPI Data I/O Register" 5 on page 148
0xF6	8	"SPI Data I/O Register" 6 on page 148
0xF7	8	"SPI Data I/O Register" 7 on page 148
0xF8–0xFD	–	Reserved
0xFE	8	"SPI Status Register" on page 148
0xFF	8	"Page Register" on page 148

Table 127: Port MIB Group 1 Registers (Pages 0x20–0x24, 0x28) with Page 0x02, Address 0x04 MIB Mode Select =1

ADDR	Bits	Description
0x00–0x01	16	Tx Collisions Total number of collisions experienced by this port during packets transmitted.
0x02–0x03	16	TxOctets Total number of good bytes transmitted by this port.
0x04–0x05	16	RxFCSErrors Total number of packets received by this port have a length between 64 and 1522 bytes inclusive and have a bad FCS within integral number of bytes.
0x06–0x07	16	RxGoodOctets Total number of bytes in all good packets received by this port.
0x08–0xEF	–	Reserved
0xF0	8	"SPI Data I/O Register" 0 on page 148
0xF1	8	"SPI Data I/O Register" 1 on page 148
0xF2	8	"SPI Data I/O Register" 2 on page 148
0xF3	8	"SPI Data I/O Register" 3 on page 148
0xF4	8	"SPI Data I/O Register" 4 on page 148
0xF5	8	"SPI Data I/O Register" 5 on page 148
0xF6	8	"SPI Data I/O Register" 6 on page 148
0xF7	8	"SPI Data I/O Register" 7 on page 148
0xF8–0xFD	–	Reserved
0xFE	8	"SPI Status Register" on page 148
0xFF	8	"Page Register" on page 148

PAGE 0X30: QOS REGISTERS

Table 128: QoS Registers (Page 0x30)

ADDR	Bits	Description
0x00–0x01	16	"QoS Control Register (Page 0x30: Address 0x00–0x01)" on page 131
0x02	8	"QoS Priority Queue Control Register (Page 0x30: Address 0x02)" on page 131
0x03	–	Reserved
0x04–0x05	16	"QoS IEEE 802.1P Enable Register (Page 0x30: Address 0x04–0x05)" on page 132
0x06–0x07	16	"QoS Diff-Serv Enable Register (Page 0x30: Address 0x06–0x07)" on page 132
0x08–0x12	–	Reserved
0x13–0x14	16	"QoS Pause Enable Register (Page 0x30: Address 0x13–0x14)" on page 133
0x15–0x16	16	"IEEE 802.1P Priority Threshold Register (Page 0x30: Address 0x15–0x16)" on page 133
0x17–0x2F	–	Reserved
0x30–0x37	8x8	"DiffServ DSCP Priority Register (Page 0x30: Address 0x30–0x37)" on page 134
0x37–0x3F	8x8	"DiffServ DSCP Priority Register (Page 0x30: Address 0x38–0x3F)" on page 134
0x40–0xFE	–	Reserved
0xF0	8	"SPI Data I/O Register" 0 on page 148
0xF1	8	"SPI Data I/O Register" 1 on page 148
0xF2	8	"SPI Data I/O Register" 2 on page 148
0xF3	8	"SPI Data I/O Register" 3 on page 148
0xF4	8	"SPI Data I/O Register" 4 on page 148
0xF5	8	"SPI Data I/O Register" 5 on page 148
0xF6	8	"SPI Data I/O Register" 6 on page 148
0xF7	8	"SPI Data I/O Register" 7 on page 148
0xF8–0xFD	–	Reserved
0xFE	8	"SPI Status Register" on page 148
0xFF	8	"Page Register" on page 148

QoS Control Register

Table 129: QoS Control Register (Page 0x30: Address 0x00–0x01)

Bit	Name	R/W	Description	Default
15	CPU Control Enable	R/W	QoS software control enable • 1 = Software controls QoS settings • 0 = Reserved (not used) Software control is the only way to change QoS settings.	1
14:12	RESERVED	RO	Write as 00, ignore when read.	00
11:10	TXQ_MODE	R/W	Transmit queue mode These bits control the number of QoS transmit queues. • 00: Single-queue (No QoS) • 01: Two-queue mode (Queue [0:1]) • 10: Three-queue mode (Queue [0:2]) • 11: Four-queue mode (Queue [0:3]) The CPU Control enable bit (bit 15) is must be set.	00
9:0	Port-Based QOS	RO	Port-based QoS enable Setting this bit enables port-based QoS on the corresponding port. The port-based priority is the assigned the highest transmit queue. Bit(s): • 0–4: 10/100BASE-T ports • 5–7 Reserved. • 8: MII Port. • 9: CPU port. The CPU control enable bit is must be set.	0x00

For more information, see "QoS" on page 3.

QoS Priority Queue Control Register

Table 130: QoS Priority Queue Control Register (Page 0x30: Address 0x02)

Bit	Name	R/W	Description	Default
7:3	Reserved	RO	Write as 0x00, ignore when read.	0x00
2	QOS_Layer_Sel	R/W	QOS layer select • 1 = Diff-Serv has higher priority. • 0 = IEEE 802.1P has higher priority. The CPU control enable bit is must be set.	1
1:0	Reserved	RO	Write as 00, ignore when read.	00

For more information, see "QoS" on page 3.

QoS IEEE 802.1P Enable Register

Table 131: QoS IEEE 802.1P Enable Register (Page 0x30: Address 0x04–0x05)

Bit	Name	R/W	Description	Default
15:10	Reserved	RO	Write as 00000, ignore when read.	00000
9:0	QOS_1P_EN	R/W	IEEE 802.1P QOS enable Bit(s): • 0–4: 10/100BASE-T ports • 5–7: Reserved • 8: MII port • 9: CPU port The CPU control enable bit is must be set.	0x3FF

For more information, see "QoS" on page 3.

QoS Diff-Serv Enable Register

Table 132: QoS Diff-Serv Enable Register (Page 0x30: Address 0x06–0x07)

Bit	Name	R/W	Description	Default
15:10	Reserved	RO	Write as 00000, ignore when read.	00000
9:0	DIFF-SERV_EN	R/W	Diff-serv enable Bit(s): • 0–4: 10/100BASE-T ports • 5–7: Reserved • 8: MII port • 9: CPU port The CPU control enable bit is must be set.	0x000

For more information, see "QoS" on page 3.

QoS Pause Enable Register

Table 133: QoS Pause Enable Register (Page 0x30: Address 0x13–0x14)

Bit	Name	R/W	Description	Default
15:10	Reserved	RO	Write as 00000, ignore when read.	00000
9:0	QoS Pause Enable Bit	R/W	QoS pause enable Setting this bit to 1 enables flow control measures on the corresponding port. Bit(s): • 0–4: 10/100BASE-T ports • 5–7: Reserved • 8: MII port The CPU control enable bit is must be set.	0x000

For more information, see “QoS” on page 3.

IEEE 802.1P Priority Threshold Register

Table 134: IEEE 802.1P Priority Threshold Register (Page 0x30: Address 0x15–0x16)

Bit	Name	R/W	Description	Default
15:14	IEEE 802.1P Priority TAG 111	R/W	These 2 bits are used to assign priority queue of tag 111.	11
13:12	IEEE 802.1P Priority TAG 110	R/W	These 2 bits are used to assign priority queue of tag 110.	11
11:10	IEEE 802.1P Priority TAG 101	R/W	These 2 bits are used to assign priority queue of tag 101.	10
9:8	IEEE 802.1P Priority TAG 100	R/W	These 2 bits are used to assign priority queue of tag 100.	10
7:6	IEEE 802.1P Priority TAG 011	R/W	These 2 bits are used to assign priority queue of tag 011.	01
5:4	IEEE 802.1P Priority TAG 010	R/W	These 2 bits are used to assign priority queue of tag 010.	01
3:2	IEEE 802.1P Priority TAG 001	R/W	These 2 bits are used to assign priority queue of tag 001.	00
1:0	IEEE 802.1P Priority TAG 000	R/W	These 2 bits are used to assign priority queue of tag 000.	00

CPU Control Enable bit is must be set. For more information, see “QoS” on page 3.

DIFFSERV DSCP PRIORITY REGISTER

Reg 0x30 to reg 0x3F are used to assign a 2-bit priority to the each corresponding DiffServ priority. The following table defines a few entries. The rest of the traffic classes are the same format as in Table 135.

Table 135: DiffServ DSCP Priority Register (Page 0x30: Address 0x30–0x37)

Address	Bit	Name	R/W	Description	Default
0x37	63:62	Priority of DSCP = 011111	R/W	See description above.	00
	61:60	Priority of DSCP = 011110	R/W	See description above.	00
	59:58	Priority of DSCP = 011101	R/W	See description above.	00
	57:56	Priority of DSCP = 011100	R/W	See description above.	00
0x36–0x31	.....	.....	R/W	.....	0's
0x30	7:6	Priority of DSCP = 000011	R/W	See description above.	00
	5:4	Priority of DSCP = 000010	R/W	See description above.	00
	3;2	Priority of DSCP = 000001	R/W	See description above.	00
	1:0	Priority of DSCP = 000000	R/W	See description above.	00

Table 136: DiffServ DSCP Priority Register (Page 0x30: Address 0x38–0x3F)

Address	Bit	Name	R/W	Description	Default
0x3F	63:62	Priority of DSCP = 111111	R/W	See description above.	00
	61:60	Priority of DSCP = 111110	R/W	See description above.	00
	61:60	Priority of DSCP = 111101	R/W	See description above.	00
	61:60	Priority of DSCP = 111100	R/W	See description above.	00
0x3E–0x39	.....	.....	R/W	.....	0's
0x38	7:6	Priority of DSCP = 100011	R/W	See description above.	00
	5:4	Priority of DSCP = 100010	R/W	See description above.	00
	3;2	Priority of DSCP = 100001	R/W	See description above.	00
	1:0	Priority of DSCP = 100000	R/W	See description above.	00

For more information, see "QoS" on page 3.

PAGE 0X31: PORT-BASE VLAN REGISTERS

Table 137: Page 0x31 VLAN Registers

Address	Bits	Description
0x00–0x01	16	"Port-Based VLAN Control Register" Port 0 on page 135
0x02–0x03	16	"Port-Based VLAN Control Register" Port 1 on page 135
0x04–0x05	16	"Port-Based VLAN Control Register" Port 2 on page 135
0x06–0x07	16	"Port-Based VLAN Control Register" Port 3 on page 135
0x08–0x09	16	"Port-Based VLAN Control Register" Port 4 on page 135
0x0A–0x0F	–	Reserved
0x10–0x11	16	"Port-Based VLAN Control Register" MII Port on page 135
0x12–0x13	16	"Port-Based VLAN Control Register" Serial Port on page 135
0x14–0xFE	–	Reserved
0xF0	8	"SPI Data I/O Register" 0 on page 148
0xF1	8	"SPI Data I/O Register" 1 on page 148
0xF2	8	"SPI Data I/O Register" 2 on page 148
0xF3	8	"SPI Data I/O Register" 3 on page 148
0xF4	8	"SPI Data I/O Register" 4 on page 148
0xF5	8	"SPI Data I/O Register" 5 on page 148
0xF6	8	"SPI Data I/O Register" 6 on page 148
0xF7	8	"SPI Data I/O Register" 7 on page 148
0xF8–0xFD	–	Reserved
0xFE	8	"SPI Status Register" on page 148
0xFF	8	"Page Register" on page 148

PORT-BASED VLAN CONTROL REGISTER

Table 138: Port VLAN Control Register Serial, MII, Ports[0:4] (Page 31h, Address 0x00-0x09, 0x10-0x13)

Bit	Name	R/W	Description	Default
15:9	RESERVED	RO	—	
8:0	FORWARD_MASK	R/W	VLAN forwarding mask Bits [8, 4:0] correspond to the MII port and ports [4:0], respectively. • 0: Disable VLAN forwarding to egress port. • 1: Enable VLAN forwarding to egress port.	FFh

PAGE 0X34: IEEE 802.1Q VLAN REGISTERS

Table 139: IEEE 802.1Q VLAN Registers (Page 0x34)

ADDR	Bits	Description
0x00	8	"IEEE 802.1Q VLAN Control 0 Register" on page 137
0x01	8	"IEEE 802.1Q VLAN Control 1 Register" on page 137
0x02	8	"IEEE 802.1Q VLAN Control 2 Register" on page 138
0x03	8	"IEEE 802.1Q VLAN Control 3 Register" on page 139
0x04	8	"IEEE 802.1Q VLAN Control 4 Register" on page 140
0x05	8	"IEEE 802.1Q VLAN Control 5 Register" on page 141
0x06–0x07	16	"IEEE 802.1Q VLAN Table Access Register" on page 142
0x08–0x0B	32	"IEEE 802.1Q VLAN Write Register" on page 142
0x0C–0x0F	32	"IEEE 802.1Q VLAN Read Register" on page 143
0x10–0x1D	16/port	"IEEE 802.1Q Default Port TAG Register" on page 144
0x1E–0x1F	–	Reserved
0x20–0x22	16	"Priority Re-Map Register" on page 145
0x23–0xEF	–	Reserved
0xF0	8	"SPI Data I/O Register" 0 on page 148
0xF1	8	"SPI Data I/O Register" 1 on page 148
0xF2	8	"SPI Data I/O Register" 2 on page 148
0xF3	8	"SPI Data I/O Register" 3 on page 148
0xF4	8	"SPI Data I/O Register" 4 on page 148
0xF5	8	"SPI Data I/O Register" 5 on page 148
0xF6	8	"SPI Data I/O Register" 6 on page 148
0xF7	8	"SPI Data I/O Register" 7 on page 148
0xF8–0xFD	–	Reserved
0xFE	8	"SPI Status Register" on page 148
0xFF	8	"Page Register" on page 148

IEEE 802.1Q VLAN CONTROL 0 REGISTER

Table 140: IEEE 802.1Q VLAN Control 0 Register (Page: 0x34, Address 0x00)

Bit	Name	R/W	Description	Default
7	EN_1QVLAN	RW	IEEE 802.1Q VLAN enable • 0 = Disable IEEE 802.1Q VLAN. • 1 = Enable IEEE 802.1Q VLAN. See "Programming the VLAN Table" on page 7 for more information.	0
6:5	VLAN Learning Mode	RW	• 00 = SVL (Shared VLAN Learning Mode), MAC is used to hash ARL table. • 11 = IVL (Individual VLAN Learning Mode), MAC and VID are used to hash ARL table. • 10 = Illegal • 01 = Illegal For more information, see "Address Table Organization" on page 23.	1
4	Reserved	RO	Write as 0, ignore when read.	0
3:2	IEEE 802.1Q FRAME Control	RW	• 00 = Forward frame as is. • 01 = Modify priority bits according to priority re-map register (4 bits). • 10 = Replace VID with the port's default VID (12 bits). • 11 = Replace both priority and VID (16 bits).	00
1:0	Reserved	RO	Write as 0, ignore when read.	0

For more information, see below.

IEEE 802.1Q VLAN CONTROL 1 REGISTER

Table 141: IEEE 802.1Q VLAN Control 1 Register (Page: 0x34, Address 0x01)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Write as 0, ignore when read.	0
6	Enable IPMC Bypass V Untagmap	RW	When asserted will not check the IP multicast (IPMC) frame with the VLAN's untagmap.	0
5	Enable IPMC Bypass V Fwdmap	RW	When asserted will not check IPMC frame with the VLAN's forward map.	0
4	Enable IPMC Bypass V Taging	RW	When asserted will not tag IP multicast frame.	0
3	Enable RSV Multicast V Untagmap	RW	When asserted, reserved multicast frames (except GMRP and GVRP) are checked by the VLAN's untagmap.	0
2	Enable RSV Multicast V Fwdmap	RW	When asserted, reserved multicast frames (except GMRP and GVRP) are checked by the VLAN's forward map.	0
1	Enable RSV Multicast V Tagging	RW	When asserted, reserved multicast frames (except GMRP and GVRP) are tagged according to VLAN rules.	0
0	Enable Special Entry VLAN Check	RW	When detecting a multiport MAC address, ARL checking is bypassed. The register provides the forwarding map. • 1 = Two special entries (group0 and group1) address frames follow 2 VLAN rules. (tagging, v_untagmap). • 0 = Bypass all VLAN checking (tagging, v_fwdmap, v_untagmap).	0

IEEE 802.1Q VLAN CONTROL 2 REGISTER

Table 142: IEEE 802.1Q VLAN Control 2 Register (Page: 0x34, Address 0x02)

Bit	*Name*	*R/W*	*Description*	*Default*
7	Enable Remap Priority Field	RW	When asserted, the priority field (3 bits) in ingress frame (IEEE 802.1Q frame or priority tagged frame) is remapped to a new value based on re_map_reg[23:0]. The CFI bit is preserved as original frame. ** When enable this feature, Global Control 0[1:0] has to be either 01, or 11.and Global Control 0[3:2] has to be either 01, or 11. The frame management port does not support VLAN tagging or untagging. So they can not support priority remap.	0
6	en_GMRP_GVRP_untagmap	RW	When set to 1, r GMRP,GVRP are checked by the VLAN's untag map. Does not apply to management port.	0
5	en_GMRP_GVRP_v_fwdmap	RW	When set to 1, GMRP,GVRP are checked by the VLAN's forward map. Does not apply to management port.	0
4	en_GMRP_GVRP_v_tagging	RW	When set to 1, GMRP,GVRP frames are tagged according to VLAN rule. Does not apply to management port.	0
3	en_manage_bypass_V untag map	RW	When set to 1, frames received by MII port bypass the VLAN's untag map.	0
2	en_manage_bypass_V fwd map	RW	When set to 1, frames received by MII port bypass the VLAN's forward map checking. Untagged frame received by Manage port won't be tagged.	0
1	en_SPI_bypass_V_untag map	RW	When set to 1, frames received by SPI port bypass the VLAN's untag map.	0
0	en_SPI_bypass_V_fwd map	RW	When set to 1, frames received by SPI port bypass the VLAN's forward map checking. ** Untagged frame received by SPI port will not be tagged.	0

IEEE 802.1Q VLAN CONTROL 3 REGISTER

Table 143: IEEE 802.1Q VLAN Control 3 Register (Page: 0x34, Address 0x03)

Bit	Name	R/W	Description	Default
7	8BIT_CHECK	RW	High order 8-bit VLAN table check enable If this bit is set the high order 8-bits of the VLAN ID of IEEE 802.1Q, tagged incoming frames are checked against the high order 8-bits contained in the indexed VLAN table entry. If this bit is not set, the 8-bits of the incoming frame are checked against high order bits currently contained in the HIGH8_VID of the "IEEE 802.1Q VLAN Write Register" on page 142.	0
6	Maxsize_1532	RW	This register has effect only when std_ovsz_drop = 1. If maxsize_1532 = 0, the maximum frame size is 1518B (incoming frame is untagged) or 1522B (incoming frame is tagged), so drop frames greater than 1518B (untagged) or 1522B (tagged). This complies to IEEE 802. If maxsize_1532 = 1, the maximum frame size is 1532B (incoming frame is untagged) or 1536B (incoming frame is tagged), so drop frames greater than 1532B (untagged) or 1536B (tagged). Although this does not complies to IEEE 802, it is used to accommodate special frame formats such as double tagging or custom frame header.	0
5	Enable drop non_1Q frame	RW	For MII port. Only apply to MII as non_management port (no CPU on MII).	0
4:0	Enable Drop Non 1Q Frame for port	RW	When enabled, any non_1Q frame is dropped by this port. Ports 5–1, respectively	0

For more information, see "IEEE 802.1Q VLAN" on page 6.

IEEE 802.1Q VLAN CONTROL 4 REGISTER

Table 144: IEEE 802.1Q VLAN Control 4 Register (Page: 0x34, Address 0x04)

Bit	*Name*	*R/W*	*Description*	*Default*
7:6	Ingress_VID_check	RW	These bits apply for ingress frames with a tagged VID found in the VLAN table, but the port itself is not a member of that VLAN. • 00 = Forward ingress VID violation frame (VID is not in the VLAN forward map), but do not learn in ARL table. • 01 = Drop frame if it has VID violation. • 10 = Do not check ingress VID violation. ***Note:*** Does not apply to the management port.	0
5	Enablemanage_receive_GVPPort	RW	When set to 1, management port (the port with CPU) is the destination port of GVRP frame.	0
4	Enablemanage_receive_GMRPort	RW	When set to 1, management port (the port with CPU) is the destination port of GMRP frame.	0
3	Enable un_tagged frame by_pass tagging	RW	When set to 1, un_tagged frame will not be tagged (it still is checked by the forward and untag maps). When set to 0, untagged frame is tagged and checked with forward and untag maps. Does not apply to management port.	0
2	std_ovsz_drop		If std_ovsz_drop = 0 (default), drop frames greater than 1536B (tagged or untagged). Although an untagged frame may become 1540B after internally tagged, it is not dropped (previously such a frame was dropped which was wrong). If std_ovsz_drop = 1, drop frames greater than 1518B untagged/1522B tagged (This complies to IEEE 802). If maxsize_1532 = 1 && std_ovsz_drop = 1, drop frames greater than 1532B untagged/1536B tagged.	
1	std_mib_mode		If 0, use 1522B as the max frame length for MIB counters. The TX Octet count will not subtract 4 bytes even when the frame gets untagged at the TX port.If 1, Use the standard 1518B untagged/1522B tagged as the maximum frame length for MIB counters. The TX Octet count subtracts 4 bytes when the frame gets untagged at the TX port.	
0	use_org_frame_leng		If 0, the frame length used by good frame check and MIB counters is the original frame length with 4B added when the incoming frame is undated and IEEE 802.1Q is enabled. If 1, the frame length used by good frame check and MIB counters is the original frame length regardless whether or not the incoming frame is tagged or IEEE 802.1Q is enabled.	

IEEE 802.1Q VLAN CONTROL 5 REGISTER

Table 145: IEEE 802.1Q VLAN Control 5 Register (Page: 0x34, Address 0x05)

Bit	Name	R/W	Description	Default
7:6	Reserved		Ignored on read.	000
5	VID high 8-bit not checked	RW	This register disables checking the high 8-bits of the VID of incoming frames. • 1 = The high 8-bits of the VID of incoming frames are not checked. The VID[11:4] of frames is not compared against the value of VID[11:4] in Table 146: "IEEE 802.1Q VLAN Table Access Register (Page: 0x34, Address 0x06–0x07)," on page 142 and VID comparison is only performed in the lower 4 bits of the VID. • 0 = The high 8-bits of the VID of incoming frames are checked against the value of VID[11:4] inTable 146: "IEEE 802.1Q VLAN Table Access Register (Page: 0x34, Address 0x06–0x07)," on page 142 as well as the lower 4 bits of the VID.	0
4	Apply bypass VLAN Forward map rule to port-based VLAN	RW	• 1 = VLAN forward map rule apply to port-based VLAN. • 0 = VLAN forward map rule not apply to port-based VLAN.	0
3	drop_Vtable_miss	RW	This bit applies to ingress frames tagged with a VID not found in the VLAN table. If the DA is not found in the ARL table, this bit controls the what happens to the frame. • 0 = Ingress frame with VLAN table miss is flooded to all ports. • 1 = Ingress frame with VLAN table miss is dropped.	0
2	RESERVED	RW	Ignored on read.	0
1	en_manage_rx_ bypass_crcchk	RW	When set to: • 1 = The management port with a CPU on it ignores any CRC (BRCM tag frame, or Ethernet frame). • 0 = The management port checks in both inner and outer CRCs.	0
0	Enable tx port CRC generation	RW	When en_1QVLAN = 0 (default = 0) • 1 = TX port regenerates CRC even when en_1QVLAN = 0. • 0 = TX port does not regenerate CRC when en_1QVALN = 0.	0

For more information, see "IEEE 802.1Q VLAN" on page 6.

IEEE 802.1Q VLAN TABLE ACCESS REGISTER

Table 146: IEEE 802.1Q VLAN Table Access Register (Page: 0x34, Address 0x06–0x07)

Bit	Name	R/W	Description	Default
15:14	Reserved	RO	Ignored on read.	00
13	START/DONE	R/W SC	Start/done command Write as 1 to initiate a read/write command to the VLAN table. This bit returns to 0 to indicate that the read/write operation is completed.	0
12	Read/Write State	RW	VLAN table read/write bit • 1 = Write State • 0 = Read State	0
11:4	HIGH8_VID	RW	High order 8-bits of VLAN ID The bits represent the higher order bits of VLAN ID. These are programmed into the VLAN table entry and checked against the corresponding bits of incoming frames. For more information, see 8BIT_CHECK bit of the "IEEE 802.1Q VLAN Control 3 Register" on page 139.	0xFF
3:0	LOW4_VID	RW	Lower order 4-bits of VLAN ID The bits represent the lower order bits of VLAN ID and are used to index the entry in the VLAN table.	0xF

For more information, see "IEEE 802.1Q VLAN" on page 6.

IEEE 802.1Q VLAN WRITE REGISTER

Table 147: IEEE 802.1Q VLAN Write Register (Page: 0x34, Address 0x08–0x0B)

Bit	Name	R/W	Description	Default
31:21	Reserved	RO	Ignored on read.	0
20	Valid	R/W	• 1 = Valid write • 0 = Invalid write	0
19:12	High 8-bit VID	RW	The bit [11:4] of VLAN ID	0x00
11	MII Port UnTAG enable	RW	• 1 = Untag transmit packet via MII Port. • 0 = Keep outgoing packet intact.	0
10	Port 4 UnTAG enable	RW	• 1 = Untag transmit packet via port 4. • 0 = Keep outgoing packet intact.	0
9	Port 3 UnTAG enable	RW	• 1 = Untag transmit packet via port 3. • 0 = Keep outgoing packet intact.	0
8	Port 2 UnTAG enable	RW	• 1 = Untag transmit packet via port 2. • 0 = Keep outgoing packet intact.	0
7	Port 1 UnTAG enable	RW	• 1 = Untag transmit packet via port 1. • 0 = Keep outgoing packet intact.	0
6	Port 0 UnTAG enable	RW	• 1 = Untag transmit packet via port 0. • 0 = Keep outgoing packet intact.	0
5	MII Port VLAN Group	RW	• 1 = MII Port is one of the assigned VID group. • 0 = MII Port is not one of the assigned VID group.	0

Table 147: IEEE 802.1Q VLAN Write Register (Page: 0x34, Address 0x08–0x0B) (Cont.)

Bit	Name	R/W	Description	Default
4	Port 4 VLAN Group	RW	• 1 = Port 4 is one of the assigned VID group. • 0 = Port 4 is not one of the assigned VID group.	0
3	Port 3 VLAN Group	RW	• 1 = Port 3 is one of the assigned VID group. • 0 = Port 3 is not one of the assigned VID group.	0
2	Port 2 VLAN Group	RW	• 1 = Port 2 is one of the assigned VID group. • 0 = Port 2 is not one of the assigned VID group.	0
1	Port 1 VLAN Group	RW	• 1 = Port 1 is one of the assigned VID group. • 0 = Port 1 is not one of the assigned VID group.	0
0	Port 0 VLAN Group	RW	• 1 = Port 0 is one of the assigned VID group. • 0 = Port 0 is not one of the assigned VID group.	0

For more information, see "IEEE 802.1Q VLAN" on page 6.

IEEE 802.1Q VLAN Read Register

Table 148: IEEE 802.1Q VLAN Read Register (Page: 0x34, Address 0x0C–0x0F)

Bit	Name	R/W	Description	Default
31:21	Reserved	RO	Ignored on read	0
20	Valid	RW	Valid Bit	0
19:12	High 8-bit VID	RW	The bit [11:4] of VLAN ID	0x000
11:6	UnTAGGed Ports	RW	The content of the VLAN entry of the corresponding assigned VID. Shown the untagged port of the specific VID. • Bits 6:10 = 10/100BASE-T Ports • Bit 11 = MII Port	0
5:0	VLAN Ports	RO	The content of the VLAN entry of the corresponding assigned VID. Shown which port belongs to the specific VID. • Bits 0:4 = 10/100BASE-T Ports • Bit 5 = MII Port	0

For more information, see "IEEE 802.1Q VLAN" on page 6.

IEEE 802.1Q DEFAULT PORT TAG REGISTER

Table 149: Default IEEE 802.1Q Tag Register Address Summary

Address	Description
10h–11h	Port 0
12h–13h	Port 1
14h–15h	Port 2
16h–17h	Port 3
18h–19h	Port 4
1Ah–1Bh	MII port
1Ch–1Dh	SPI port

Table 150: Default IEEE 802.1Q Tag Register (Page 34h, Address 10h–1Dh)

Bit	Name	R/W	Description	Default
15:13	DEFAULT_PRI/ PORT_QOS_PRI	R/W	**Default IEEE 802.1Q priority** If an IEEE 802.1Q tag is to be added to an incoming non-IEEE 802.1Q frame, these bits are the default priority value for the new tag. See "Port-Based VLAN" on page 5"for more information. **Port-based QoS priority map bits** When port-based QoS is enabled in the "QoS Control Register" on page 131, these bits represent the Priority ID for the ingress port. The Priority ID determines the TX Queue for each frame based on the "IEEE 802.1P Priority Threshold Register" on page 133.	000
12	CFI	R/W	Conical form indicator	0
11:0	DEFAULT_VID	R/W	**Default IEEE 802.1Q VLAN ID** If an IEEE 802.1Q tag is to be added to an incoming non-IEEE 802.1Q frame, these bits will be the default VID for the new tag. See "Port-Based VLAN" on page 5 for more information.	001

For more information, see "IEEE 802.1Q VLAN" on page 6.

PRIORITY RE-MAP REGISTER

Table 151: Priority Re-Map Register (Page: 0x34, Address 0x20–0x22)

Bit	*Name*	*R/W*	*Description*	*Default*
23:0	Priority Re-Map register	R/W	When 1) global_1Q_control1[8]=1 and 2) control0[0] = 1 and 3) control0[2] = 1. The device remaps the original frames's priority to the one in re_map_reg[23:0]. The mapping rules are: **OLD PRI** **NEW PRI** 000 re_map_reg[2:0] 001 re_map_reg[5:3] 010 re_map_reg[8:6] 011 re_map_reg[11:9] 100 re_map_reg[14:12] 101 re_map_reg[17:15] 110 re_map_reg[20:18] 111 re_map_reg[23:21] ** If incoming frame is pri_tagged frame, or tagged frame, the device is remapped it's priority field if remapping feature is enabled. ** If incoming frame is an un-tagged frame, the device uses priority in Default Port Tag Register as new priority.	

PAGE 0X35: MULTICAST/BROADCAST/DLF SUPPRESSION REGISTER

Table 152: Multicast /Broadcast /DLF Suppression Register (Page 0x35)

ADDR	Bits	Description
0x00	8	"Rate Control Register" Port 0 on page 147.
0x01	8	"Rate Control Register" Port 1 on page 147.
0x02	8	"Rate Control Register" Port 2 on page 147.
0x03	8	"Rate Control Register" Port 3 on page 147.
0x04	8	"Rate Control Register" Port 4 on page 147.
0x05–0xFE		Reserved
0xF0	8	"SPI Data I/O Register" 0 on page 148
0xF1	8	"SPI Data I/O Register" 1 on page 148
0xF2	8	"SPI Data I/O Register" 2 on page 148
0xF3	8	"SPI Data I/O Register" 3 on page 148
0xF4	8	"SPI Data I/O Register" 4 on page 148
0xF5	8	"SPI Data I/O Register" 5 on page 148
0xF6	8	"SPI Data I/O Register" 6 on page 148
0xF7	8	"SPI Data I/O Register" 7 on page 148
0xF8–0xFD	–	Reserved
0xFE	8	"SPI Status Register" on page 148
0xFF	8	"Page Register" on page 148

RATE CONTROL REGISTER

Table 153: Rate Control Register (Page: 0x35, Address 0x00–0x04)

Bit	Name	R/W	Description	Default
7	Drop Frame	RO/ SC	Dropped Frames Indicator When Broadcast/Multicast/DLF frames are dropped this bit is set. It is cleared after read.	0
6	Rate Control Multicast	RW	Multicast Rate Control Enable • 0 = Disable Multicast Rate Control. • 1 = Enable Multicast Rate Control.	0
5	Rate Control Broadcast	RW	Broadcast Rate Control Enable • 0 = Disable Broadcast Rate Control. • 1 = Enable Broadcast Rate Control.	0
4	Rate Control DLF	RW	DLF Rate Control Enable. • 0 = Disable DLF Rate Control. • 1 = Enable DLF Rate Control.	0
3:2	Bucket Size	RW	Rate Control Bucket Size • 00 = 2*1024 bytes • 01 = 4*1024 bytes • 10 = 6*1024 bytes • 11 = 8*1024 bytes	00
1:0	Rate Percentage	RW	Rate Control Rate Percentage These bits set the maximum combined rate for rate controlled packet types. Rate is based on the percentage of port line rate. • 00 = 10% Multicast/Broadcast/DLF • 01 = 20% Multicast/Broadcast/DLF • 10 = 30% Multicast/Broadcast/DLF • 11 = 40% Multicast/Broadcast/DLF	00

For more information, see “Rate Control” on page 8.

GLOBAL REGISTERS

Table 154: Global Registers (Maps to All Pages)

Address	Bits	Description
0xF0	8	"SPI Data I/O Register" 0 on page 148
0xF1	8	"SPI Data I/O Register" 1 on page 148
0xF2	8	"SPI Data I/O Register" 2 on page 148
0xF3	8	"SPI Data I/O Register" 3 on page 148
0xF4	8	"SPI Data I/O Register" 4 on page 148
0xF5	8	"SPI Data I/O Register" 5 on page 148
0xF6	8	"SPI Data I/O Register" 6 on page 148
0xF7	8	"SPI Data I/O Register" 7 on page 148
0xF8–0xFD	–	Reserved
0xFE	8	"SPI Status Register" on page 148
0xFF	8	"Page Register" on page 148

SPI DATA I/O REGISTER

Table 155: SPI Data I/O Register (Maps to All Registers, Address 0xF0-0xF7)

Bit	Name	R/W	Description	Default
7:0	SPI Data I/O	R/W	SPI data bytes[7:0]	

SPI STATUS REGISTER

Table 156: SPI Status Register (Maps to All Registers, Address 0xFE)

Bit	Name	R/W	Description	Default
7	SPIF	RO	SPI Read/Write Complete Flag.	0
6	WCOL	RO	SPI Write Collision	0
5	RACK	RO (SC)	SPI Read Data Ready Acknowledgement (Self-Clearing).	0
4:3	RESERVED	RO	Write as 000, ignore when read.	0
2	MDIO Start	RO	Start/Done MDC/MDIO operation	0
1	RXRDY	RO	SPI Rx Ready Flag—should check every 8 bytes.	0
0	TXRDY	RO	SPI Tx Ready Flag—should check every 8 bytes.	0

PAGE REGISTER

Table 157: Page Register (Maps to All Registers, Address 0xFF)

Bit	Name	R/W	Description	Default
7:0	PAGE_REG	R/W	Binary value determines the value of the accessed register page.	0

Section 7: Timing Characteristics

RESET AND CLOCK TIMING

The following specifies timing information regarding the Reset and Clock pins.

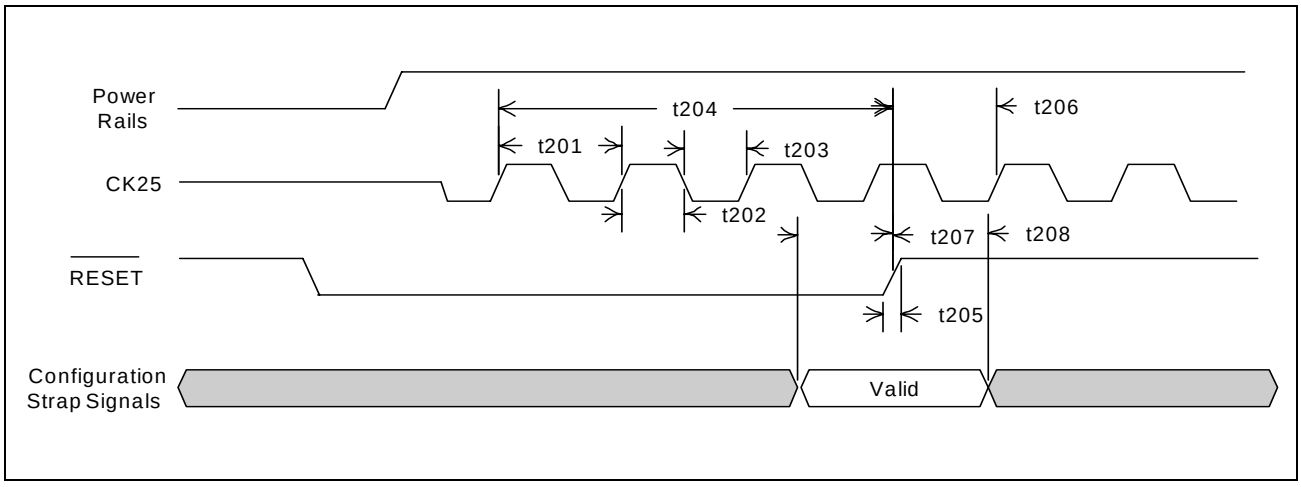


Figure 26: Reset and Clock Timing

Table 158: Reset and Clock Timing

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t201	XTALI/CK25 period	39.998 ns	40.000 ns	40.002 ns
t202	XTALI/CK25 high time	18 ns	–	22 ns
t203	XTALI/CK25 low time	18 ns	–	22 ns
t204	$\overline{\text{RESET}}$ low pulse duration	400 ns	50 ms	–
t207	Configuration valid setup to $\overline{\text{RESET}}$ rising	100 ns	–	–
t208	Configuration valid hold from $\overline{\text{RESET}}$ rising	–	–	0 ns
t209	$\overline{\text{RESET}}$ deassertion to normal switch operation	18.5 ms	–	–

SERIAL LED INTERFACE TIMING

The following specifies timing information regarding the Serial LED pins.

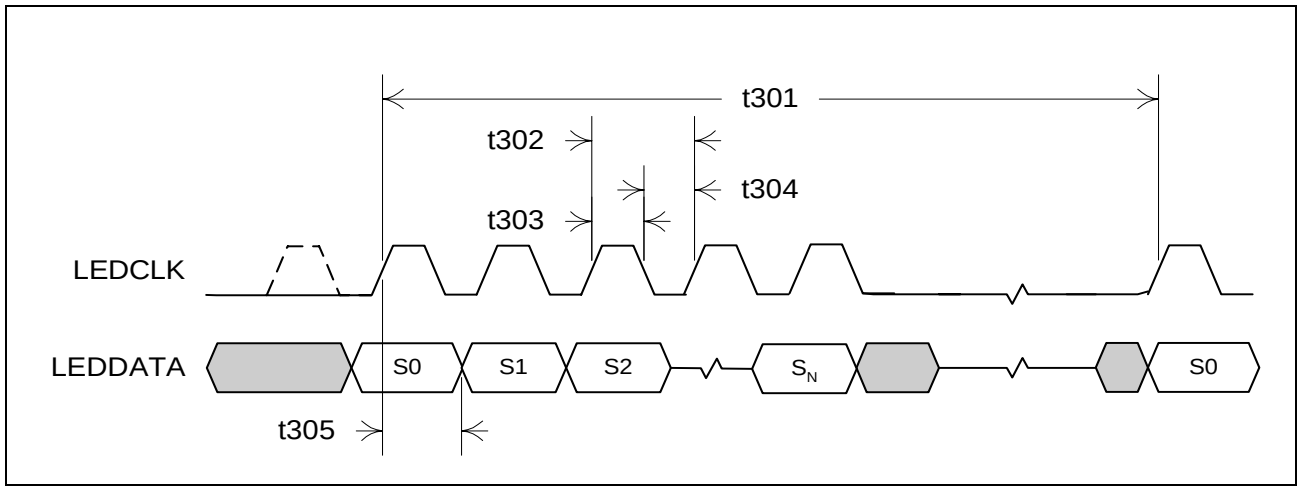


Figure 27: Serial LED Timing

Table 159: Serial LED Timing

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t301	LED update cycle period	–	42 ms	–
t302	LEDCLK period	–	640 ns	–
t303	LEDCLK high pulse width	310 ns	–	330 ns
t304	LEDCLK low pulse width	310 ns	–	330 ns
t305	LEDCLK to LEDDATA output time	270 ns	–	340 ns

MII INTERFACE TIMING

The following specifies timing information regarding the MII Interface pins.

MII INPUT TIMING

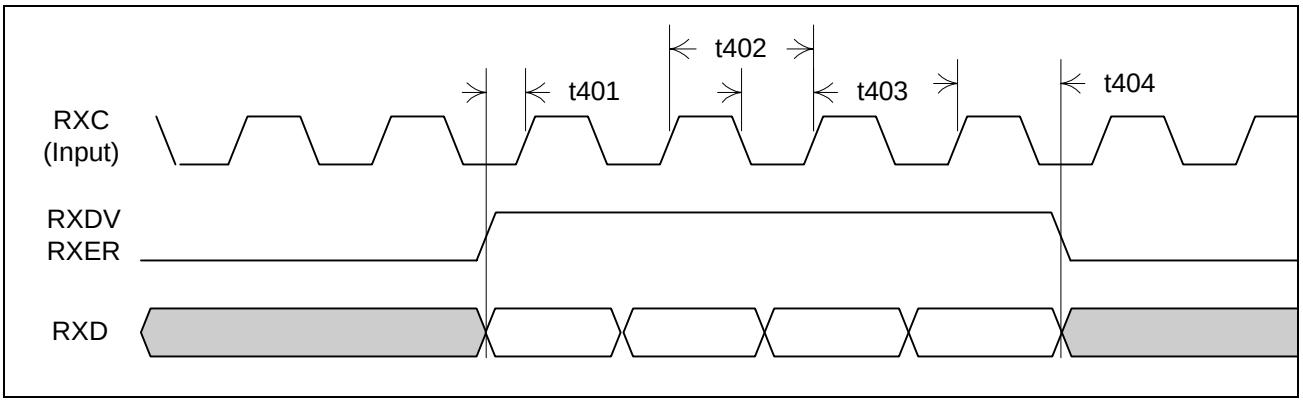


Figure 28: MII Interface Input Timing

Table 160: MII Interface Input Timing

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t401	RXDV, RXD, RXER, to RXC rising setup time	5 ns	–	–
t402	RXC clock period (10BASE-T mode)	–	400 ns	–
	RXC clock period (100BASE-TX mode)	–	40 ns	–
t403	RXC high/low time (10BASE-T mode)	160 ns	–	240 ns
	RXC high/low time (100BASE-TX mode)	14 ns	–	26 ns
t404	RXDV, RXD, RXER, to RXC rising hold time	5 ns	–	–

MII OUTPUT TIMING

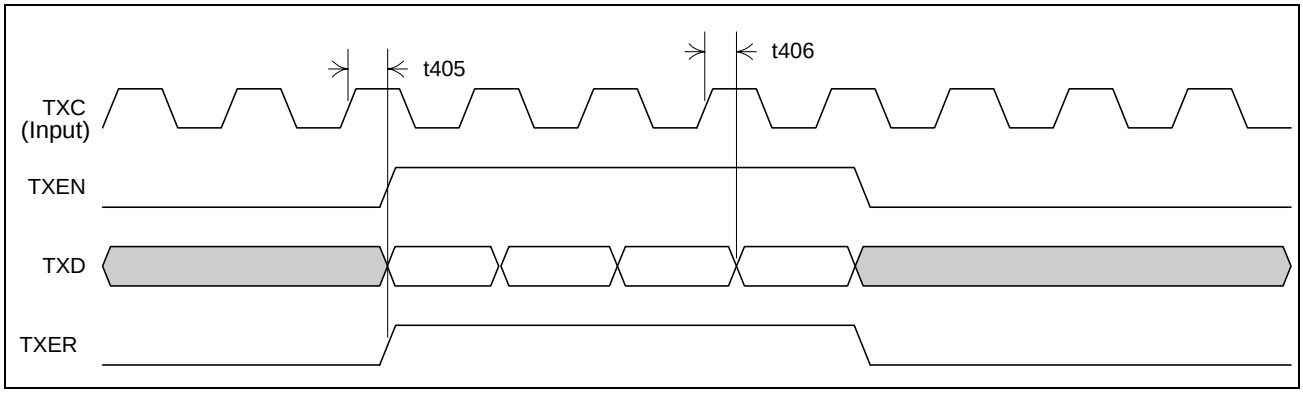


Figure 29: MII Interface Output Timings

Table 161: MII Interface Output Timings

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t405	TXC high to TXEN, TXD, TXER valid	–	–	22 ns
t406	TXC high to TXEN, TXD, TXER invalid	3 ns	–	–

REVERSE MII TIMING

The following specifies timing information regarding the MII Interface pins when in Reverse MII mode.

REVERSE MII INPUT TIMING

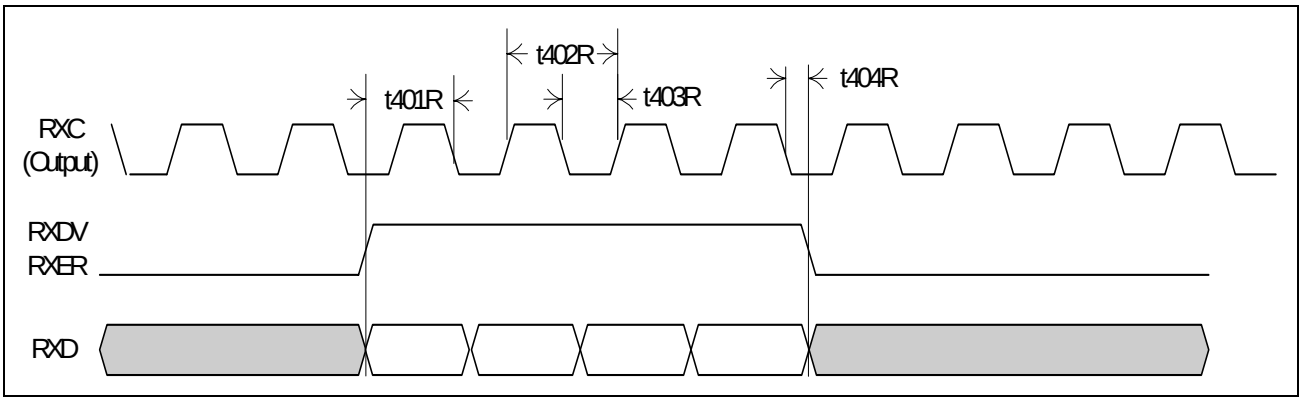


Figure 30: Reverse MII Mode Input Timings

Table 162: Reverse MII Mode Input Timings

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t401R	RXDV, RXD, RXER, to RXC falling setup time	10 ns	–	–
t402R	RXC clock period (100BASE-TX mode only)	–	40 ns	–
t403R	RXC high/low time (100BASE-TX mode only)	14 ns	–	26 ns
t404R	RXDV, RXD, RXER, to RXC falling hold time	0 ns	5 ns	–

REVERSE MII OUTPUT TIMING

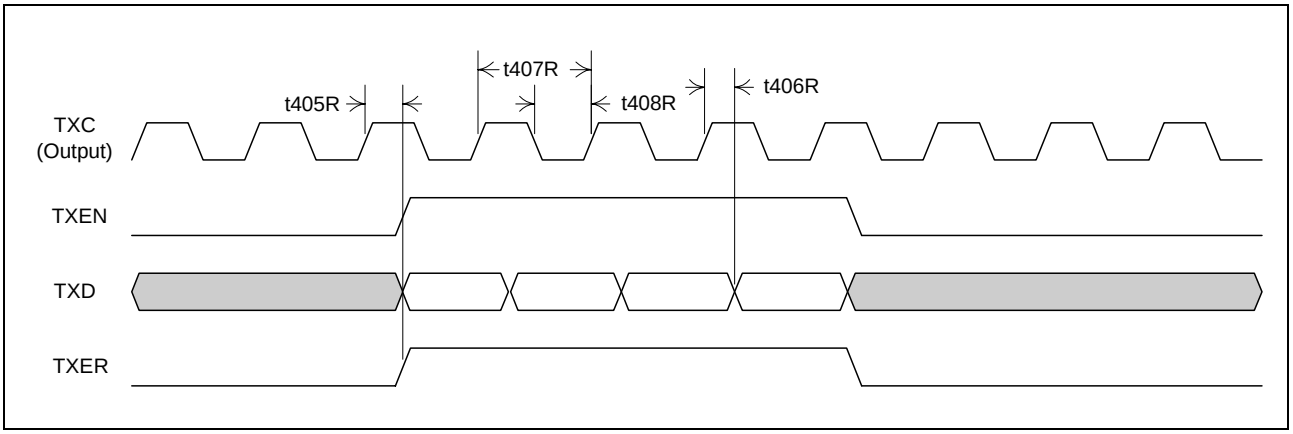


Figure 31: Reverse MII Mode Output Timings

Table 163: Reverse MII Mode Output Timings

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t405R	TXC high to TXEN, TXD, TXER valid	–	–	25 ns
t406R	TXC high to TXEN, TXD, TXER invalid	11 ns	–	–
t407R	TXC clock period	–	40 ns	–
t408R	TXC high/low time	14 ns	–	26 ns

SPI TIMING

The following specifies timing information regarding the Programming Interface pins when in SPI mode:

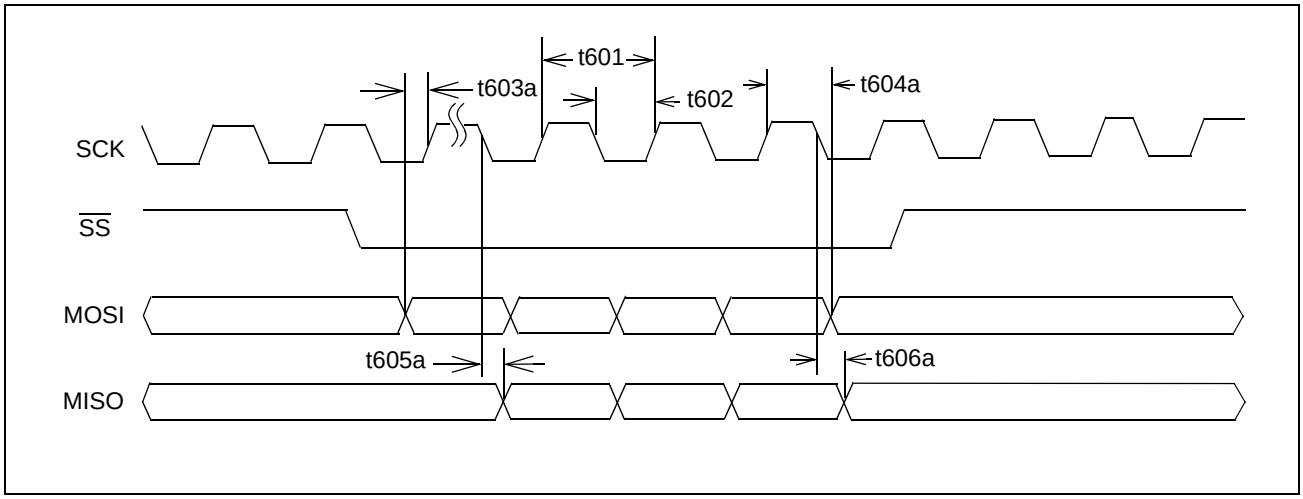


Figure 32: SPI Timings when $\overline{SS}$ Asserted During SCK High

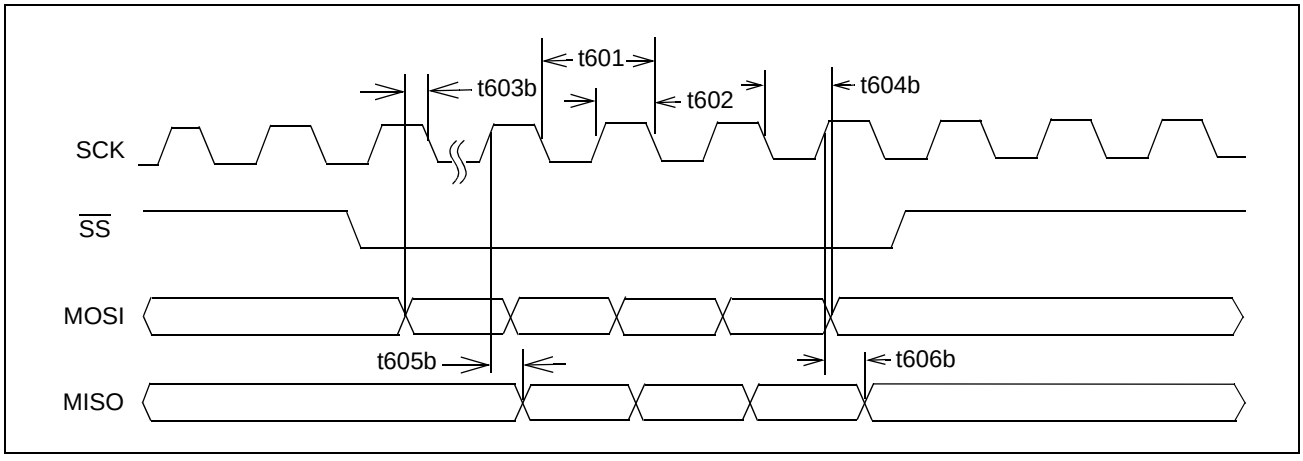


Figure 33: SPI Timings when $\overline{SS}$ Asserted During SCK Low

Table 164: SPI Timings

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t601	SCK clock period	–	500 ns	–
t602	SCK high/low time	200 ns	–	300 ns
t603a, t603b	MOSI to SCK setup time	5 ns	–	–
t604a, t604b	MOSI to SCK hold time	12 ns	–	–
t605a, t605b	SCK to MISO valid	–	–	25 ns
t606a, t606b	SCK to MISO invalid	0 ns	–	–

Note: The BCM5325E behaves only as a slave device. $\overline{SS}$ is asynchronous. If $\overline{SS}$ is asserted during SCK high then BCM5325E samples data on the rising edge of SCK and references the falling edge to output data. Otherwise BCM5325E samples data on the falling edge and outputs data on the rising edge of SCK.

EEPROM TIMING

The following specifies timing information regarding the Programming Interface pins when in EEPROM mode.

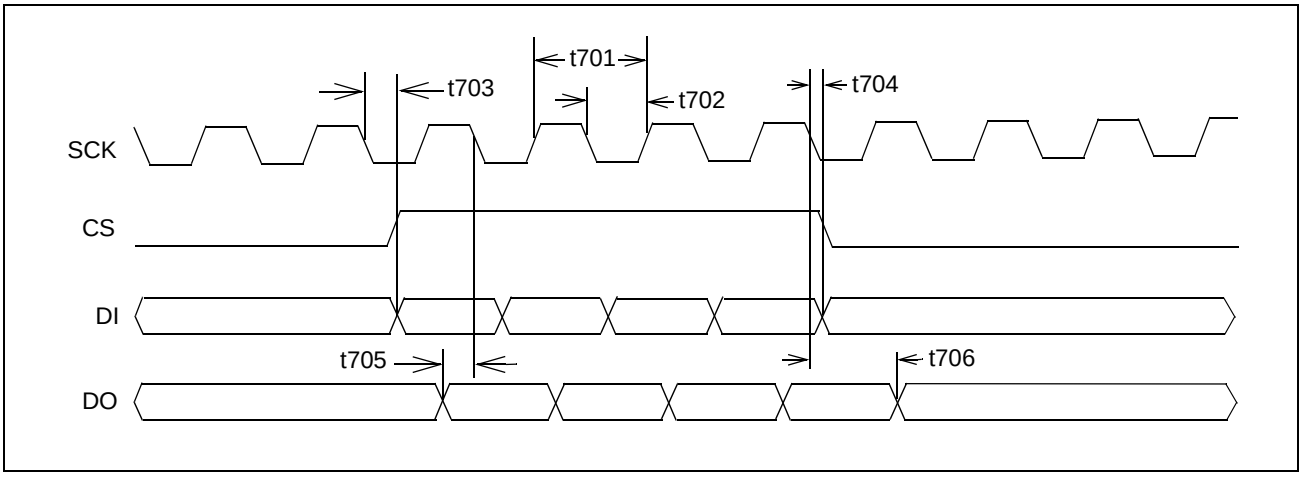


Figure 34: EEPROM Timing

Table 165: EEPROM Timing

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t701	SCK clock frequency	–	100 kHz	–
t702	SCK high/low time	–	5 µs	–
t703	SCK low to CS, DI valid	–	–	500 ns
t704	SCK low to CS, DI invalid	500 ns	–	–
t705	DO to SCK falling setup time	200 ns	–	–
t706	DO to SCK falling hold time	200 ns	–	–

MANAGEMENT DATA INTERFACE TIMING

The following specifies timing information regarding the Management Data Interface pins (MDC/MDIO).

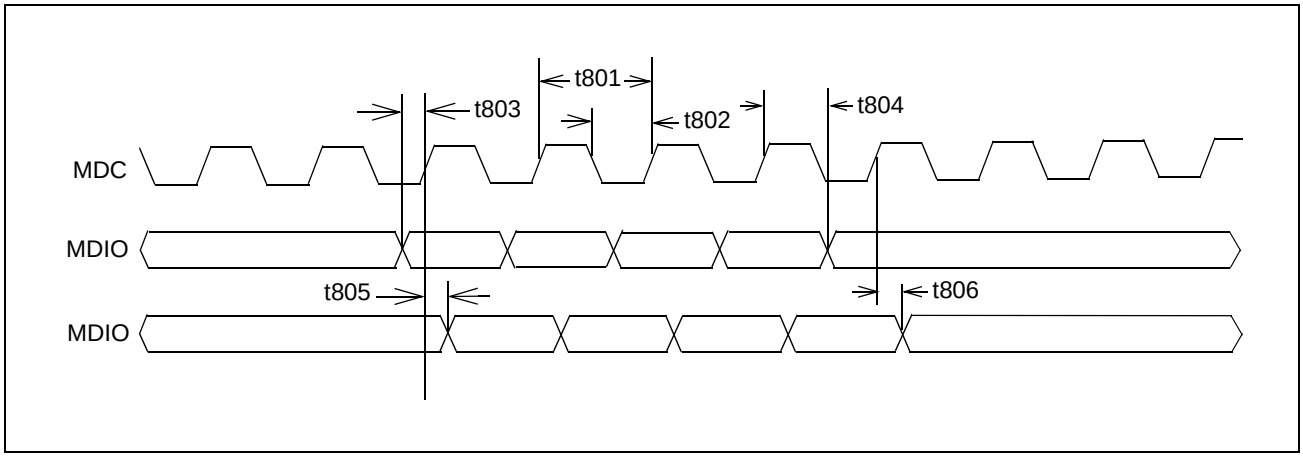


Figure 35: Management Data Interface (Slave Mode)

Table 166: Management Data Interface (Slave Mode)

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t801	MDC clock period	–	80 ns	–
t802	MDC high/low time	30 ns	–	50 ns
t803	MDIO to MDC rising setup time	5 ns	–	–
t804	MDIO to MDC rising hold time	5 ns	–	–
t805	MDC rising to MDIO valid	–	–	50 ns
t806	MDC rising to MDIO invalid	10 ns	–	–

Section 8: Electrical Characteristics

Caution! These specifications indicate conditions where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods may adversely affect the long-term reliability of the device.

Table 167: Absolute Maximum Ratings

Symbol	*Parameter*	*Minimum*	*Maximum*	*Units*
VDD	Supply voltage: VDDC, VDDA, VDDPLL	GND – 0.3	1.98	V
VI	Supply voltage: VDDP, VDDXTAL, input voltage	GND – 0.3	3.60	V
II	Input current	–	±10	mA
TSTG	Storage temperature	–40	+125	°C
VESD	Electrostatic discharge	–	1000	V

Table 168: Recommended Operating Conditions

Symbol	*Parameter*	*Pin Name*	*Minimum*	*Maximum*	*Units*
V_{DD}	Supply voltage	VDDC, VDDA, VDDPLL	1.71	1.89	V
		VDDXTAL	3.135	3.465	V
		VDDP	3.135	3.465	V
V_{IH}	High-level input voltage	All digital inputs	2.0	–	V
V_{IL}	Low-level input voltage	All digital inputs	–	0.8	V
V_{IDIFF}	Differential input voltage	RD± {1:5}	150	–	mV
R_{DAC}	DAC current-setting resistance	RDAC	1.24	1.24	kΩ
T_A	Ambient operating temperature	–	0	70	°C
V_{IDIFF}	Differential input voltage in full threshold mode, 100BASE-EFX	RD±	1000	–	mV, pk-pk
V_{IDIFF}	Differential input voltage in half threshold mode, 100BASE-EFX	RD±	600	–	mV, pk-pk
V_{ICM}	Common mode input voltage, 100BASE-EFX	RD±	1.5	–	VDD

Table 169: Electrical Characteristics

Symbol	Parameter	Pins	Conditions	Minimum	Typical	Maximum	Units
I_{DD}	Total supply current for	1.8V for VDDC, VDDPLL, VDDA	100BASE-TX	–	–	290	mA
		3.3V for VDDP, VDDXTAL	–	–	–	20	mA
		1.8V for front end (center tap) per POR 45 mA	–	–	–	225	mA
		3.3V for front end (center tap) per POR 45 mA	–	–	–	225	mA
TDV cm	Common Mode Voltage	TD±	100BASE-EFX	3.145	–	3.465	V
V_O	Output Voltage	TD±	100BASE-EFX	TDVcm – 2	–	TDV cm	V
V_{OH}	High-level output voltage	$\overline{LEDA}$, $\overline{LEDB}$, $\overline{LEDC}$, LEDDATA, LEDCLK, TXC, TXD, TXEN, TXER, RXC, RXD[0], RXDV, COL, MDIO, MDC, MISO, SCK, CS, DI	I_{OH} = –8 mA	2.4	–	–	V
V_{OH}	High-level output voltage	QOS_FC_DIS	I_{OH} = –10 mA	2.4	–	–	V
V_{OH}	High-level output voltage	TD± {1:5}	Driving loaded magnetics module	–	–	VDD + 1.5	V
V_{OL}	Low-level output voltage	$\overline{LEDA}$, $\overline{LEDB}$, $\overline{LEDC}$, LEDDATA, LEDCLK, TXC, TXD, TXEN, TXER, RXC, RXD[0], RXDV, COL, MDIO, MDC, MISO, SCK, CS, DI	I_{OL} = 8 mA	–	–	0.4	V
V_{OL}	Low-level output voltage	QOS_FC_DIS	I_{OL} = 10 mA	–	–	0.4	V
V_{OL}	Low-level output voltage	TD± {1:5}	Driving loaded magnetics module	VDD – 1.5	–	–	V
I_I	Input current	Digital inputs w/pull-up resistors	V_I = VDDP	–	–	+100	µA
			V_I = GND	–	–	–200	µA
		Digital inputs w/pull-down resistors	V_I = VDDP	–	–	+200	µA
			V_I = GND	–	–	–10	µA
		All other digital inputs	GND ≤ V_I ≤ VDDP	–	–	±100	µA
I_{OZ}	High-impedance output current	All three-state outputs	GND ≤ V_O ≤ VDDP	–	–	±10	µA
		All open-drain outputs	V_O = VDDP	–	–	±10	µA
V_{BIAS}	Bias voltage	RDAC	–	–	1.24	–	V

Section 9: Thermal Information

Table 170: 128-MQFP Thermal Characteristics—Without Heat Sink[a] (2-Layer PCB)

Airflow	*0 fpm 0 mps*	*100 fpm, 0.508 mps*	*200 fpm, 1.016 mps*	*400 fpm, 2.032 mps*	*600 fpm, 3.048 mps*
Theta-JA (^{o}C/W)	51.42	47.81	45.61	43.33	42.11
Theta-JB (^{o}C/W)	35.19	–	–	–	–
Theta-JC (^{o}C/W)	20.66	–	–	–	–
Max junction temperature T_J	–	125^{o}C	–	–	–

a. Without heat sink, Ta = 70°C. This is an estimation based on 2-layer PCB.

Table 171: 128-MQFP Thermal Characteristics—Without Heat Sink[a] (4-Layer PCB)

Airflow	*0 fpm 0 mps*	*100 fpm, 0.508 mps*	*200 fpm, 1.016 mps*	*400 fpm, 2.032 mps*	*600 fpm, 3.048 mps*
Theta-JA (^{o}C/W)	46.65	43.74	42.20	40.66	39.76
Theta-JB (^{o}C/W)	35.19	–	–	–	–
Theta-JC (^{o}C/W)	20.66	–	–	–	–
Max junction temperature T_J	125^{o}C	–	–	–	–

a. Without heat sink, Ta = 70°C. This is an estimation based on 4-layer PCB.

Table 172: 128-MQFP Thermal Characteristics—With Heat Sink[a]

Airflow	*0 fpm 0 mps*	*100 fpm, 0.508 mps*	*200 fpm, 1.016 mps*	*400 fpm, 2.032 mps*	*600 fpm, 3.048 mps*
Theta-JA (°C/W)	35.53	32.40	29.86	27.72	26.93
Theta-JB (°C/W)	35.19	–	–	–	–
Theta-JC (°C/W)	20.66	–	–	–	–
Max junction temperature T_J	125°C	–	–	–	–

a. Without heat sink, Ta = 85°C. This is an estimation based on 2-layer PCB.
Heat sink: TwinPeaks Electronics, TPEF 14-20-10-5B, Extruded Aluminum, 14x20x10 mm, k = 180(W/m*K).
Thermal Interface: T411, 0.23-mm thick tape, Chomerics, k = 0.4 (W/m*K)

Section 10: Mechanical Information

N	A	A1	A2	B	D	D1	D2	E	E1	E2	e	L	L1
128	3.4 Max	0.25 Min	2.70 ±0.2	0.20 0 ±0.07	23.20 ±0.25	20.00 ±0.10	18.50 ±0.10	17.20 ±0.25	14.00 ±0.10	12.50 ±0.10	0.50	0.88 ±0.2	1.60 ±0.12

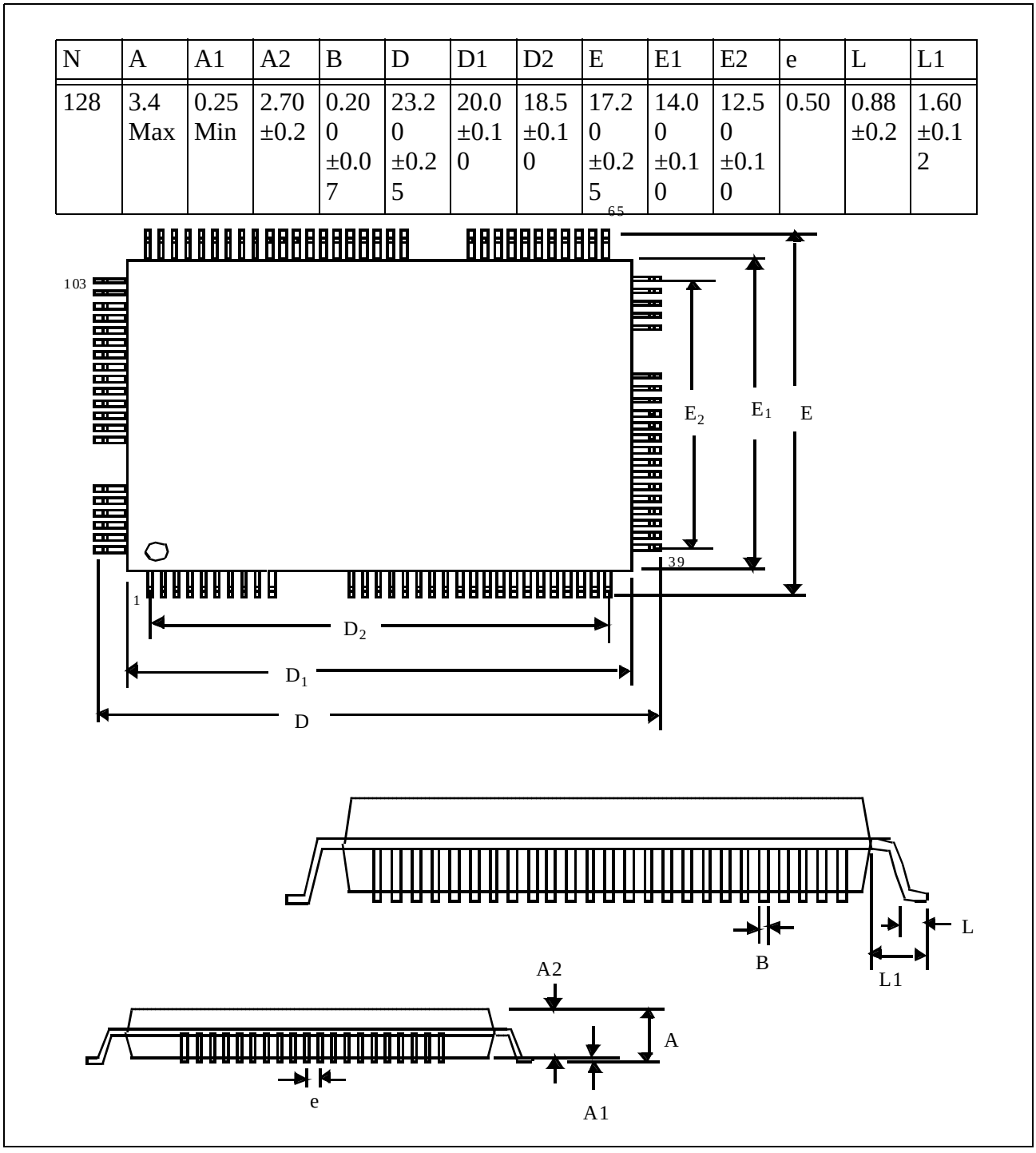


Figure 36: 128-Pin MQFP Package Outline Drawing

Section 11: Ordering Information

Table 173: Ordering Information

Part Number	*Package*	*Ambient Temperature*
BCM5325EKQM(G)	128-MQFP	Commercial Grade 0°C to 70°C
BCM5325EIQM(G)	128-MQFP	Industrial Grade –40°C to 85°C

Note: G indicates that this is a lead-free option.

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